Switched-Capacitor Voltage Converter

Features

- Wide Operating Supply Voltage Range: 4.5 V to 20 V
- 99.7% Open Circuit Voltage Conversion Efficiency
- 95% Power Conversion Efficiency

Benefits

- Inexpensive Negative Supply Generation
- Easy to Use, Requires Only Two External Capacitors
- Minimum Parts Count
- Small Size

Applications

- Conversion of +12-V to ± 12-V Supplies
- RS-232 Power Supply
- Negative Supplies for Analog Circuits
- Data Acquisition Systems
- Handheld Instruments
- High-Side Load Switches

Description

The Si7661 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7661 performs a supply voltage conversion from positive to negative for an input range of +4.5 V to +20 V, resulting in a complementary output voltage of −4.5 V to −20 V with the addition of only two capacitors.

Typical applications for the Si7661 are data acquisition and microprocessor based systems, where a +5- to +20-V supply is available for the digital functions, and an additional −5- to −20-V supply is required for analog devices, such as op amps. The Si7661 is also ideally suited for providing low current, −5-V body bias supply for dynamic RAMs.

Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output n-channel switch substrates are not forward-biased. An epitaxial layer prevents latchup.

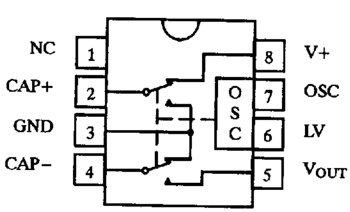
The oscillator, when unloaded, runs at a nominal frequency of 10 kHz for an input supply voltage of 4.5 to 20 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+8 to +20 V), the "LV" pin should be left disconnected.

For applications information refer to AN401.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	8-Pin Plastic MiniDIP	Si7661CJ
−40 to 85°C		Si7661DJ

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Absolute Maximum Ratings

Supply Voltage (V+ to GND or GND to V_{OUT}) .... 22 V
Oscillator Input Voltage
V+ <8 V .... −0.3 V to (V+) +0.3 V
V+ >8 V .... (V+) −8 V to (V+) +0.2 V
LV .... No connection for V+ >9 V
Storage Temperature .... −65 to 125°C

Power Dissipation:[a]
8-Pin Plastic MiniDIP[b] .... 500 mW

Notes:
a. All leads welded or soldered to PC board.
b. Derate 6.6 mW/°C above 25°C.

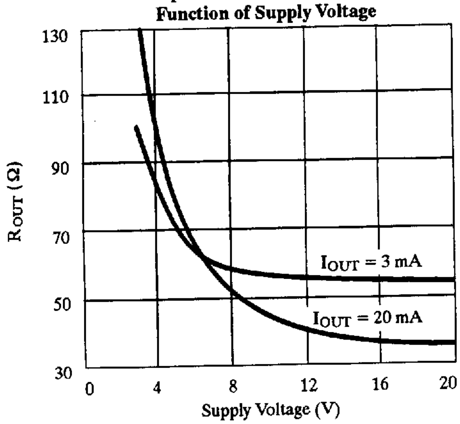
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, C_{OSC} = 0[d]	Temp[a]	Limits Min[b]	Typ[c]	Max[b]	Unit
Input							
Supply Voltage Range Low	$V+_L$	R_L = 10 kΩ, LV = GND	Full	4.5		9	V
Supply Voltage Range High	$V+_H$	R_L = 10 kΩ, LV = Open	Full	8		20	V
Supply Current	I+	V+ = 4.5 V, R_L = ∞, LV = GND	Full		100	200	µA
		V+ = 15 V, R_L = ∞, LV = Open	Full		0.7	2	mA
Output							
Output Source Resistance	R_{OUT}	V+ = 4.5 V, LV = GND, I_{OUT} = 3 mA	Room		35		Ω
		V+ = 15 V, LV = Open, I_{OUT} = 20 mA	Room		30	100	
			Full			120	
Power Conversion Efficiency	P_{EF}	V+ = 15 V, R_L = 2 kΩ	Room		92		%
Voltage Conversion Efficiency	V_{EF}	V+ = 15 V, R_L = ∞	Room	97	99.7		
Dynamic							
Oscillator Frequency[d]	f_{OSC}	V+ = 15 V	Room		10		kHz
Oscillator Impedance	Z_{OSC}	V+ = 4.5 V, LV = GND	Room		1		MΩ
		V+ = 15 V	Room		100		kΩ

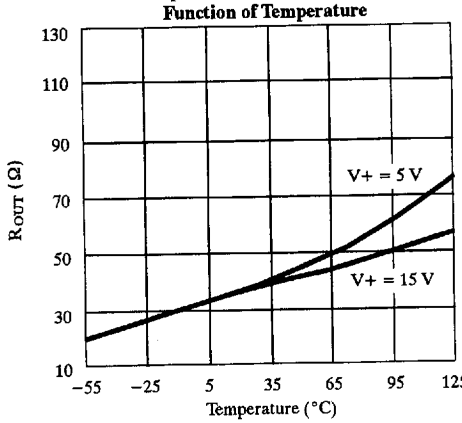
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. For C_{OSC} > 1000 pF, C_1 and C_2 should be increased to 100 µF. C_1 = Pump Capacitor, C_2 = Reservoir Capacitor.

Typical Characteristics

Output Source Resistance as a Function of Supply Voltage



Output Source Resistance as a Function of Temperature



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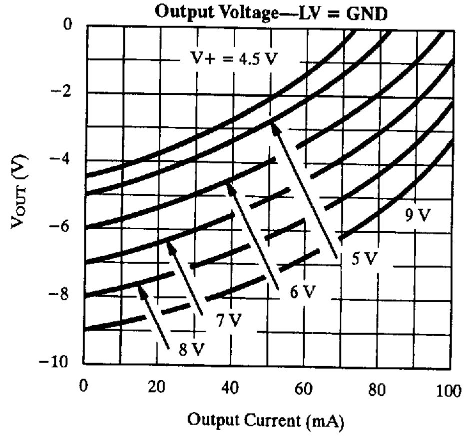
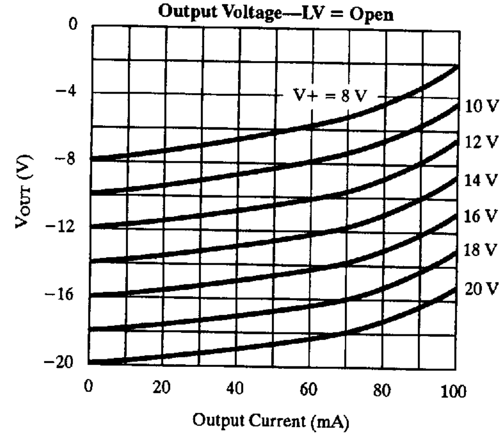
Typical Characteristics (Cont'd)

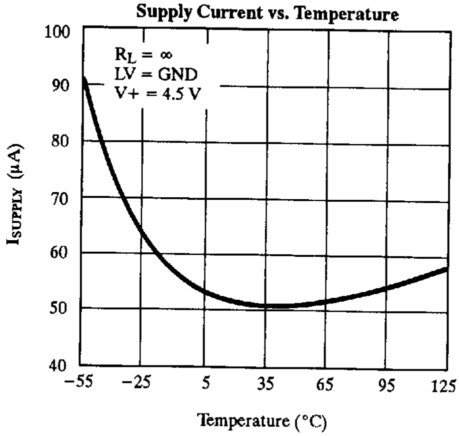
Output Voltage—LV = GND



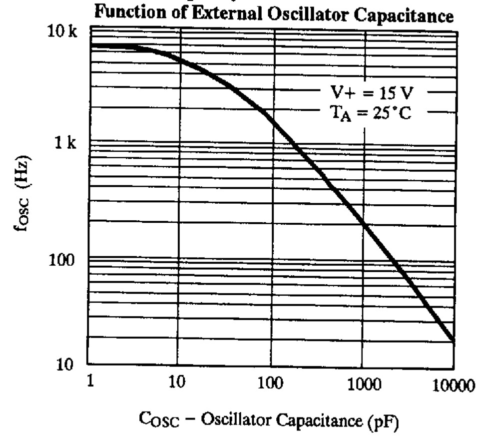
Output Voltage—LV = Open



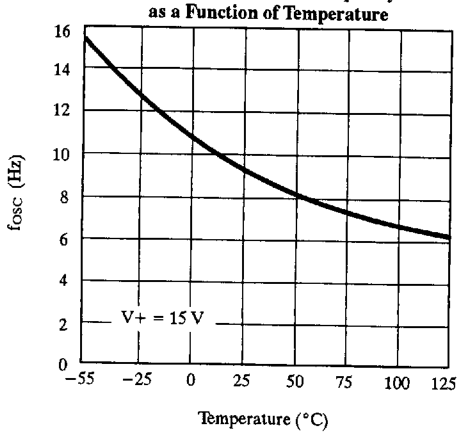
Supply Current vs. Temperature



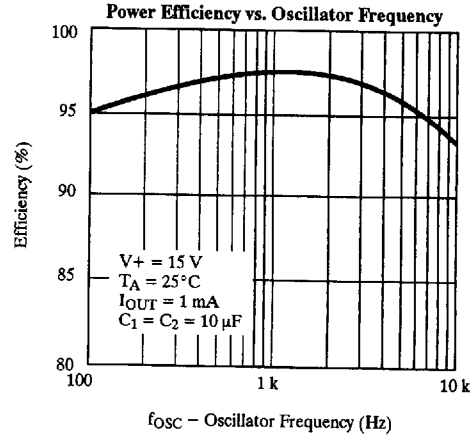
Frequency of Oscillation as a Function of External Oscillator Capacitance



Unloaded Oscillator Frequency as a Function of Temperature



Power Efficiency vs. Oscillator Frequency



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Schematic Diagram

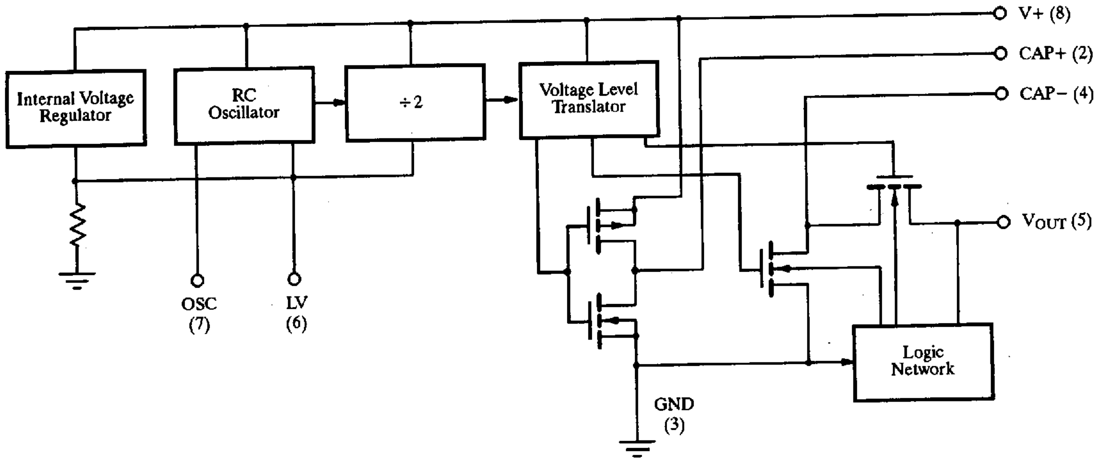


Figure 1.

Test Circuit

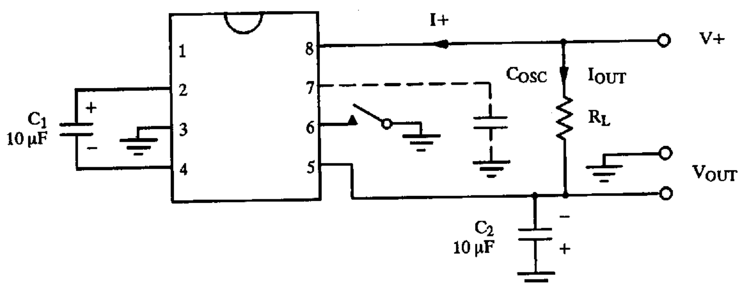


Figure 2.

Applications

The Si7661 contains all the circuitry necessary to make a charge pump for voltage inversion, doubling, division, multiplication, etc. Only two external capacitors are needed and they may be inexpensive electrolytics. Since the output resistance is in the tens of ohms, heavy load currents will reduce the output voltage and eventually may cause the device to go into shutdown.

There are many applications where a low current supply made with a charge pump does just as well as a conventional, fully regulated negative supply or dc-to-dc converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems. In addition, the extended input voltage range of the Si7661 lends itself for use as a negative generator for most op-amp applications.

Applications (Cont'd)

If the output ripple of the Si7661 is too great for a particular application, the value of the pump (C_1, Figure 3) and reservoir (C_2) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000 μF.

When an external clock is used to drive the Si7661 a 1-kΩ resistor should be used between the clock source and the OSC input (Pin 7) as shown in Figure 4.

Figure 5 shows a regulator that will operate with much less than 1-V drop between V+ and V_{OUT} at large output currents. Most three-terminal voltage regulators would exhibit a drop of a volt or more under these conditions.

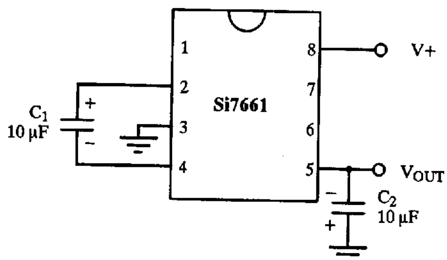


Figure 3. Basic Inverter Circuit

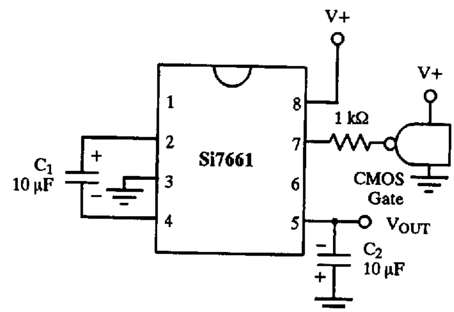
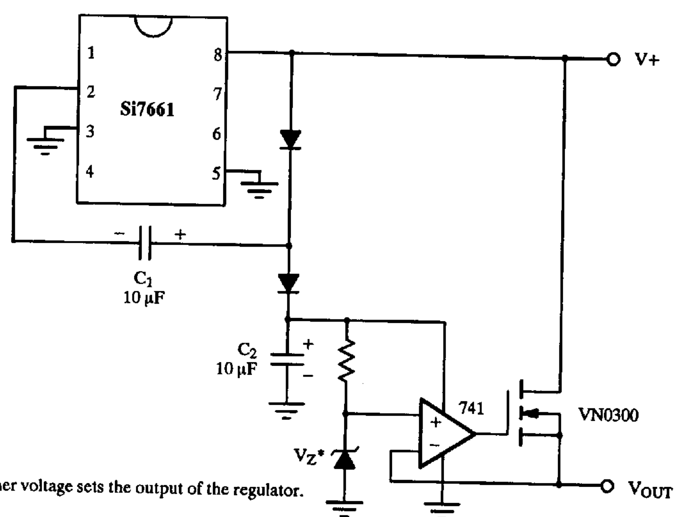


Figure 4. Driving the Si7661 with an External Clock



*The Zener voltage sets the output of the regulator.

Figure 5. Low Loss Regulator Circuit

Applications (Cont'd)

Battery Splitter

To obtain supplies from a single battery or power supply, the circuit shown in Figure 6 offers a simple solution. It generates symmetrical ± output voltages equal to one-half the input voltage. Both output voltages are referenced to Pin 3 (output common). To improve low-voltage operation, Pin 6 should be connected to Pin 3 when the input voltage is less than 9 V.

High Precision Voltage Divider

A high precision voltage divider is shown in Figure 7. Increasing the load current beyond 100 nA will cause a small loss in accuracy.

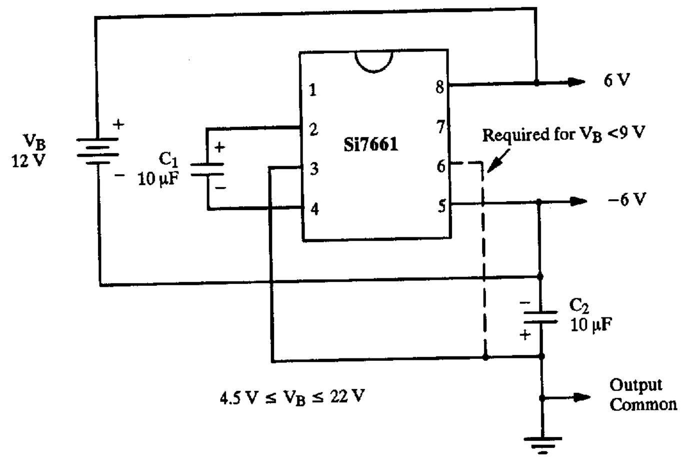


Figure 6. Battery Splitter

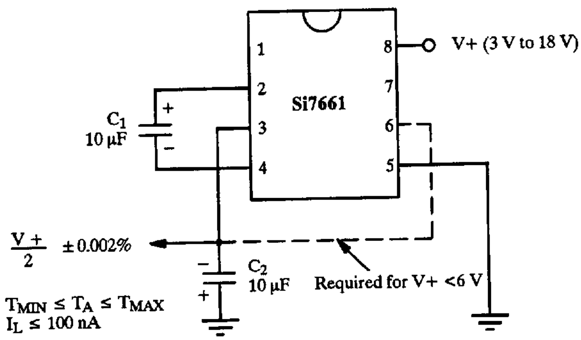


Figure 7. High Precision Voltage Divider

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