- Inputs are TTL-Voltage Compatible

- Independent Registers for A and B Buses

- Multiplexed Real-Time and Stored Data

- Inverting Data Paths

- Flow-Through Architecture Optimizes PCB Layout

- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise

- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process

- 500-mA Typical Latch-Up Immunity at 125°C

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11648 . . . JT PACKAGE
74ACT11648 . . . DW OR NT PACKAGE
(TOP VIEW)

$\overline{G}$	1		28	CAB
A1	2		27	SAB
A2	3		26	B1
A3	4		25	B2
A4	5		24	B3
GND	6		23	B4
GND	7		22	V_{CC}
GND	8		21	V_{CC}
GND	9		20	B5
A5	10		19	B6
A6	11		18	B7
A7	12		17	B8
A8	13		16	CBA
DIR	14		15	SBA

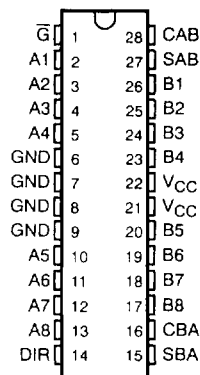54ACT11648 . . . FK PACKAGE
(TOP VIEW)

description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.
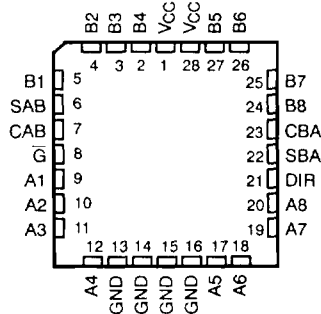
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 54ACT11648 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11648 is characterized for operation from – 40°C to 85°C.

TEXAS
INSTRUMENTS

54ACT11648, 74ACT11648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A

1	14	28	26	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B

1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B

1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS-MANAGEMENT FUNCTIONS

Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified[†]	Store A, B unspecified[†]
X	X	X	↑	X	X	Unspecified[†]	Input	Store B, A unspecified[†]
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Store $\overline{A}$ Data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol[‡]
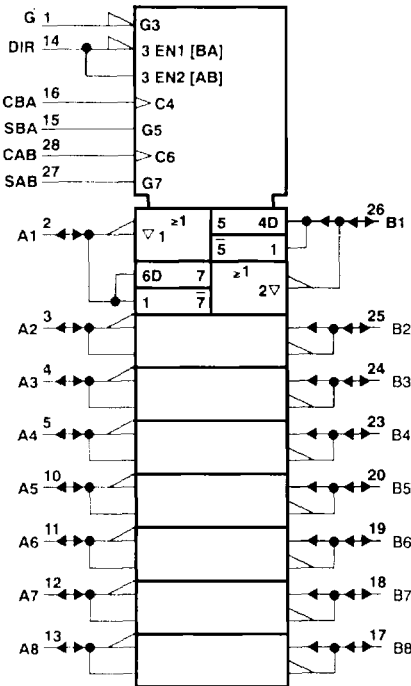
logic diagram (positive logic)

TO 7 OTHER CHANNELS
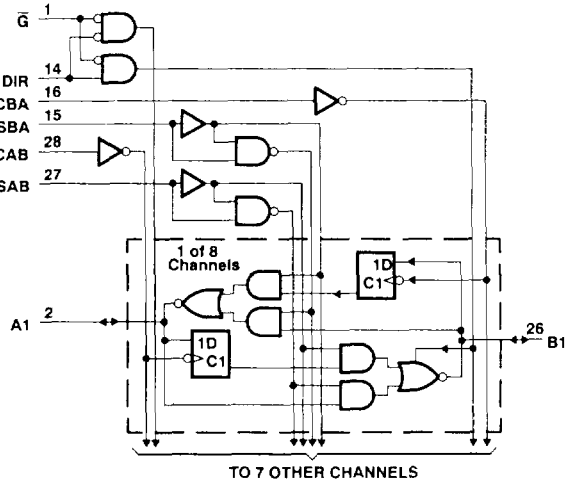
[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	$-65°C$ to $150°C$

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11648			74ACT11648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			-24			-24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t / \Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-55		125	-40		85	°C

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	54ACT11648 MIN	MAX	74ACT11648 MIN	MAX	UNIT
V_{OH}		$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50$ mA†	5.5 V				3.85				
		$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}		$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		$I_{OL} = 50$ mA†	5.5 V					1.65			
		$I_{OL} = 75$ mA†	5.5 V							1.65	
I_I	Control Inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{OZ}	A or B ports‡	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_I = V_{CC}$ or GND	5 V		12						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage currrent.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements, $V_{CC} = 5$ V ± 0.5 V (see Note 2)

		$T_A = 25°C$ MIN	MAX	54ACT11648 MIN	MAX	74ACT11648 MIN	MAX	UNIT
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CAB or CBA high or low	6.7		6.7		6.7		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	5		5		5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2		2		2		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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54ACT11648, 74ACT11648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS
D3458, MARCH 1990- REVISED OCTOBER 1990

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11648		74ACT11648		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	A or B	B or A	2.4	6.5	9.5	2.4	11.6	2.4	10.7	ns
t_{PHL}			4.4	8.5	11.3	4.4	13.8	4.4	12.7	
t_{PZH}	$\overline{G}$	A or B	4.2	9.2	13	4.2	15.8	4.2	14.6	ns
t_{PZL}			4.3	9.8	13.9	4.3	16.9	4.3	15.6	
t_{PHZ}	$\overline{G}$	A or B	5.7	8.7	11.3	5.7	12.9	5.7	12.2	ns
t_{PLZ}			5.3	8.1	10.5	5.3	12.1	5.3	11.4	
t_{PLH}	CBA or CAB	A or B	5.2	9.4	12	5.2	14.9	5.2	13.7	ns
t_{PHL}			6	10.5	13.5	6	16.3	6	15.2	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4.7	8.6	11.3	4.7	14	4.7	12.9	ns
t_{PHL}			3.8	8.6	12	3.8	14.3	3.8	13.4	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	2.6	7.1	10.2	2.6	12.5	2.6	11.5	ns
t_{PHL}			5.4	9.7	12.6	5.4	15.2	5.4	14.1	
t_{PZH}	DIR	A or B	3.9	9.8	14.9	3.9	18.4	3.9	16.9	ns
t_{PZL}			3.9	10.8	15.1	3.9	18.7	3.9	17.2	
t_{PHZ}	DIR	A or B	4.5	8.2	10.6	4.5	12	4.5	11.5	ns
t_{PLZ}			3.9	7.3	9.6	3.9	11.9	3.9	11.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per transceivers	Outputs enabled	C_L = 50 pF,	f = 1 MHz	61	pF
	Outputs disabled			15	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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2-26