SIEMENS

High-Performance
8-Bit Single Chip Microcontroller

SAB 80515/80535

Preliminary

SAB 80515 Microcontroller with factory mask-programmable ROM
SAB 80535 Microcontroller for external ROM

- 8 K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processo
- 256-bit-addressable locations
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Two temperature ranges available:
  0 to 70 °C
  – 40 to 85 °C (T40/85)

The SAB 80515/80535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in + 5 V N-channel, silicon-gate Siemens MYMOS technology. The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).

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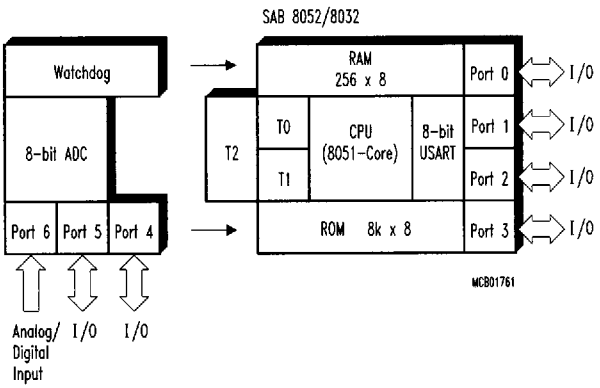

Ordering Information

Type	Ordering code	Package	Description 8-bit CMOS microcontroller
SAB 80515-N	Q 67120-C211	P-LCC-68	with mask-programmable ROM
SAB 80535-N	Q 67120-C241	P-LCC-68	for external memory
SAB 80515-N-T40/85	Q 67120-C210	P-LCC-68	with mask-programmable ROM
SAB 80535-N-40/85	Q 67120-C240	P-LCC-68	for external memory

Note: Extended temperature range – 40 to 110 °C on request

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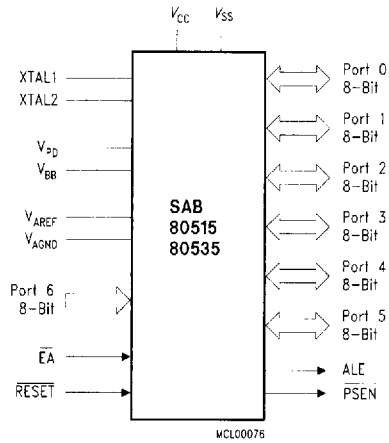
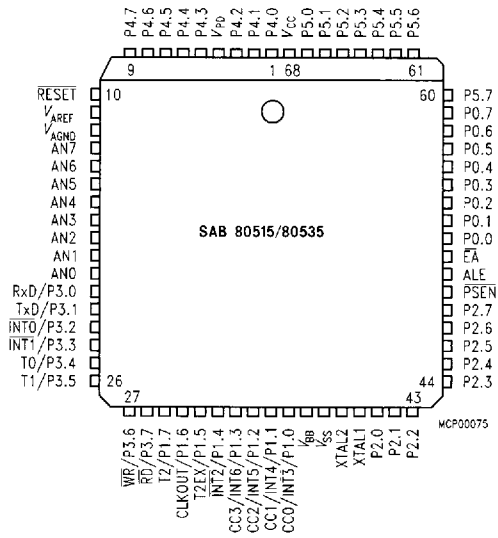


Logic Symbol



Pin Configuration
(P-LCC-68)

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Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port . Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4	I	Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs

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Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads.The secondary functions are assigned to the pins of port 3, as follows: – R × D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T × D (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$(P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$(P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$(P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0

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Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7 - P1.0	29 - 36	I/O	Port 1 is an 8-bit bidirectional I/O port .It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – $\overline{\text{INT2}}$(P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39	–	XTAL2 is the output from the oscillator's amplifier.Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40	–	XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.

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Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0-P2.7	41- 48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+ 5 V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

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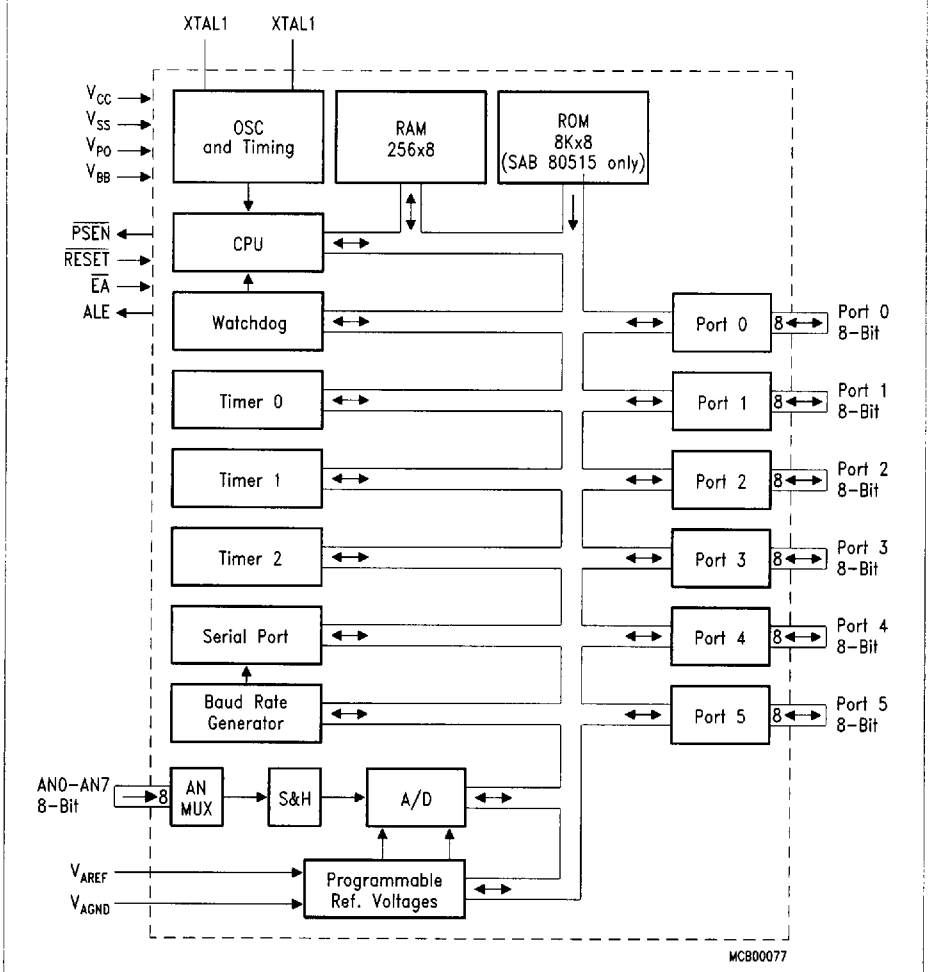

Figure 1
Block Diagram

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Functional Description

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described in the following. (Figure 2 illustrates the memory address spaces of the SAB 80515).

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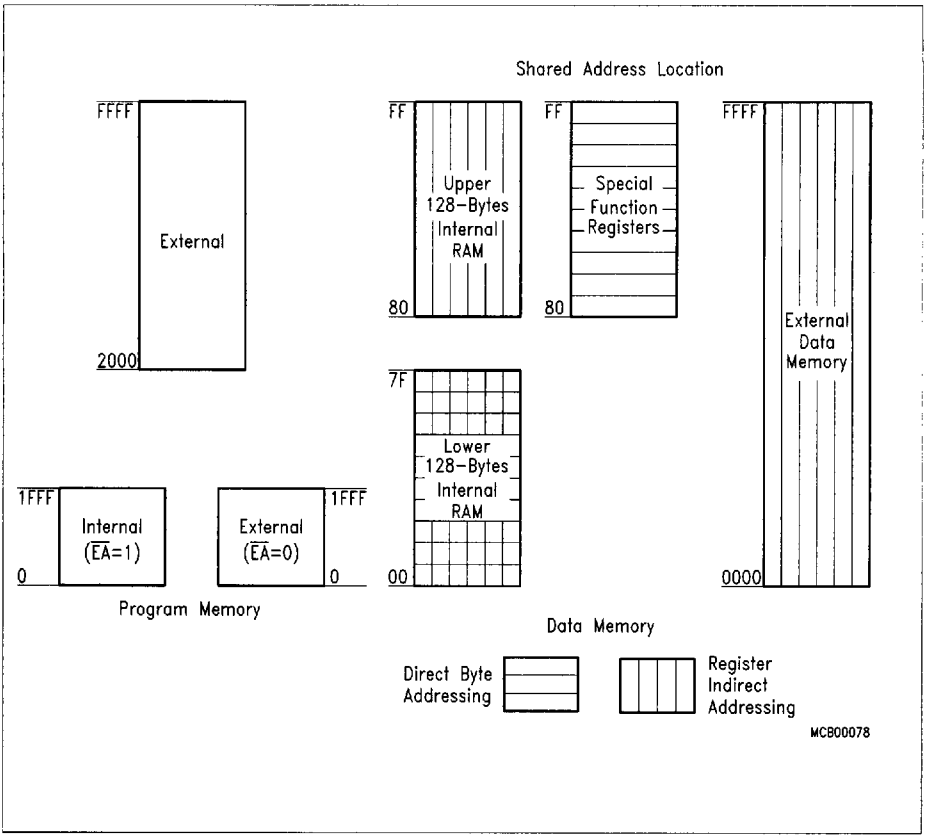

Figure 2
Memory Address Spaces

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Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds $1FFF_H$. Locations 2000_H through $0FFFF_H$ are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through $1F_H$ in the lower RAM area. The next 16 bytes, locations 20_H through $2F_H$, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

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Special Function Registers

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

In table 1 they are organized in numeric order of their addresses. In table 2 they are organized in groups which refer to the functional blocks of the SAB 80515/80535.

Table 1
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	$0FF_H$	98_H	**SCON** [1]	00_H
81_H	SP	07_H	99_H	SBUF	XXXX $XXXX_B$
82_H	DPL	00_H	$9A_H$	reserved	XX_H [2]
83_H	DPH	00_H	$9B_H$	reserved	XX_H [2]
84_H	reserved	XX_H [2]	$9C_H$	reserved	XX_H [2]
85_H	reserved	XX_H [2]	$9D_H$	reserved	XX_H [2]
86_H	reserved	XX_H [2]	$9E_H$	reserved	XX_H [2]
87_H	PCON	000X 0000_B [2]	$9F_H$	reserved	XX_H [2]
88_H	**TCON** [1]	00_H	$A0_H$	**P2** [1]	$0FF_H$
89_H	TMOD	00_H	$A1_H$	reserved	XX_H [2]
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H [2]
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H [2]
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H [2]
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	$A6_H$	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	$A7_H$	reserved	XX_H [2]
90_H	**P1** [1]	$0FF_H$	$A8_H$	**IEN0** [1]	00_H
91_H	reserved	XX_H [2]	$A9_H$	IP0	X000 0000_B [2]
92_H	reserved	XX_H [2]	AA_H	reserved	XX_H [2]
93_H	reserved	XX_H [2]	AB_H	reserved	XX_H [2]
94_H	reserved	XX_H [2]	AC_H	reserved	XX_H [2]
95_H	reserved	XX_H [2]	AD_H	reserved	XX_H [2]
96_H	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
97_H	reserved	XX_H [2]	AF_H	reserved	XX_H [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

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Table 1
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3**[1]	**$0FF_H$**	**$D0_H$**	**PSW** [1]	**00_H**
$B1_H$	reserved	XX_H[2]	$D1_H$	reserved	XX_H[2]
$B2_H$	reserved	XX_H[2]	$D2_H$	reserved	XX_H[2]
$B3_H$	reserved	XX_H[2]	$D3_H$	reserved	XX_H[2]
$B4_H$	reserved	XX_H[2]	$D4_H$	reserved	XX_H[2]
$B5_H$	reserved	XX_H[2]	$D5_H$	reserved	XX_H[2]
$B6_H$	reserved	XX_H[2]	$D6_H$	reserved	XX_H[2]
$B7_H$	reserved	XX_H[2]	$D7_H$	reserved	XX_H[2]
$B8_H$	**IEN1** [1]	**00_H**	**$D8_H$**	**ADCON**	**$00X0\ 0000_B$** [2]
$B9_H$	IP1	$XX00\ 0000_B$ [2]	$D9_H$	ADDAT	00_H
BA_H	reserved	XX_H[2]	DA_H	DAPR	00_H
BB_H	reserved	XX_H[2]	DB_H	P6	
BC_H	reserved	XX_H[2]	DC_H	reserved	XX_H[2]
BD_H	reserved	XX_H[2]	DD_H	reserved	XX_H[2]
BE_H	reserved	XX_H[2]	DE_H	reserved	XX_H[2]
BF_H	reserved	XX_H[2]	DF_H	reserved	XX_H[2]
$C0_H$	**IRCON** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	reserved	XX_H[2]
$C2_H$	CCL1	00_H	$E2_H$	reserved	XX_H[2]
$C3_H$	CCH1	00_H	$E3_H$	reserved	XX_H[2]
$C4_H$	CCL2	00_H	$E4_H$	reserved	XX_H[2]
$C5_H$	CCH2	00_H	$E5_H$	reserved	XX_H[2]
$C6_H$	CCL3	00_H	$E6_H$	reserved	XX_H[2]
$C7_H$	CCH3	00_H	$E7_H$	reserved	XX_H[2]
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**$0FF_H$**
$C9_H$	reserved	XX_H[2]	$E9_H$	reserved	XX_H[2]
CA_H	CRCL	00_H	EA_H	reserved	XX_H[2]
CB_H	CRCH	00_H	EB_H	reserved	XX_H[2]
CC_H	TL2	00_H	EC_H	reserved	XX_H[2]
CD_H	TH2	00_H	ED_H	reserved	XX_H[2]
CE_H	reserved	XX_H[2]	EE_H	reserved	XX_H[2]
CF_H	reserved	XX_H[2]	EF_H	reserved	XX_H[2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

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Table 1
Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$F0_H$	B [1]	00_H	$F8_H$	P5 [1]	$0FF_H$
$F1_H$	reserved	XX_H [2]	$F9_H$	reserved	XX_H [2]
$F2_H$	reserved	XX_H [2]	FA_H	reserved	XX_H [2]
$F3_H$	reserved	XX_H [2]	FB_H	reserved	XX_H [2]
$F4_H$	reserved	XX_H [2]	FC_H	reserved	XX_H [2]
$F5_H$	reserved	XX_H [2]	FD_H	reserved	XX_H [2]
$F6_H$	reserved	XX_H [2]	FE_H	reserved	XX_H [2]
$F7_H$	reserved	XX_H [2]	FF_H	reserved	XX_H [2]

[1] Bit-addressable Special Function Register
[2] X means that the value is indeterminate and the location is reserved

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Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumululator	**$0E0_H$** [1]	00_H
	B	B-Register	**$0F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	083_H	00_H
	DPL	Data Pointer, Low Byte	082_H	00_H
	PSW	Program Status Word Register	**$0D0_H$** [1]	00_H
	SP	Stack Pointer	081_H	07_H
A/D-Converter	ADCON [2]	A/D Converter Control Register	**$0D8_H$** [1]	$00X0\ 0000_B$ [3]
	ADDAT	A/D Converter Data Register	$09D_H$	00_H
	DAPR	A/D Converter Program Register	$0DA_H$	00_H)
Interrupt System	IEN0 [2]	Interrupt Enable Register 0	**$0A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$0B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$0A9_H$	$X000\ 0000_B$ [3]
	IP1	Interrupt Priority Register 1	$0B9_H$	$XX00\ 0000_B$ [3]
	IRCON	Interrupt Request Control Register	**$0C0_H$** [1]	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$0C8_H$** [1]	00_H
Compare/ Capture- Unit Compare/ Capture- Unit (CCU) (cont'd) (CCU)	CCEN	Comp./Capture Enable Reg.	$0C1_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$0C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$0C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$0C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$0C2_H$	00_H
	CCL2	Comp./Capture Reg. 2. Low Byte	$0C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$0C6_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	$0CB_H$	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	$0CA_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
	T2CON [2]	Timer 2 Control Register [1]	**$0C8_H$** [1]	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks
3) X means that the value is indeterminate

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Table 2
Special Function Registers- Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** [1]	$0FF_H$
	P1	Port 1	**90_H** [1]	$0FF_H$
	P2	Port 2	**$0A0_H$** [1]	$0FF_H$
	P3	Port 3	**$0B0_H$** [1]	$0FF_H$
	P4	Port 4	**$0E8_H$** [1]	$0FF_H$
	P5	Port 5	**$0F8_H$** [1]	$0FF_H$
	P6	Port 6, Analog/Digital Input	$0DB_H$	
Pow. Sav. Modes	PCON [2]	Power Control Register	087_H	000X 0000 B [2]
Serial Channels	ADCON [2]	A/D Converter Control Reg.	**$0D8_H$** [1]	00X0 0000_B [3]
	PCON [2]	Power Control Register	087_H	000X 0000_B [3]
	SBUF	Serial Channel Buffer Reg.	099_H	XXXX $XXXX_B$ [3]
	SCON	Serial Channel Control Reg.	**098_H** [1]	00_H
Timer 0/ Timer 1	TCON [2]	Timer Control Register	**088_H** [1]	00_H
	TH0	Timer 0. High Byte	$08C_H$	00_H
	TH1	Timer 1, High Byte	$08D_H$	00_H
	TL0	Timer 0, Low Byte	$08A_H$	00_H
	TL1	Timer 1, Low Byte	$08B_H$	00_H
	TMOD	TImer Mode Register	089_H	00_H
Watchdog	IEN0 [2]	Interrupt Enable Register 0	**$0A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$0B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$0A9_H$	X000 0000_B [3]

[1] Bit-addressable special function registers
[2] This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
[3] X means that the value is indeterminate and the location is reserved

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Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 3 shows a block diagram of the A/D converter.

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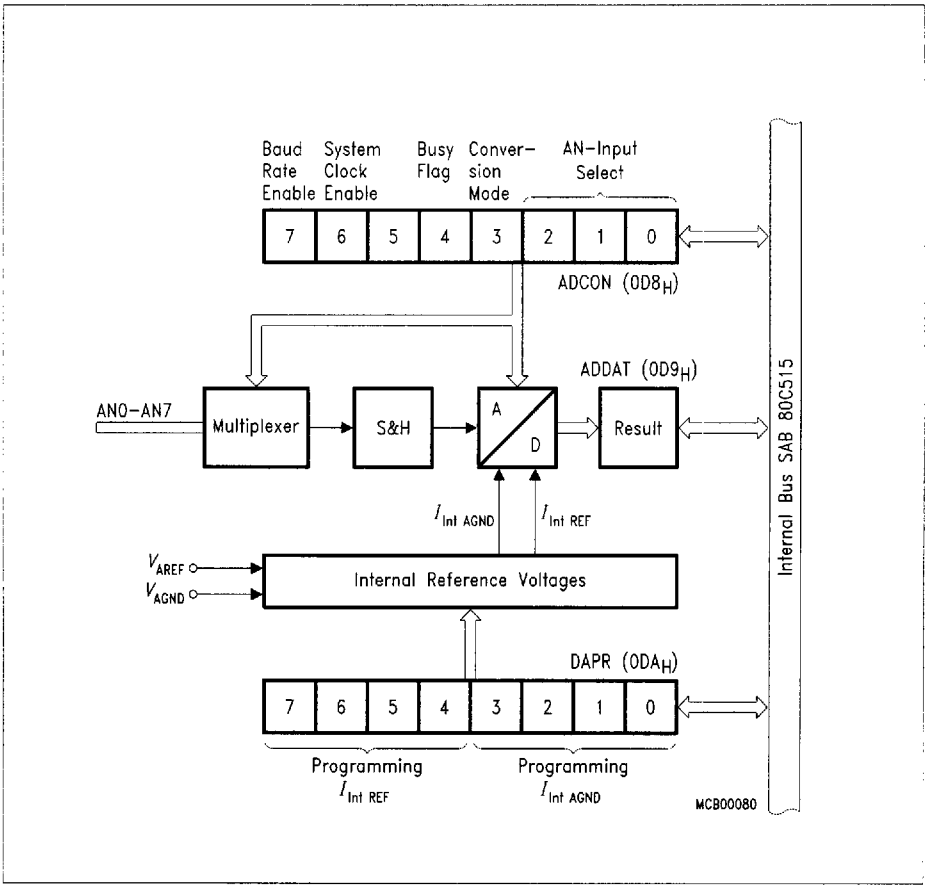


Figure 3
Block Diagram of the A/D Converter

8235605 0082094 390

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 4 shows a block diagram of the timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

8235605 0082095 227

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

8235605 0082096 163

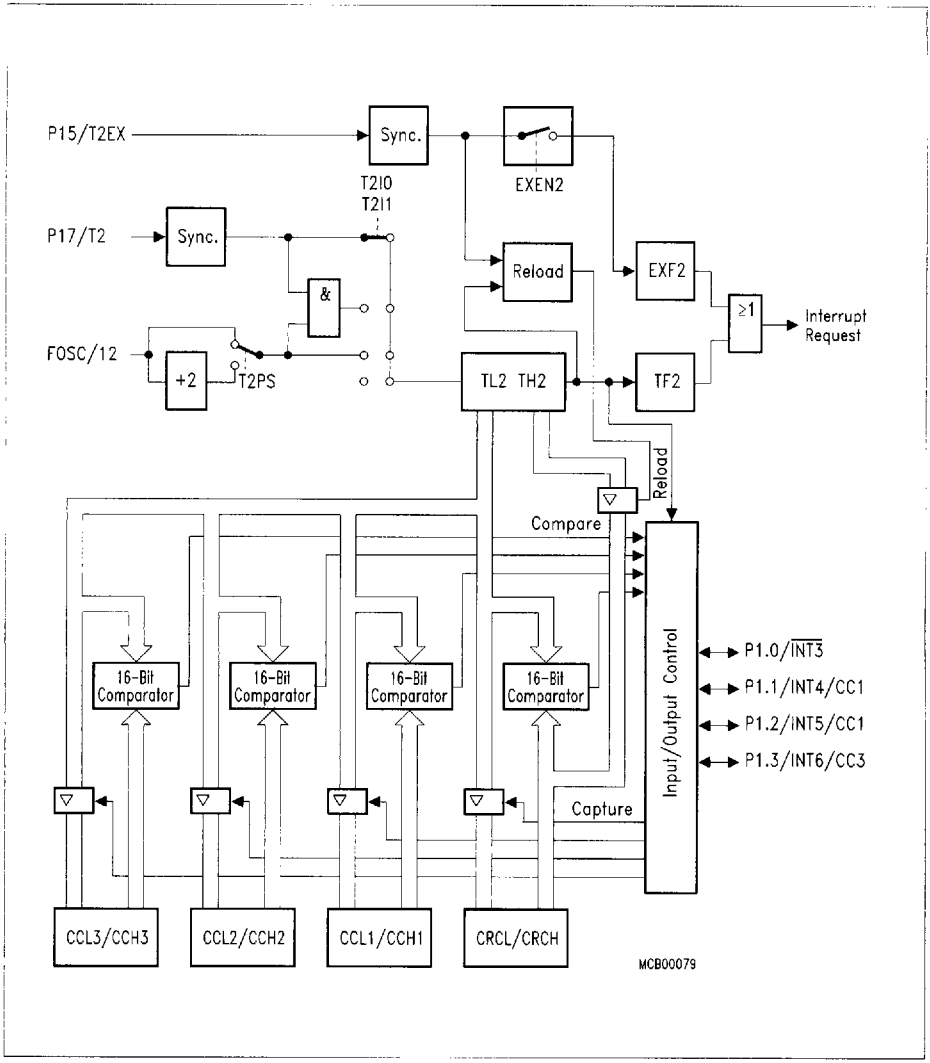


Figure 4
Block Diagram of Timer/Counter 2

8235605 0082097 0TT

Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 3
Interrupt Sources and Vectors

Source (Request Flags)	Vector Address	Vector
IE0	0003_H	External interrupt 0
TF0	$000B_H$	Timer 0 interrupt
IE1	0013_H	External interrupt 1
TF1	$001B_H$	Timer 1 interrupt
RI + TI	0023_H	Serial port interrupt
TF2 + EXF2	$002B_H$	Timer 2 interrupt
IADC	0043_H	A/D converter interrupt
IEX2	$004B_H$	External interrupt 2
IEX3	0053_H	External interrupt 3
IEX4	$005B_H$	External interrupt 4
IEX5	0063_H	External interrupt 5
IEX6	$006B_H$	External interrupt 6

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

8235605 0082098 T36

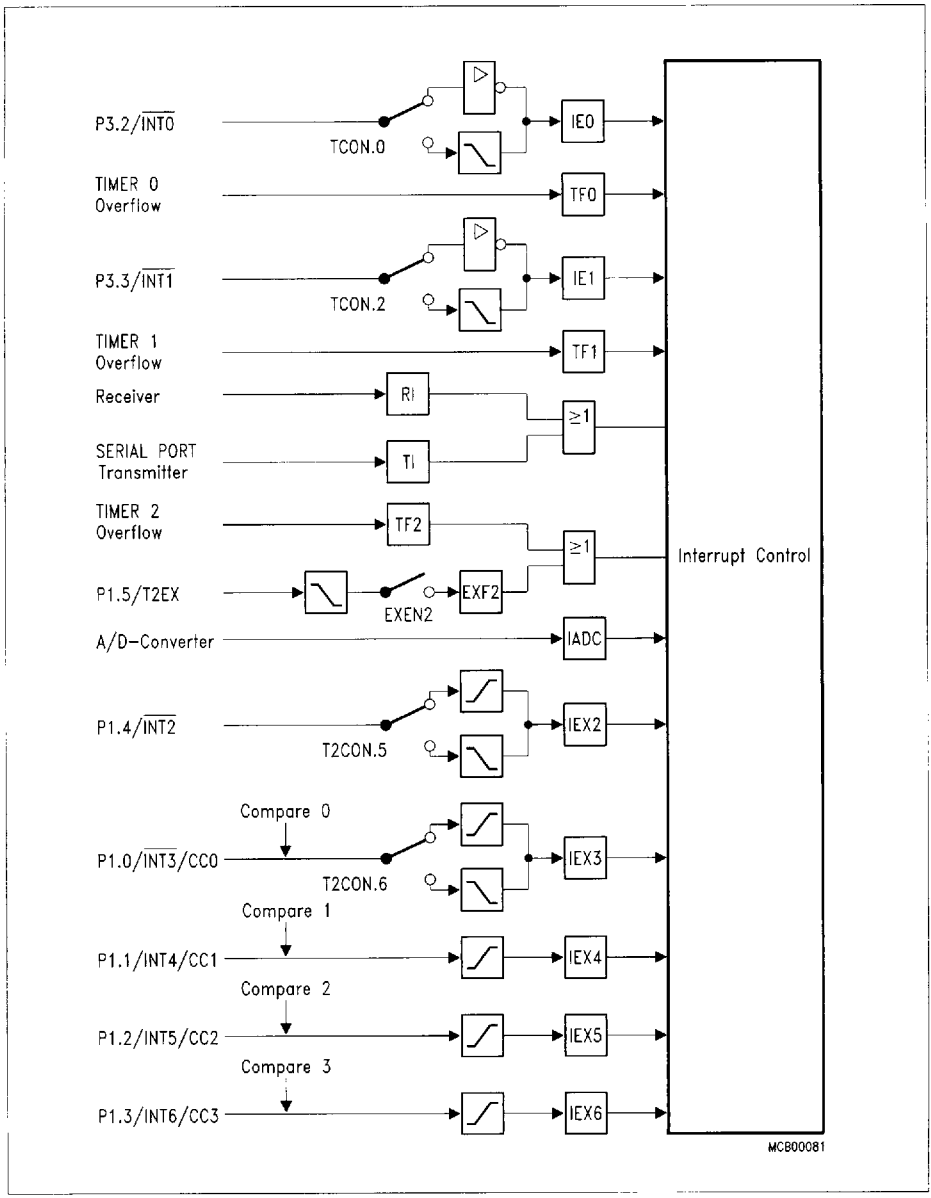


Figure 5
Interrupt Request Sources

8235605 0082099 972

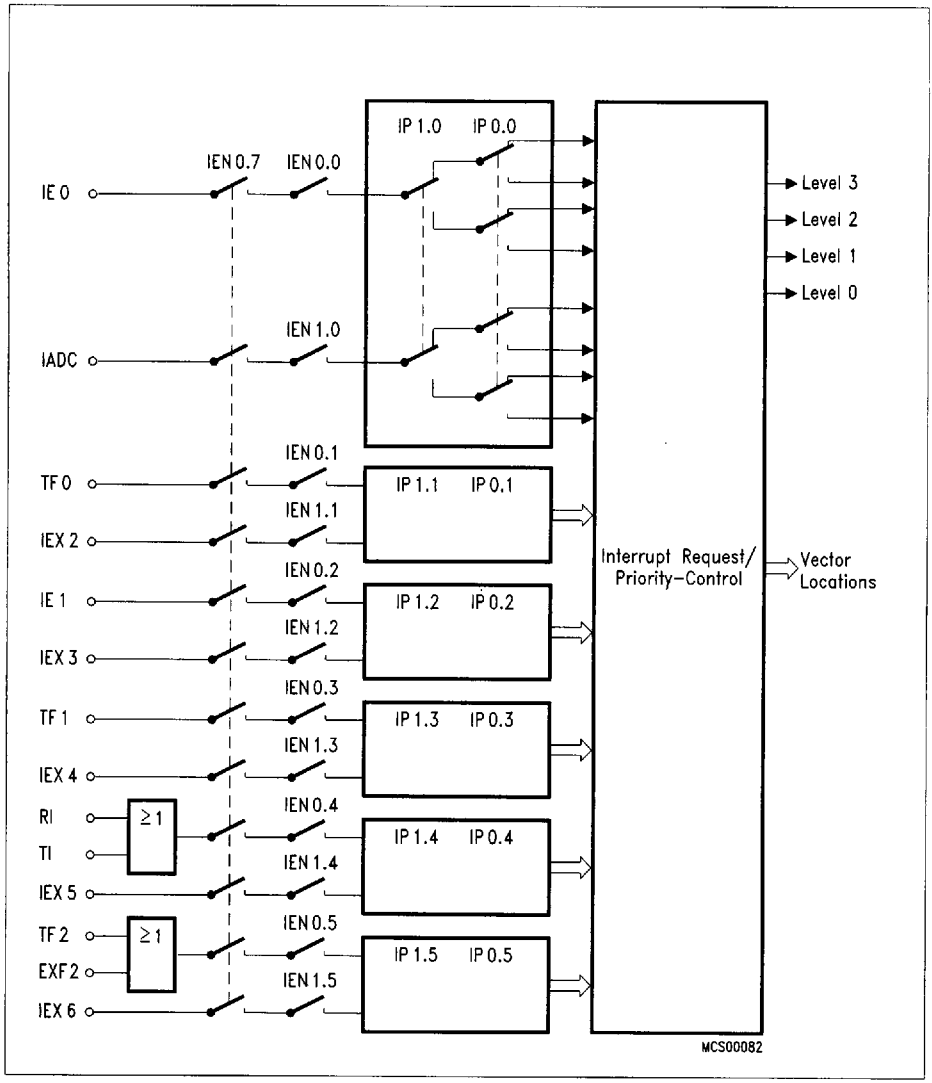


Figure 6
Priority Level Structure

8235605 0082100 414

I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	$\overline{\text{INT6}}$/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0-AN7 is used for analog input signals to the A/D converter.

8235605 0082101 350

Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

The SAB 80515/80535 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-B6599 - X - X - 7600

8235605 0082102 297

Absolute Maximum Ratings

Ambient temperature under bias
SAB 80515/80535 ..... 0 to 70 °C
SAB 80515/80535-T40/85 ..... – 40 to 85 °C
Storage temperature ..... – 65 to 150 °C
Voltage on any pins with respect to ground (V_{SS}) ..... – 0.5 V to 7 V
Power dissipation ..... 2 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB 80515/80535
T_A = – 40 to 85 °C for the SAB 80515/80535-T40/85
T_A = – 40 to110 °C for the SAB 80515/80535-T40/110

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage) (except $\overline{\text{RESET}}$, XTAL2	V_{IH}	2.0	V_{CC} – 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
Input high voltage to $\overline{\text{RESET}}$	V_{IH2}	3.0	–	V	–
Power down voltage	V_{PD}	3	5.5	V	V_{CC} = 0 V
Output low voltage ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA[1)]
Output low voltage port 0, ALE, $\overline{\text{PSEN}}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1)]
Output high voltage ports 1, 2, 3, 4, 5	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
Output high voltage port 0, ALE, $\overline{\text{PSEN}}$	V_{OH1}	2.4	–	V	I_{OH} = – 400 µA

[1)] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1,3,4,5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

8235605 0082103 123

DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Logic 0 input current ports 1, 2, 3, 4, 5	I_{IL}	–	– 800	µA	V_{IL} = 0.45 V
Logic 0 input current XTAL2	I_{IL2}	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
Input low current to $\overline{\text{RESET}}$ for reset	I_{IL3}	–	– 500	µA	V_{IL} = 0.45 V
Input leakage current to port 0, $\overline{\text{EA}}$ AN0 - AN7	I_{LI}	–	± 10	µA	0 V < V_{IN} < V_{CC}
Power supply current:[1] SAB 80515/80535 SAB 80515/80535-T40/85 SAB 80515/80535-T40/110	 I_{CC} I_{CC} I_{CC}	 – – –	 210 230 230	 mA mA mA	 all outputs disconnected
Power-down current	I_{PD}	–	3	mA	V_{CC} = 0 V
Capacitance of I/O buffer	C_{IO}	–	10	pF	f_C =1 MHz

[1] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1,3,4,5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

8235605 0082104 06T

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to + 70 °C for SAB 80515/80535
T_A = – 40 to + 85 °C for SAB 80515/80535 - T40/85

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND}- 0.2	–	V_{AREF}+ 0.2	V	–
Analog input capacitance	C_I	–	25	–	pF	1)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	5 t_{CY}	µs	–
Conversion time (including sample time)	t_C	–	–	13 t_{CY}	µs	–
Differential non-linearity Integral non-linearity Offset error Gain error Total unadjusted error	DNLE INLE TUE	–	± 1/2 ± 1/2 ± 1/2 ± 1/2 ± 1	± 1 ± 1 ± 1 ± 1 ± 2	LSB LSB LSB LSB LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS} 2)
V_{AREF} supply current	I_{REF}	–	–	5	mA	2)
Internal reference error	$V_{IntREFER}$	–	± 5	± 30	mV	2)

1) The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I)during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

8235605 0082105 TT6

AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; (C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF) T_A = 0 to + 70 °C; for SAB 80515/80535
T_A = – 40 to + 85 °C; for SAB 80515/80535 - 40/85

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min	max.	min.	max.	
Program Memory Characteristics						
Cycle Time	t_{CY}	1000	–	12 t_{CLCL}	–	ns
ALE pulse width	t_{LHLL}	127	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	53	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX1}	48	–	t_{CLCL} – 35	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	4 t_{CLCL} – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215		3 t_{CLCL} – 35	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	150	–	3 t_{CLCL} –100	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	t_{CLCL} – 8	–	ns
Address to valid instruction in	t_{AVIV}	–	302	–	5 t_{CLCL} – 115	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

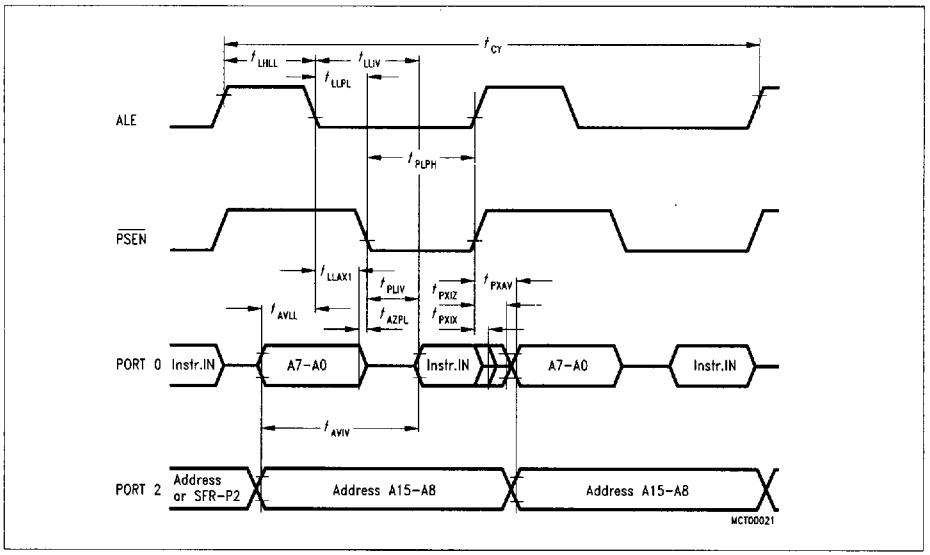
*) Interfacing the SAB 805156 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

8235605 0082106 932

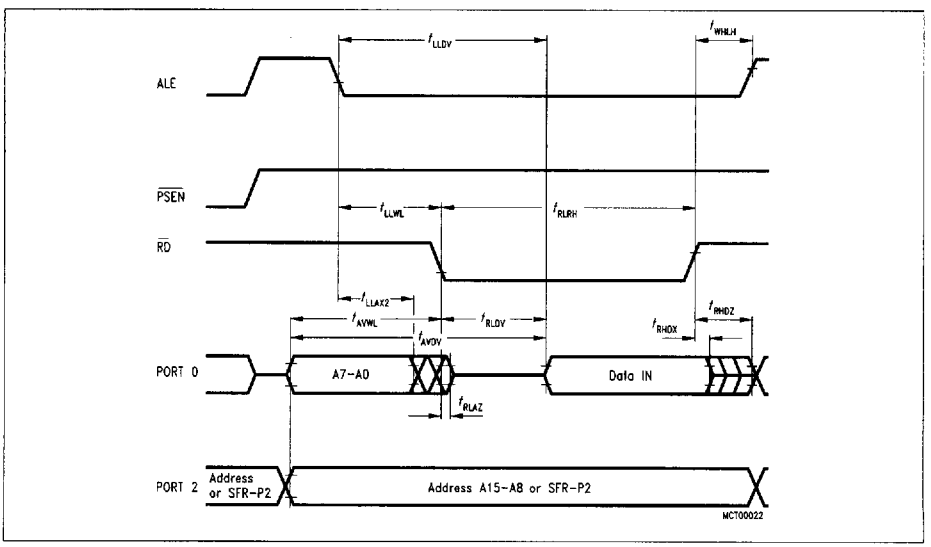
Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min	max.	min.	max.	
External Data Memory Characteristics						
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6\,t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6\,t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2\,t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5\,t_{CLCL} - 165$	ns
DATA hold after $\overline{RD}$	t_{RHDX}	0	–	0		ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2\,t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8\,t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9\,t_{nCLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3\,t_{CLCL} - 50$	$3\,t_{CLCL} + 50$	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4\,_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7\,t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

8235605 0082107 879

Waveforms



Program Memory Read Cycle



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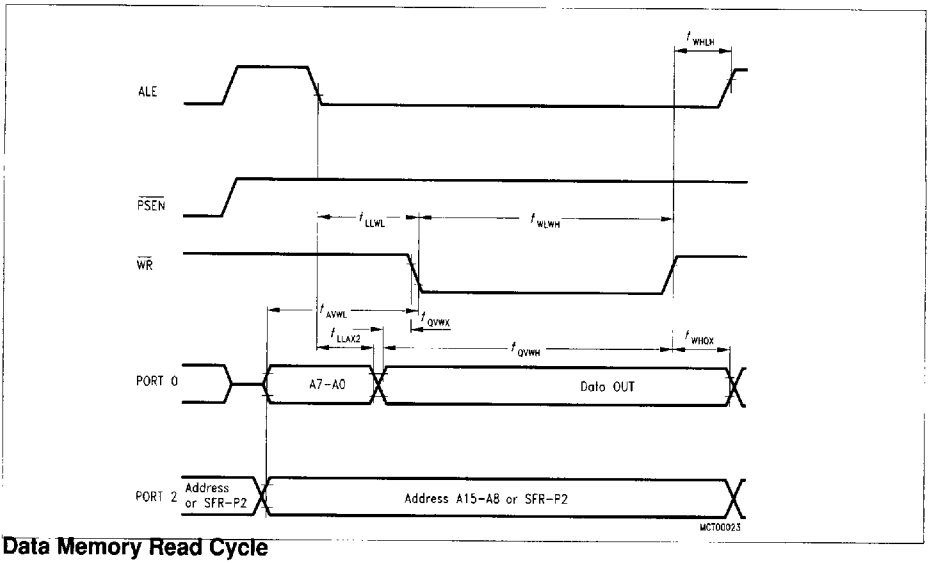
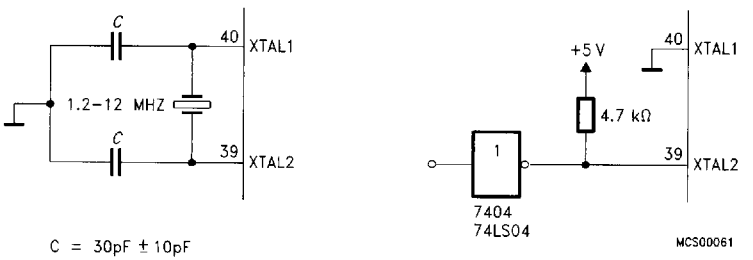


Data Memory Read Cycle



Crystal Oscillator Mode

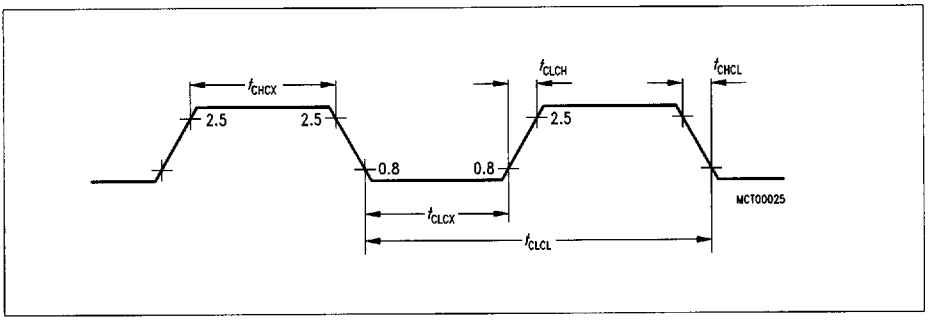
Driving from External Source

Recommended Oscillator Circuits

8235605 0082109 641

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit
		Variable clock Frequ. = 1.2 MHz to 12 MHz		
		min.	max.	
External Clock Drive XTAL2				
Oscillator period	t_{CLCL}	83.3	833.3	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns
Oscillator period	t_{CLCL}	83.3	833.3	ns



External Clock Cycle

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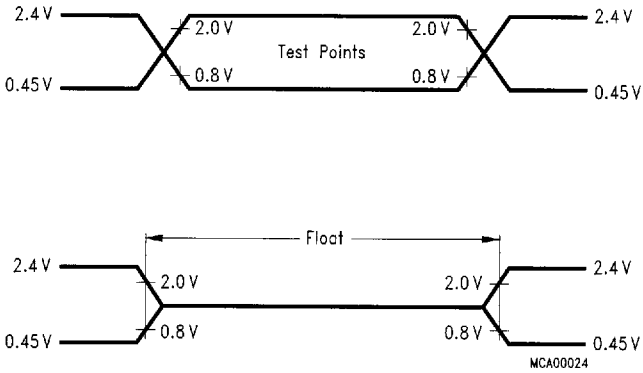


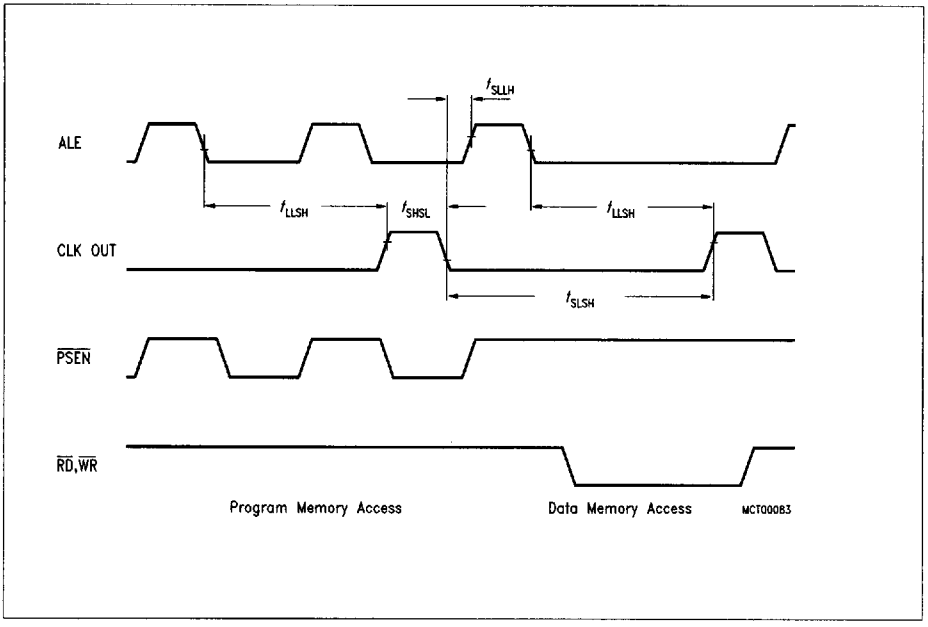
A.C. testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

A.C. Testing Input, Output, Float Waveforms

8235605 0082111 2TT

AC Characteristics (cont'd)

Parameter	Symbol	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
ALE to CLKOUT	t_{LLSH}	543	–	$7\ t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2\ t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10\ t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns



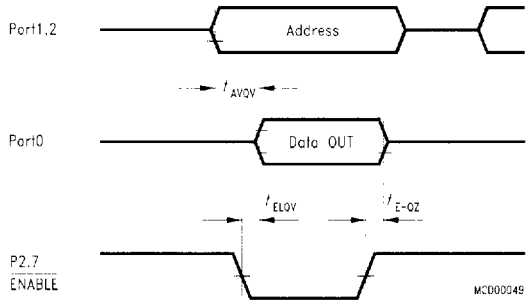
System Clock Timing

8235605 0082112 136

ROM Verification Characteristics

$T_A = 25\ ^\circ C \pm 5\ ^\circ C$; $V_{CC} = 5\ V \pm 10\ \%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit values		Unit
		min	max.	
ROM Verification				
Address to valid data	t_{AVQV}	–	48 t_{CLCL1}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL1}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL1}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: Port 0 =D0–D7

Inputs: P2.5–P2.6, $\overline{PSEN}$=V_{SS}
ALE, $\overline{EA}$= V_{IH}
RESET = V_{IL}

Address: P1.0-P1.7 = A0-A7
P2.0-P2.4 = A8-A12

Data: Port 0 = D0-D7

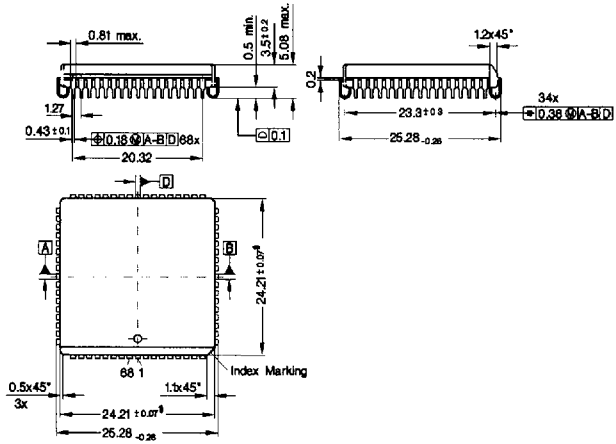
Inputs: P2.5-P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

ROM Verification

8235605 0082113 072

Package Outlines

Plastic Package, P-LCC-68 – SMD
(Plastic Leaded Chip-Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

8235605 0082114 T09