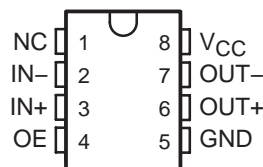- **Operates From a Single 5-V Supply**
- **0-V to 5.5-V Common-Mode Input Voltage Range**
- **Self-Biased Inputs**
- **Complementary 3-State Outputs**
- **Enable Capability**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 25 ns Typ**

D, P, PS, OR PW PACKAGE
(TOP VIEW)

```
        _____
NC  [ 1      8 ] V_CC
IN− [ 2      7 ] OUT−
IN+ [ 3      6 ] OUT+
OE  [ 4      5 ] GND
```

NC – No internal connection
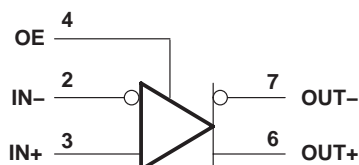
description/ordering information

The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable (OE) is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL712CP	TL712CP
	SOIC (D)	Tube of 75	TL712CD	TL712C
		Reel of 2500	TL712CDR	
	SOP (PS)	Reel of 2000	TL712CPSR	T712
	TSSOP (PW)	Tube of 150	TL712CPW	T712
		Reel of 2000	TL712CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (positive logic)

```
OE   4
         ┌───
IN−  2   │\     7
     ──○─┤  \────── OUT−
IN+  3   │   \  6
     ────┤    \──── OUT+
         │    /
         │   /
          \ /
```

TEXAS INSTRUMENTS

schematics of inputs and outputs

EQUIVALENT OF EACH DIFFERENTIAL INPUT	EQUIVALENT OF EACH ENABLE INPUT	TYPICAL OF ALL OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 7 V
Differential input voltage, V_{ID} (see Note 2) .... $\pm$25 V
Input voltage, V_I, any differential input .... $\pm$25 V
Output enable voltage .... 7 V
Low-level output current, I_{OL} .... 50 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package .... 97°C/W
P package .... 85°C/W
PS package .... 95°C/W
PW package .... 149°C/W
Operating virtual junction temperature, T_J .... 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltage values are at IN+ with respect to IN–.
3. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IC}	Common-mode input voltage	0		5.5	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics at V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	V_{ICR} = 0 to 5 V		−100†		100	mV
V_{hys}	Hysteresis (V_{T+} − V_{T-})				5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	I_{OH} = −1 mA	2.7	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 16 mA		0.4	0.5	V
I_{OZ}	Off-state output current	V_O = 2.4 V				−20	µA
I_I	Enable current	V_I = 5.5 V				100	µA
I_{IH}	High-level enable current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable current	V_{IL} = 0.4 V				−360	µA
r_i	Differential input resistance			4			kΩ
r_o	Output resistance					100	Ω
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current	V_{ID} = 0,	No load		17	20	mA

† The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

## switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TTL load, See Note 5 and Figure 1	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output		25	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total) and is the interval between the input step function and the instant when the output crosses 2.5 V.

PARAMETER MEASUREMENT INFORMATION
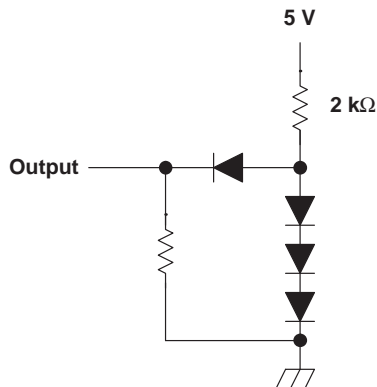
NOTE A: All diodes are 1N4148 or equivalent.

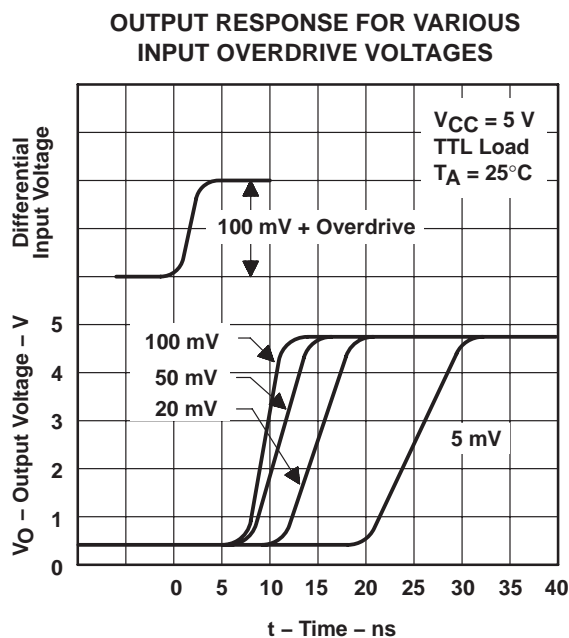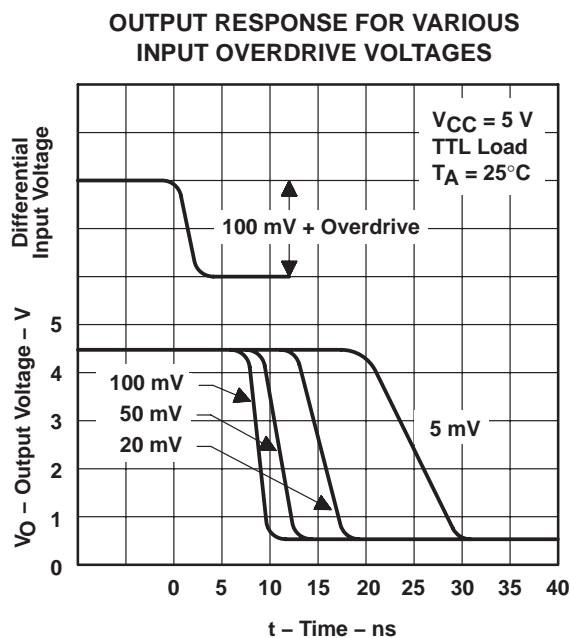**Figure 1. TTL Output Load Circuit**

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVE VOLTAGES

Figure 2

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVE VOLTAGES

Figure 3

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TYPICAL CHARACTERISTICS

**COMMON-MODE
PULSE RESPONSE**
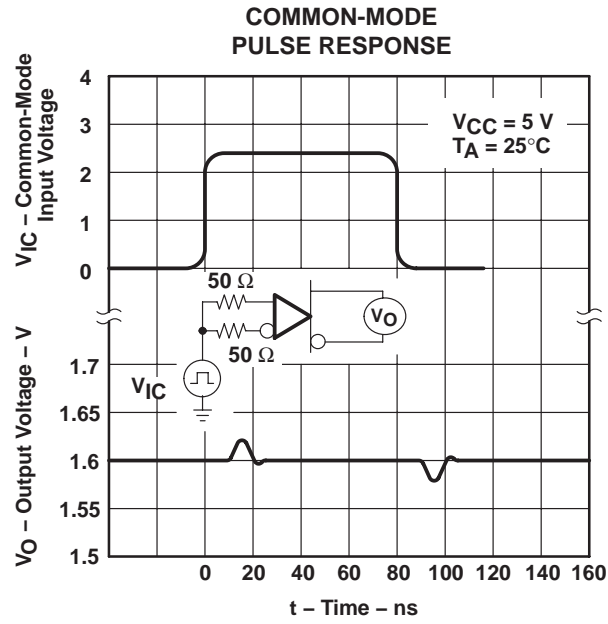
Figure 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL712CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL712C	Samples
TL712CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL712C	Samples
TL712CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL712C	Samples
TL712CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL712C	Samples
TL712CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL712C	Samples
TL712CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL712C	Samples
TL712CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL712CP	Samples
TL712CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL712CP	Samples
TL712CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T712	Samples
TL712CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T712	Samples
TL712CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T712	Samples
TL712CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T712	Samples
TL712CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T712	Samples
TL712CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T712	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL712CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL712CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL712CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
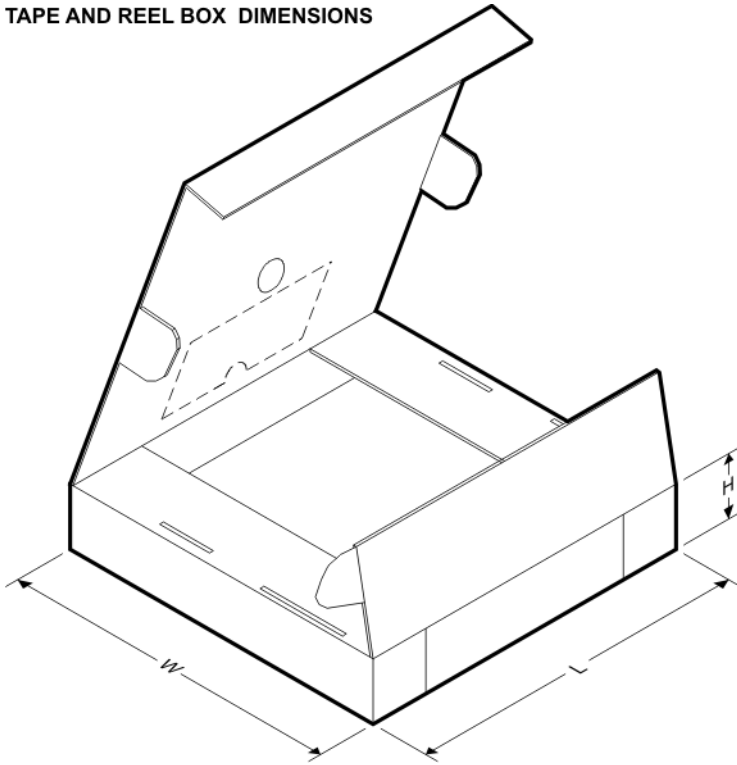
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL712CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL712CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL712CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE
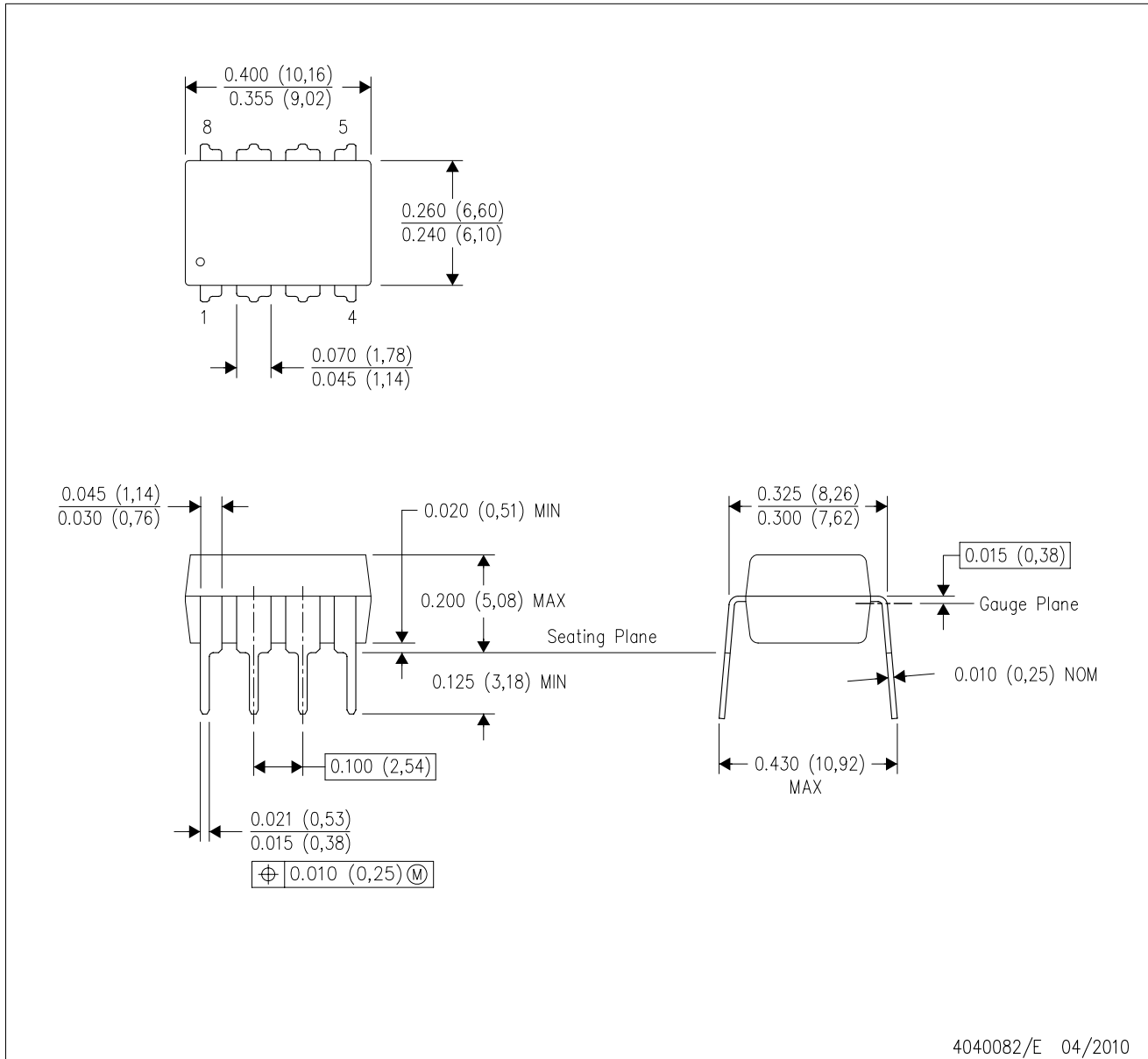
0.400 (10,16)
─────────────
0.355 (9,02)

8   5

0.260 (6,60)
─────────────
0.240 (6,10)

1   4

0.070 (1,78)
─────────────
0.045 (1,14)

0.045 (1,14)
─────────────
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
─────────────
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

Gauge Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92)
MAX

0.021 (0,53)
─────────────
0.015 (0,38)

⌖ | 0.010 (0,25) Ⓜ

4040082/E   04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE
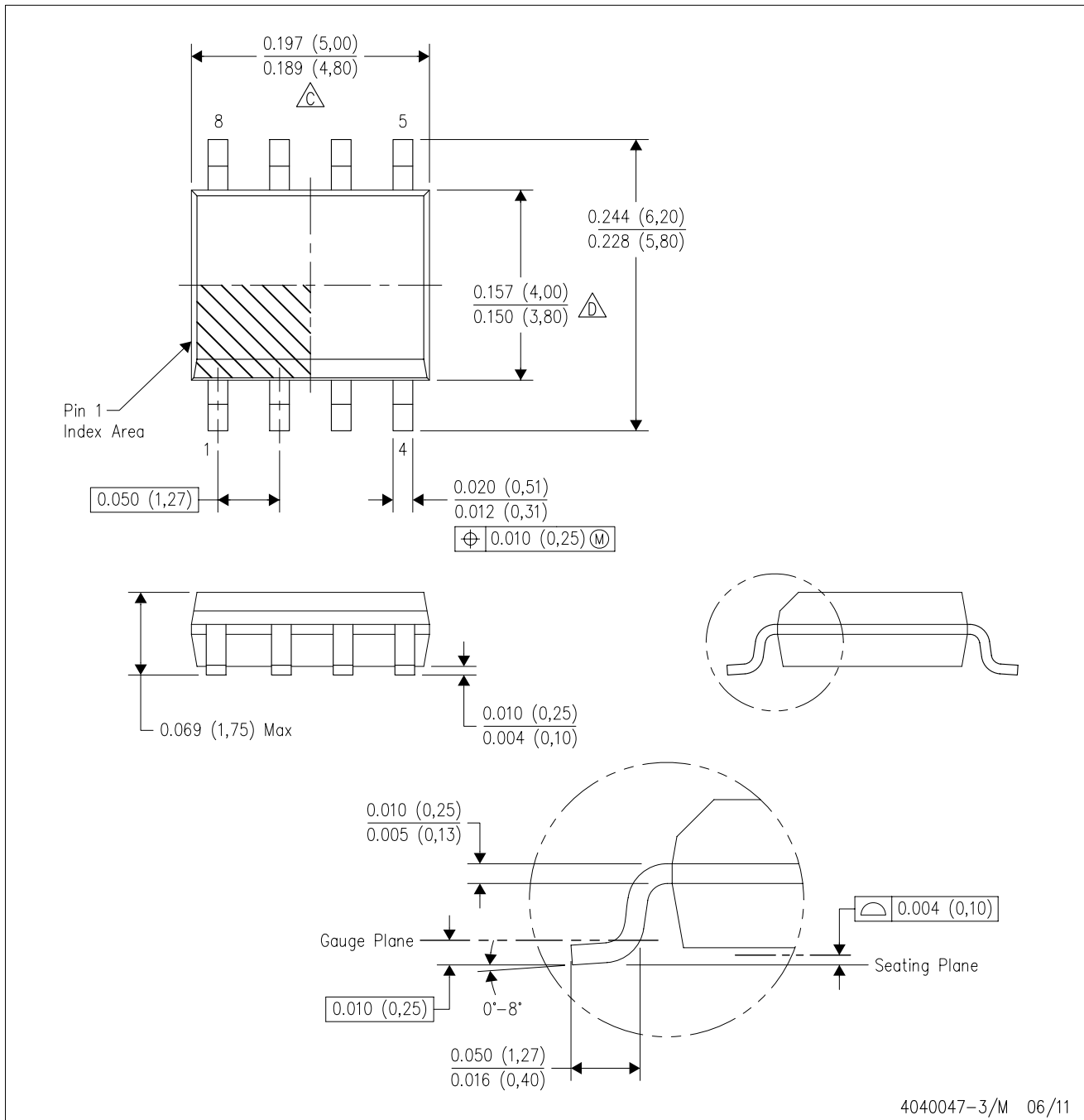
0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
        △C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
        △D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.
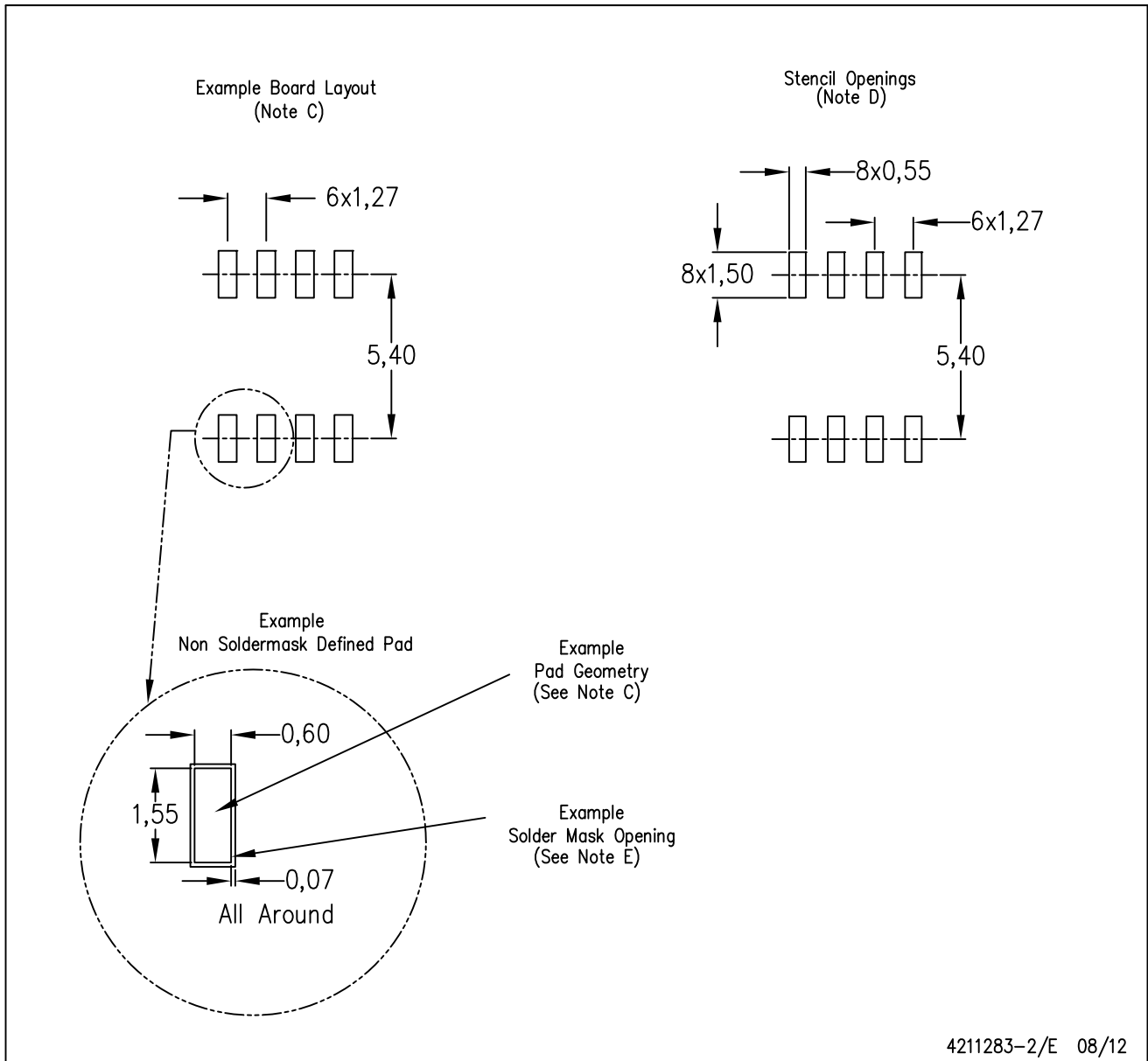
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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

8x1,50

6x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE
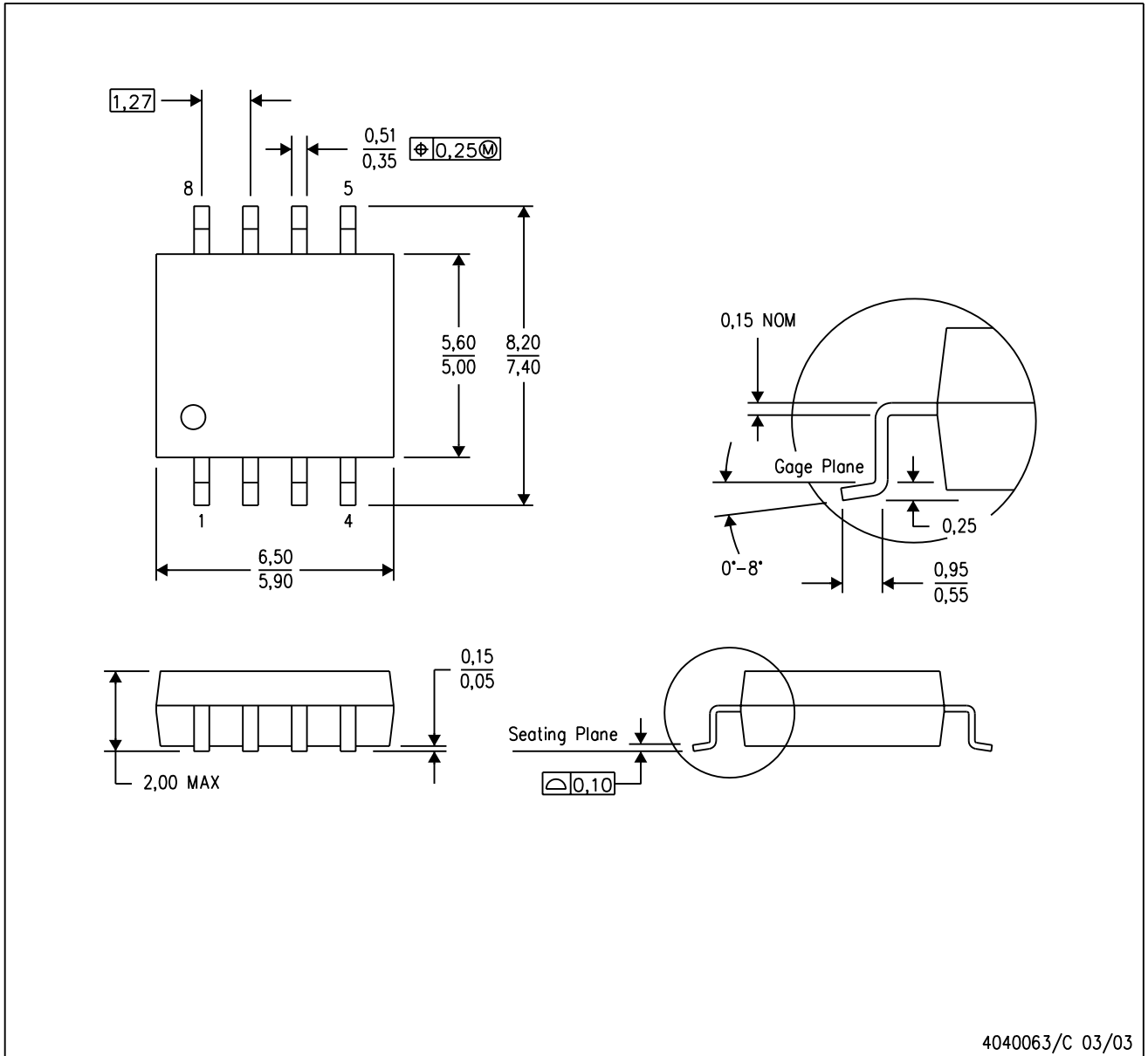
4040063/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R−PDSO−G8)   PLASTIC SMALL OUTLINE
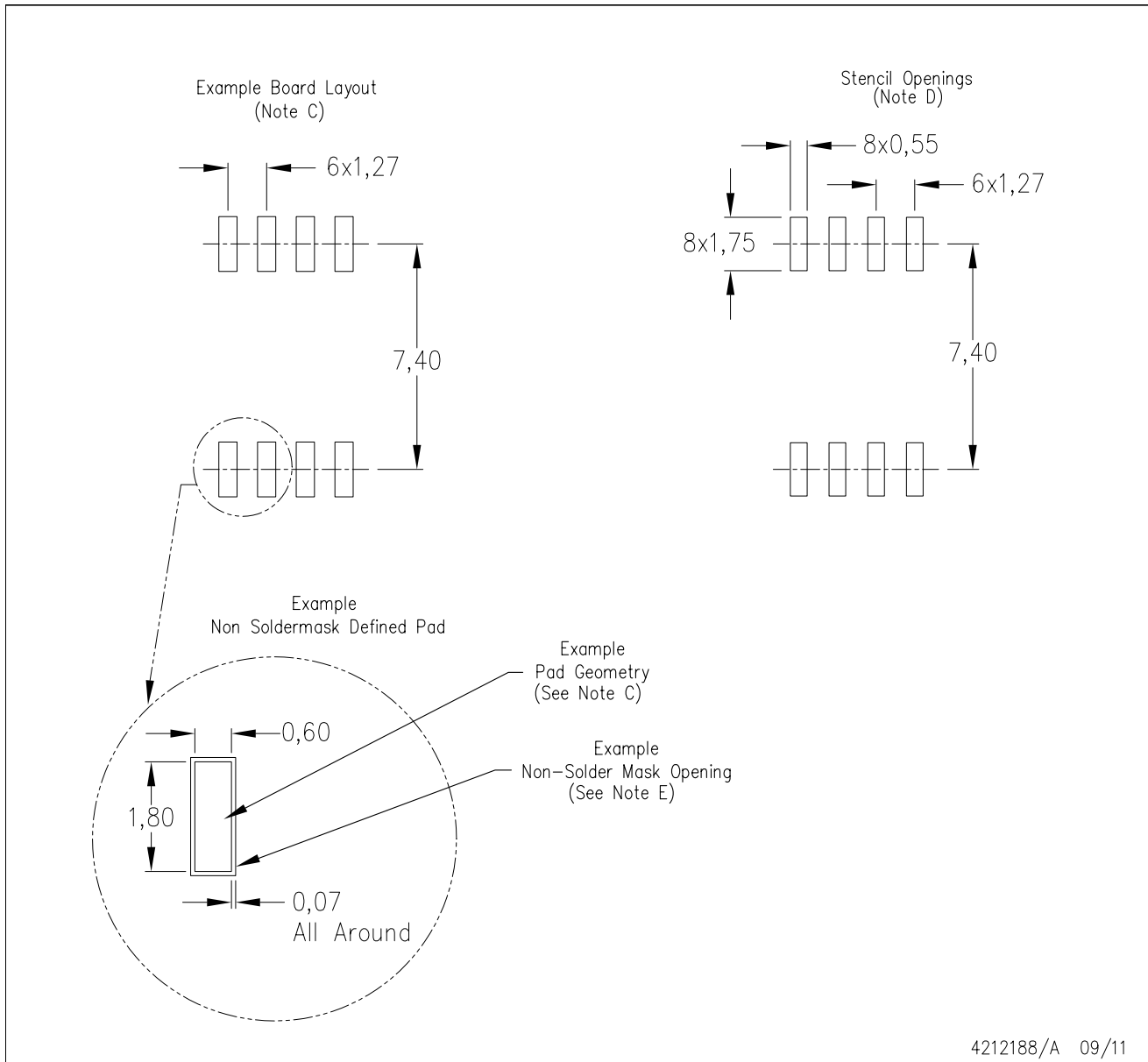
Example Board Layout
(Note C)

6x1,27

7,40

Stencil Openings
(Note D)

8x0,55

6x1,27

8x1,75

7,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Non−Solder Mask Opening
(See Note E)

0,60

1,80

0,07
All Around

4212188/A   09/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
           contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PW (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 | Ⓜ

8   5

△D 4,50
     4,30

6,60
6,20

1   4

3,10
2,90

△C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◻ | 0,10
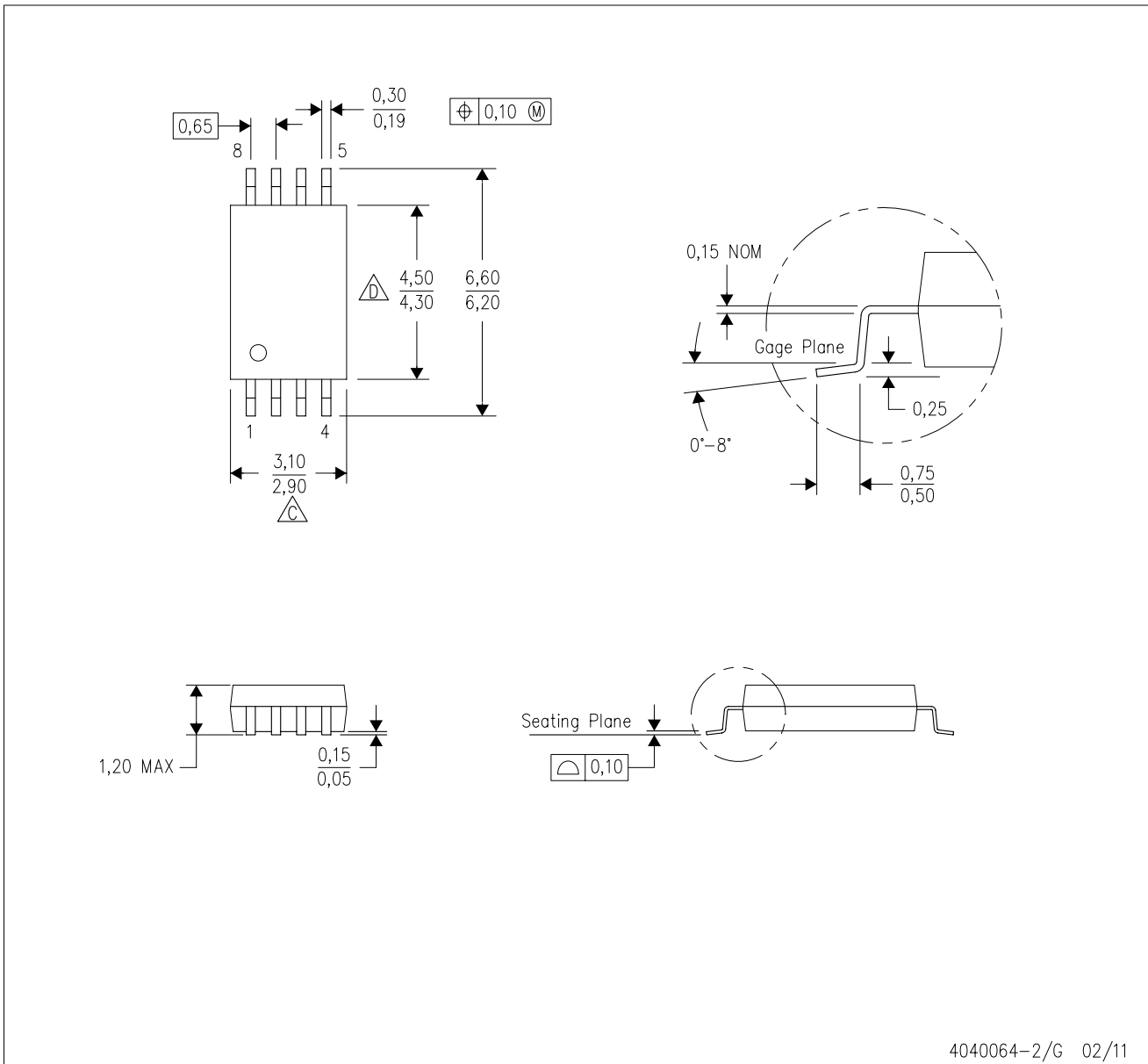
4040064−2/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         △D   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

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