FAIRCHILD
A Schlumberger Company

F3528L
2048 x 8 Static RAM

Preliminary Data Sheet

MOS Memory Products

Description

The F3528L is a 16,384-bit static Random Access Memory (RAM) organized as 2048 words of eight bits each. Since the operation of the F3528L is entirely static, no clocks or refresh are required. This device operates from a single +5V supply and is directly TTL compatible at all inputs and outputs, including the eight bidirectional data DQ pins. The F3528L has an automatic power down feature controlled by the Chip Enable function ($\overline{E}$ = active LOW). When not enabled, the F3528L is in standby mode; this reduces power dissipation by as much as 75% with no degradation of access time.

The F3528L is designed for memory applications where static operation, low cost, large bit-capacity and simple interfacing are important design considerations. It is manufactured using Fairchild's high performance, scaled NMOS technology, Isoplanar-H™. State-of-the-art design and process techniques ensure high density, lower power dissipation and excellent speed performance.

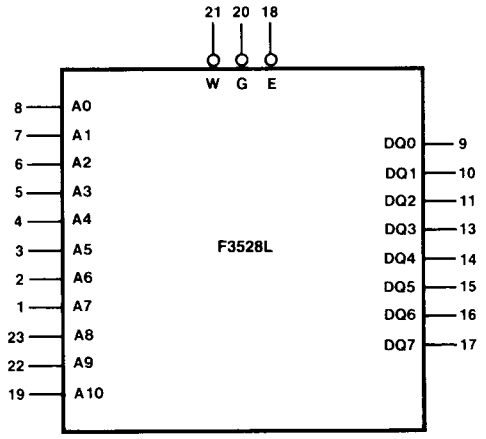
The F3528L is available in a standard 24-pin dual in-line package in a configuration that is pin and function compatible with industry standard EPROMS.

- **2048 x 8-BIT ORGANIZATION**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **SINGLE +5V SUPPLY**
- **AUTOMATIC POWER DOWN WHEN CHIP NOT ENABLED ($\overline{E}$)**
- **ACCESS TIME—100ns, 120ns, 150ns, 200ns**
- **LOW POWER DISSIPATION 330 mW ACTIVE (MAX) 66 mW STANDBY (MAX)**
- **TOTALLY TTL COMPATIBLE WITH SIMPLE BUS CONTROL**
- **COMMON DATA I/O BUS WITH 3-STATE CAPABILITY**
- **JEDEC STANDARD PINOUT**
- **STANDARD 24-PIN DIP**
- **EPROM COMPATIBLE PINOUT**

Pin Names

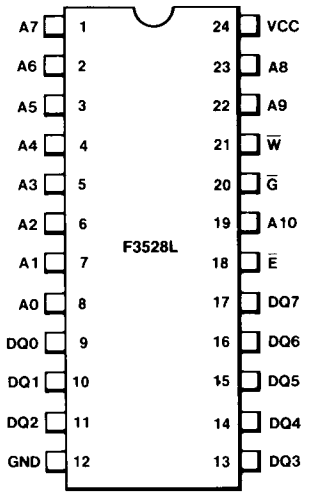
AO-A10	Address Inputs
$\overline{W}$	Write Enable Input
$\overline{G}$	Output Enable Input
$\overline{E}$	Chip Enable Input
DQO-DQ7	Data Inputs/Outputs
VCC	Power (+5V)
GND	Ground (OV)

Logic Symbol



VCC = Pin 24
GND = Pin 12

Connection Diagram
24-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	IT	D
Plastic DIP	IU	P

23 pp 2079

002279

Only FSC

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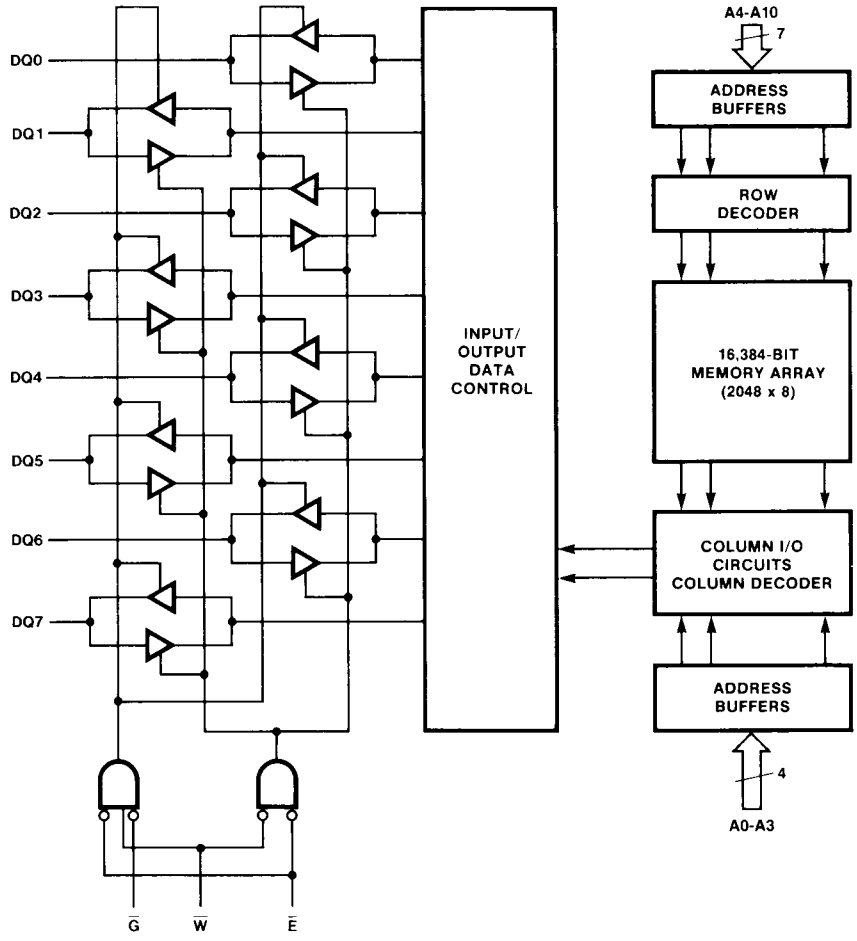
Block Diagram



Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Chip Not Enabled	HIGH Z	Standby
H	L	X	Output Not Enabled	HIGH Z	Active
L	L	H	Read	Data	Active
L	L	L	Write	HIGH Z	Active

Absolute Maximum Ratings

Voltage on any Pin with Respect to GND	−0.5 −7.0 V
V_{CC}, Power Supply Voltage with Respect to GND	−0.5 −7.0 V
Storage Temperature	−55 to 150°C
Operating Temperature	0–70°C
Power Dissipation	1.0 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		$V_{CC}+1.0$	V
V_{IL}	Input LOW Voltage	−0.5		0.8	V

DC Characteristics $T_A = 0\ -70°C, V_{CC} = 5\ V \pm 10\%$

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
I_{IL}	Input Leakage Current				±10	µA	$V_{IN} = 0$ to 5.5 V
I_{OH}	Output HIGH Current		−1.0			mA	$V_O = 2.4$ V
I_{OL}	Output LOW Current		2.1			mA	$V_O = 0.4$ V
V_{OH}	Output HIGH Voltage		2.4			V	$I_{OUT} = -1.0$ mA
V_{OL}	Output LOW Voltage				0.4	V	$I_{OUT} = 2.1$ mA
I_{LO}	Output Leakage Current				±10	µA	$V_{OUT} = 0 - V_{CC}$
I_{SBP}	Peak Power on Current	−10/−12/−15			30	mA	$I_{OUT} = 0$ mA
		−20			45	mA	Note 11
I_{SB}	Standby Current	−10/−12/−15			12	mA	$I_{OUT} = 0$ mA
		−20			12	mA	Note 10
I_{CC}	Operating Current	−10/−12			70	mA	$I_{OUT} = 0$ mA
		−15/−20			60	mA	

Capacitance $T_A = 25°C, f = 1.0$ MHz

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance			5.0	pF	$V_{IN} = 0$ V
C_{OUT}	Output Capacitance			5.0	pF	$V_{OUT} = 0$ V

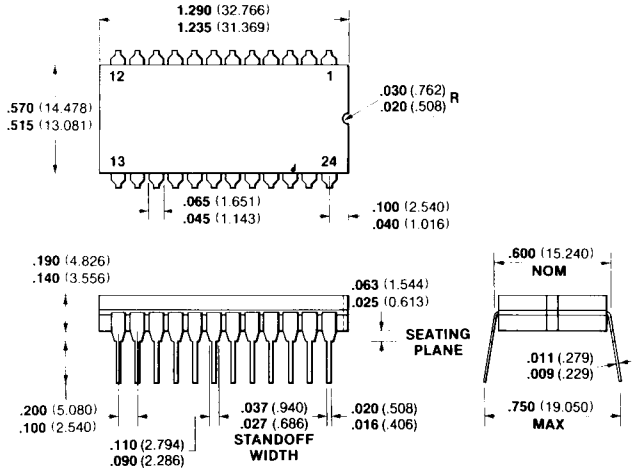
Note
500 µs on time is required from the time V_{CC} reaches 4.5 volts to allow start up of the internal charge pump.

Ordering Information

Part Number	Access Time	Max ICC Current	Package Type	Temp Range	Order Code
F3528L-10	100 ns	70 mA	Ceramic	0° to 70°C	F3528L10DC
F3528L-10	100 ns	70 mA	Plastic	0° to 70°C	F3528L10PC
F3528L-12	120 ns	70 mA	Ceramic	0° to 70°C	F3528L12DC
F3528L-12	120 ns	70 mA	Plastic	0° to 70°C	F3528L12PC
F3528L-15	150 ns	60 mA	Ceramic	0° to 70°C	F3528L15DC
F3528L-15	150 ns	60 mA	Plastic	0° to 70°C	F3528L15PC
F3528L-20	200 ns	60 mA	Ceramic	0° to 70°C	F3528L20DC
F3528L-20	200 ns	60 mA	Plastic	0° to 70°C	F3528L20PC

Package Information

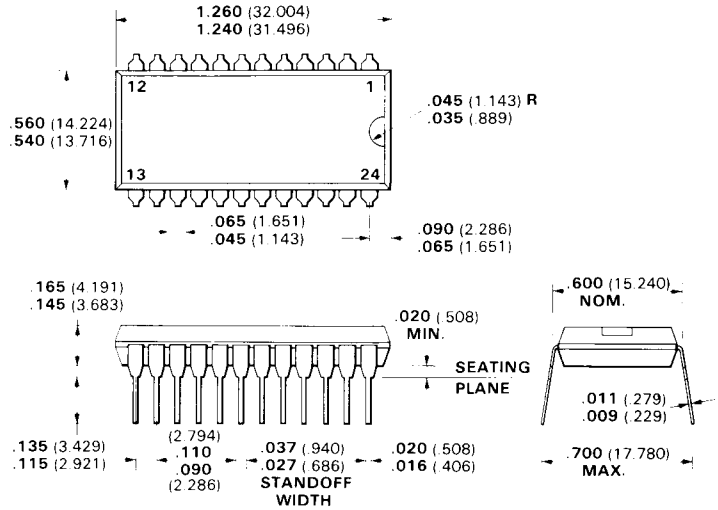
24-Pin Side-brazed Ceramic DIP



IT

Notes
Pins are tin-plated kovar
Package material is alumina
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is .230 x .230 (5.84 x 5.84)
Package weight is 6.5 grams

24-Pin Plastic DIP

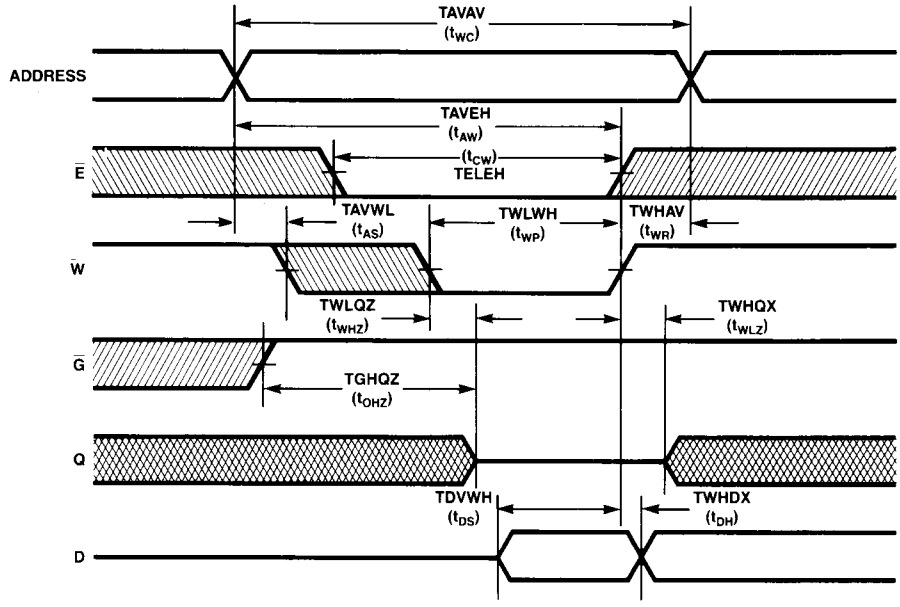


IU

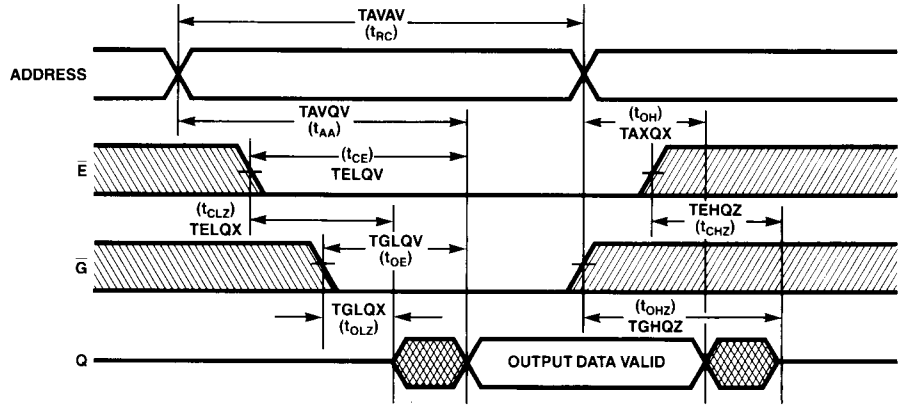
Notes
Pins are tin-plated copper
Package material is plastic
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion

Timing Waveforms

Write Cycle



Read Cycle



AC Characteristic Read Cycle (3, 4, 5, 6, 7) $T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 10\%$

IEEE Symbol	Symbol	Characteristic	F3528L-10		F3528L-12		F3528L-15		F3528L-20		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
TAVAV	t_{RC}	Read Cycle Time	100				150		200		ns	1
TAVQV	t_{AA}	Address Access Time		100		120		150		200	ns	
TELQV	t_{CE}	Chip Select Access Time		100		120		150		200	ns	2
TGLQV	t_{OE}	Output Enable Time		35		40		55		55	ns	
TAXQX	t_{OH}	Output Hold Time from Address Change	10				10		10		ns	
TELQX	t_{CLZ}	Output in LOW Z from $\overline{E}$	10				10		10		ns	12
TEHQZ	t_{CHZ}	Output in HIGH Z from $\overline{E}$		45		50		55		55	ns	
TGLQX	t_{OLZ}	Output in LOW Z from $\overline{G}$	5				5		5		ns	
TGHQZ	t_{OHZ}	Output in HIGH Z from $\overline{G}$		40		45		50		50	ns	
TELICCH	t_{PU}	Chip Selection to Power Up	0		0		0		0		ns	
TEHICCL	t_{PD}	Chip Deselection to Power Down		50				60		60	ns	

AC Characteristic Write Cycle (3, 4, 5, 6, 7) $T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 10\%$

IEEE Symbol	Symbol	Characteristic	F3528L-10		F3528L-12		F3528L-15		F3528L-20		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
TAVAV	t_{WC}	Write Cycle Time	100		120		150		200		ns	8,9
TELEH	t_{CW}	Chip Selection to End of Write	90		110		120		150		ns	
TAVWL	t_{AS}	Address Setup Time	20		20		20		20		ns	
TWLWH	t_{WP}	Write Pulse Width	70		80		100		120		ns	8
TWHAV	t_{WR}	Write Recovery Time	10		10		10		10		ns	
TDVWH	t_{DS}	Data Setup Time	40		50		60		60		ns	
TWHDX	t_{DH}	Data Hold Time	10		10		15		15		ns	
TWHQX	t_{WLZ}	Output in LOW Z from $\overline{W}$	5		5		5		5		ns	
TWLHZ	t_{WHZ}	Output in HIGH Z from $\overline{W}$		40		45		50		50	ns	

Notes

1. A read occurs during the overlap of a LOW $\overline{E}$, a LOW $\overline{G}$, and a HIGH $\overline{W}$.
2. Access from $\overline{E}$ includes power-up time.
3. Timing specifications are valid for $V_{CC} = 5\ V \pm 10\%$, $0°C \leq T_A \leq 70°C$.
4. Input pulse levels: 0.8 V to + 2.2 V.
5. Input rise and fall time: 10 ns.
6. Timing measurements reference level: 1.5 V.
7. Output load: 1 TTL gate and $C_L = 100$ pF.
8. A write cycle occurs during the overlap of a LOW $\overline{E}$ and a LOW $\overline{W}$.
9. $\overline{G}$ may be both HIGH and LOW in a write cycle.
10. Power down occurs some 100 ns after $\overline{E}$ goes HIGH.
11. A power surge can be expected during power up. A pull up resistor from V_{CC} to $\overline{E}$ is needed; otherwise, $I_{SBP} = I_{CC}$.
12. $\overline{G}$ must be LOW during this time.