PRELIMINARY

# CY2275A

# Pentium II™ Clock Synthesizer/Driver for 82440LX Chipset with 3 DIMM Support

## Features

- **Mixed 2.5V and 3.3V operation**
- **Clock solution to meet requirements of Pentium II™ motherboards**
  - **— Four CPU clocks at 2.5V**
  - **— Twelve 3.3V SDRAM clocks**
  - **— Seven synchronous PCI clocks**
  - **— Two 2.5V IOAPIC clocks at 14.318 MHz**
  - **— One 3.3V Ref. clock at 14.318 MHz**
- **1 ns–4 ns CPU-PCI delay, factory-EPROM programmable**
- **I²C™ Serial Configuration Interface**
- **Factory-EPROM programmable output drive and slew rate for optimal EMI control. Improved output drivers are designed for low EMI.**
- **Factory-EPROM programmable CPU clock frequencies for custom configurations**
- **Powerdown, CPU stop and PCI stop pins for power management**
- **Low CPU clock jitter ≤ 250 ps cycle-cycle.**
- **Low skew outputs**
- **Intel Test Mode support**
- **Available in space-saving 48-pin SSOP package**
- **CY2030 generates USB, Audio, I/O and Reference clocks**

## Functional Description

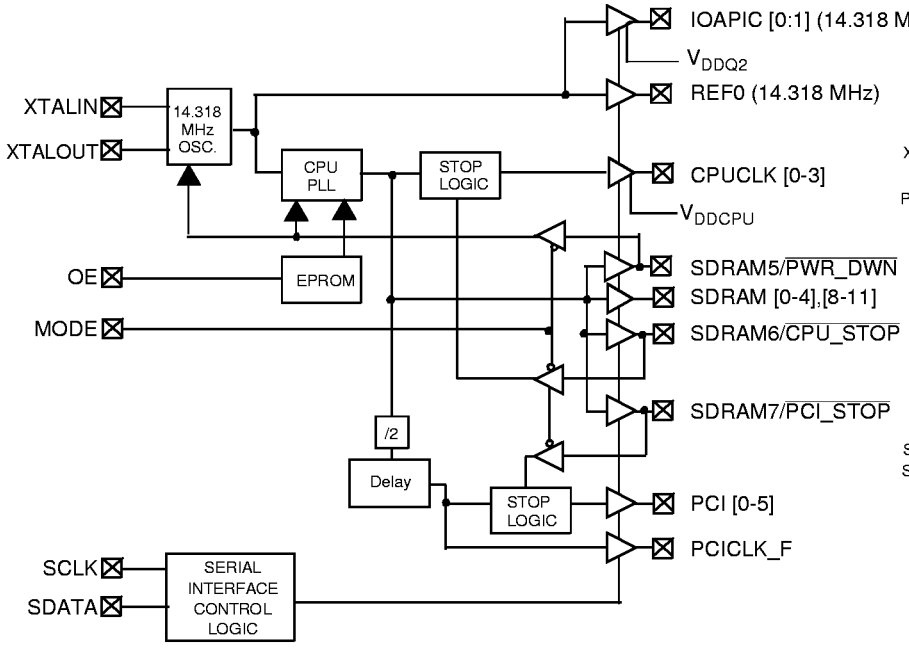
The CY2275A is a Clock Synthesizer/Driver for a Pentium II-based PC using an Intel 82440LX or other core-logic chipset.

The CY2275A outputs four CPU clocks at 2.5V. There are seven PCI clocks, running at one half the CPU clock frequency. One of the PCI clocks is free-running. Additionally, the part outputs twelve 3.3V SDRAM clocks, two 2.5V IOAPIC clocks at 14.318 MHz, and one 3.3V reference clock at 14.318 MHz. All output clocks meet Intel's drive strength, rise/fall time, jitter, accuracy, and skew requirements.

The part has power-down, CPU stop, and PCI stop pins for power management control. These inputs are multiplexed with SDRAM clock outputs, and are selected when the MODE pin is driven LOW. Additionally, these inputs are synchronized on-chip, enabling glitch-free output transitions. When the $\overline{\text{CPU\_STOP}}$ input is asserted, the CPU clock outputs are driven LOW. When the $\overline{\text{PCI\_STOP}}$ input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. Finally, when the $\overline{\text{PWR\_DWN}}$ pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

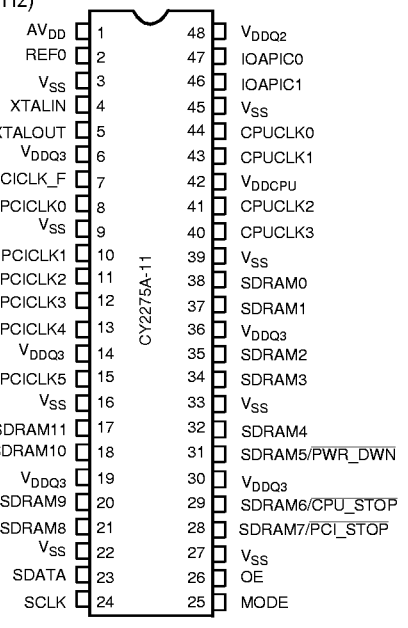
The CY2275A clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2275A to have lower EMI than clock devices from other manufacturers. Additionally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations for EMI control.

## Logic Block Diagram




## Pin Configuration

SSOP
Top View



## Pin Summary

| Name | Pins | Description |
|---|---|---|
| $V_{DDQ3}$ | 6, 14, 19, 30, 36 | 3.3V Digital voltage supply |
| $V_{DDQ2}$ | 48 | IOAPIC Digital voltage supply, 2.5V |
| $V_{DDCPU}$ | 42 | CPU Digital voltage supply, 2.5V |
| $AV_{DD}$ | 1 | Analog voltage supply, 3.3V |
| $V_{SS}$ | 3, 9, 16, 22, 27, 33, 39, 45 | Ground |
| XTALIN[1] | 4 | Reference crystal input |
| XTALOUT[1] | 5 | Reference crystal feedback |
| SDRAM7/ $\overline{\text{PCI\_STOP}}$ | 28 | SDRAM clock output. Also, active LOW control input to stop PCI clocks, enabled when MODE is LOW |
| SDRAM6/ $\overline{\text{CPU\_STOP}}$ | 29 | SDRAM clock output. Also, active LOW control input to stop CPU clocks, enabled when MODE is LOW. |
| SDRAM5/ $\overline{\text{PWR\_DWN}}$ | 31 | SDRAM clock output. Also, active LOW control input to power down device, enabled when MODE is LOW. |
| SDRAM[0:4],[8:11] | 38, 37, 35, 34, 32, 21, 20, 18, 17 | SDRAM clock outputs |
| OE | 26 | Active HIGH Output Enable Input (see table below) |
| CPUCLK[0:3] | 44, 43, 41, 40 | CPU clock outputs |
| PCICLK[0:5] | 8, 10, 11, 12, 13, 15 | PCI clock outputs, at one-half the CPU frequency |
| PCICLK_F | 7 | Free-running PCI clock output |
| IOAPIC[0:1] | 47, 46 | IOAPIC clock output |
| REF0 | 2 | Reference clock outputs, 14.318 MHz, drives 45 pF load |
| SDATA | 23 | Serial data input for serial configuration port |
| SCLK | 24 | Serial clock input for serial configuration port |
| MODE | 25 | Mode Select pin for enabling power management features |

**Note:**
1. For best accuracy, use a parallel-resonant crystal, $C_{LOAD}$ = 18 pF.

## Function Table

| OE | XTALIN | CPUCLK[0:3] SDRAM[0:11] | PCICLK[0:5] PCICLK_F | REF0 IOAPIC[0:1] |
|---|---|---|---|---|
| 0 | 14.318 MHz | Hi-Z | Hi-Z | Hi-Z |
| 1 | 14.318 MHz | 66.67 MHz | 33.33 MHz | 14.318 MHz |

## Actual Clock Frequency Values

| Clock Output | Target Frequency (MHz) | Actual Frequency (MHz) | PPM |
|---|---|---|---|
| CPUCLK | 66.67 | 66.654 | –195 |

## CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

## Power Management Logic - Active when MODE pin is held 'LOW'

| CPU_STOP | PCI_STOP | PWR_DWN | CPUCLK | PCICLK | PCICLK_F | Other Clocks | Osc. | PLLs |
|---|---|---|---|---|---|---|---|---|
| X | X | 0 | Low | Low | Stopped | Stopped | Off | Off |
| 0 | 0 | 1 | Low | Low | Running | Running | Running | Running |
| 0 | 1 | 1 | Low | 33/30 MHz | Running | Running | Running | Running |
| 1 | 0 | 1 | 66/60 MHz | Low | Running | Running | Running | Running |
| 1 | 1 | 1 | 66/60 MHz | 33/30 MHz | Running | Running | Running | Running |

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0".
- $I^2C$ Address for the CY2275 is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | ---- |

## Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)

| Bit | Pin # | Description | |
|---|---|---|---|
| Bit 7 | -- | (Reserved) drive to '0' | |
| Bit 6 | -- | (Reserved) drive to '0' | |
| Bit 5 | -- | (Reserved) drive to '0' | |
| Bit 4 | -- | (Reserved) drive to '0' | |
| Bit 3 | -- | (Reserved) drive to '0' | |
| Bit 2 | -- | (Reserved) drive to '0' | |
| Bit 1<br>Bit 0 | -- | Bit 1<br>1<br>1<br>0<br>0 | Bit 0<br>1 - Three-State<br>0 - N/A<br>1 - Testmode<br>0 - Normal Operation |

## Select Functions

| Functional Description | Outputs | | | | |
|---|---|---|---|---|---|
| | CPU | PCI, PCI_F | SDRAM | Ref | IOAPIC |
| Three-State | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| Test Mode | TCLK/2[2] | TCLK/4 | TCLK/2 | TCLK | TCLK |

**Note:**

2. TCLK supplied on the XTALIN pin in Test Mode.

**Byte 1: CPU Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | N/A | (Reserved) drive to '0' |
| Bit 6 | N/A | (Reserved) drive to '0' |
| Bit 5 | N/A | (Reserved) drive to '0' |
| Bit 4 | N/A | Not used - drive to '0' |
| Bit 3 | 40 | CPUCLK3 (Active/Inactive) |
| Bit 2 | 41 | CPUCLK2 (Active/Inactive) |
| Bit 1 | 43 | CPUCLK1 (Active/Inactive) |
| Bit 0 | 44 | CPUCLK0 (Active/Inactive) |

**Byte 2: PCI Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | -- | (Reserved) drive to '0' |
| Bit 6 | 7 | PCICLK_F (Active/Inactive) |
| Bit 5 | 15 | PCICLK5 (Active/Inactive) |
| Bit 4 | 14 | PCICLK4 (Active/Inactive) |
| Bit 3 | 12 | PCICLK3 (Active/Inactive) |
| Bit 2 | 11 | PCICLK2 (Active/Inactive) |
| Bit 1 | 10 | PCICLK1 (Active/Inactive) |
| Bit 0 | 8 | PCICLK0 (Active/Inactive) |

**Byte 3: SDRAM Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 28 | SDRAM7 (Active/Inactive) |
| Bit 6 | 29 | SDRAM6 (Active/Inactive) |
| Bit 5 | 31 | SDRAM5 (Active/Inactive) |
| Bit 4 | 32 | SDRAM4 (Active/Inactive) |
| Bit 3 | 34 | SDRAM3 (Active/Inactive) |
| Bit 2 | 35 | SDRAM2 (Active/Inactive) |
| Bit 1 | 37 | SDRAM1 (Active/Inactive) |
| Bit 0 | 38 | SDRAM0 (Active/Inactive) |

**Byte 4: SDRAM Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | N/A | Not used - drive to '0' |
| Bit 6 | N/A | Not used - drive to '0' |
| Bit 5 | N/A | Not used - drive to '0' |
| Bit 4 | N/A | Not used - drive to '0' |
| Bit 3 | 17 | SDRAM11 |
| Bit 2 | 18 | SDRAM10 |
| Bit 1 | 20 | SDRAM9 |
| Bit 0 | 21 | SDRAM8 |

**Byte 5: Peripheral Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | N/A | (Reserved) drive to '0' |
| Bit 6 | N/A | (Reserved) drive to '0' |
| Bit 5 | 46 | IOAPIC1 (Active/Inactive) |
| Bit 4 | 47 | IOAPIC0 (Active/Inactive) |
| Bit 3 | N/A | (Reserved) drive to '0' |
| Bit 2 | N/A | (Reserved) drive to '0' |
| Bit 1 | N/A | (Reserved) drive to '0' |
| Bit 0 | 2 | REF0 (Active/Inactive) |

**Byte 6: Reserved, for future use**

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to $V_{DD}$+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation ..... 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

## Operating Conditions[3]

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $AV_{DD}$, $V_{DDQ3}$ | Analog and Digital Supply Voltage | 3.135 | 3.465 | V |
| $V_{DDCPU}$ | CPU Supply Voltage | 2.375 | 2.9 | V |
| $V_{DDQ2}$ | IOAPIC Supply Voltage | 2.375 | 2.9 | V |
| $T_A$ | Operating Temperature, Ambient | 0 | 70 | °C |
| $C_L$ | Max. Capacitive Load on<br>CPUCLK, IOAPIC[0:1]<br>PCICLK, SDRAM<br>REF0 | <br>10<br>30, 20<br>20 | <br>20<br>30<br>45 | pF |
| $f_{(REF)}$ | Reference Frequency, Oscillator Nominal Value | 14.318 | 14.318 | MHz |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level Input Voltage | Except Crystal Inputs | | | 2.0 | | V |
| $V_{IL}$ | Low-level Input Voltage | Except Crystal Inputs | | | | 0.8 | V |
| $V_{OH}$ | High-level Output Voltage | $V_{DDCPU}$ = $V_{DDQ2}$ = 2.375V | $I_{OH}$ = 16 mA | CPUCLK | 2.0 | | V |
| | | | $I_{OH}$ = 18 mA | IOAPIC | | | |
| $V_{OL}$ | Low-level Output Voltage | $V_{DDCPU}$ = $V_{DDQ2}$ = 2.375V | $I_{OL}$ = 27 mA | CPUCLK | | 0.4 | V |
| | | | $I_{OL}$ = 29 mA | IOAPIC | | | |
| $V_{OH}$ | High-level Output Voltage | $V_{DDQ3}$, $AV_{DD}$ = 3.135V | $I_{OH}$ = 36 mA | SDRAM | 2.4 | | V |
| | | | $I_{OH}$ = 32 mA | PCICLK | | | |
| | | | $I_{OH}$ = 36 mA | REF0 | | | |
| $V_{OL}$ | Low-level Output Voltage | $V_{DDQ3}$, $AV_{DD}$ = 3.135V | $I_{OL}$ = 29 mA | SDRAM | | 0.4V | V |
| | | | $I_{OL}$ = 26 mA | PCICLK | | | |
| | | | $I_{OL}$ = 29 mA | REF0 | | | |
| $I_{IH}$ | Input High Current | $V_{IH}$ = $V_{DD}$ | | | –5 | +5 | µA |
| $I_{IL}$ | Input Low Current | $V_{IL}$ = 0V | | | | 5 | µA |
| $I_{OZ}$ | Output Leakage Current | Three-state | | | –10 | +10 | µA |
| $I_{DD}$ | Power Supply Current[4] | $V_{DD}$ = 3.465V, $V_{IN}$ = 0 or $V_{DD}$, Loaded Outputs, CPU clocks = 66.67 MHz | | | | 300 | mA |
| $I_{DD}$ | Power Supply Current[4] | $V_{DD}$ = 3.465V, $V_{IN}$ = 0 or $V_{DD}$, Unloaded Outputs | | | | 120 | mA |
| $I_{DDS}$ | Power-down Current | Current draw in power-down state | | | | 50 | µA |

**Notes:**

3. Electrical parameters are guaranteed with these operating conditions.
4. Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: TBD

## Switching Characteristics[5]

| Parameter | Output | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_1$ | All | Output Duty Cycle[6] | $t_1 = t_{1A} \div t_{1B}$ | 45 | 50 | 55 | % |
| $t_{1C}$ | CPUCLK | CPU Clock HIGH Time | Above 2.0V, 66.6 MHz, $V_{DDCPU}$ = 2.5V<br>Above 2.0V, 60.0 MHz, $V_{DDCPU}$ = 2.5V | 5.2<br>6.0 | | | ns |
| $t_{1C}$ | PCICLK | PCI Clock HIGH Time | Above 2.4V, 33.3 MHz<br>Above 2.4V, 30.0 MHz | 12.0<br>13.3 | | | ns |
| $t_{1D}$ | CPUCLK | CPU Clock LOW Time | Below 0.4V, 66.6 MHz, $V_{DDCPU}$ = 2.5V<br>Below 0.4V, 60.0 MHz, $V_{DDCPU}$ = 2.5V | 5.0<br>5.8 | | | ns |
| $t_{1D}$ | PCICLK | PCI Clock LOW Time | Below 0.4V, 33.3 MHz<br>Below 0.4V, 30.0 MHz | 12.0<br>13.3 | | | ns |
| $t_2$ | CPUCLK, IOAPIC | CPU and IOAPIC Clock Rising and Falling Edge Rate | Between 0.4V and 2.0V | 1.0 | | 4.0 | V/ns |
| $t_2$ | PCICLK, REF0 | PCI, REF0 Clock Rising and Falling Edge Rate | Between 0.4V and 2.4V | 1.0 | | 4.0 | V/ns |
| $t_2$ | SDRAM | SDRAM Rising and Falling Edge Rate | Between 0.4V and 2.4V | 1.5 | | 4.0 | V/ns |
| $t_3$ | CPUCLK | CPU Clock Rise Time | Between 0.4V and 2.0V, $V_{DDCPU}$ = 2.5V | 0.4 | | 1.6 | ns |
| $t_4$ | CPUCLK | CPU Clock Fall Time | Between 2.0V and 0.4V, $V_{DDCPU}$ = 2.5V | 0.4 | | 1.6 | ns |
| $t_5$ | CPUCLK | CPU-CPU Clock Skew | Measured at 1.25V, $V_{DDCPU}$ = 2.5V | | 100 | 250 | ps |
| $t_6$ | CPUCLK, PCICLK | CPU-PCI Clock Skew | Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks | 1.0 | 2.5 | 4.0 | ns |
| $t_7$ | CPUCLK, SDRAM | CPU-SDRAM Clock Skew | Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks | | | 500 | ps |
| $t_8$ | CPUCLK, SDRAM | Cycle-Cycle Clock Jitter | Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks | | | 250 | ps |
| $t_8$ | PCICLK | Cycle-Cycle Clock Jitter | Measured at 1.5V | | | 500 | ps |
| $t_9$ | CPUCLK, PCICLK, SDRAM | Power-up Time | CPU, PCI, and SDRAM clock stabilization from power-up | | | 3 | ms |

**Notes:**

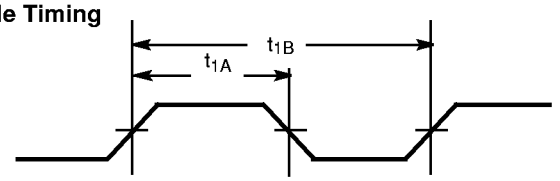
5. All parameters specified with loaded outputs.
6. Duty cycle is measured at 1.5V when $V_{DD}$ = 3.3V. When $V_{DDCPU}$ = 2.5V, CPUCLK duty cycle is measured at 1.25V.

## Timing Requirement for the I²C Bus

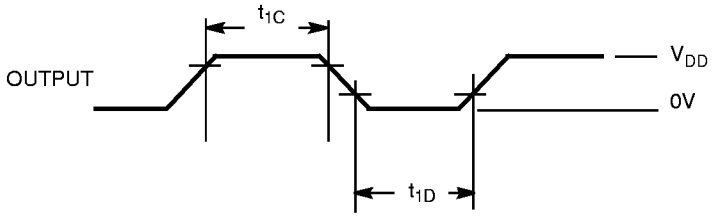
| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{10}$ | SCLK Clock Frequency | 0 | 100 | kHz |
| $t_{11}$ | Time the bus must be free before a new transmission can start | 4.7 | | µs |
| $t_{12}$ | Hold time start condition. After this period the first clock pulse is generated. | 4 | | µs |
| $t_{13}$ | The LOW period of the clock. | 4.7 | | µs |
| $t_{14}$ | The HIGH period of the clock. | 4 | | µs |
| $t_{15}$ | Setup time for start condition. (Only relevant for a repeated start condition.) | 4.7 | | µs |
| $t_{16}$ | Hold time DATA<br>for CBUS compatible masters.<br>for I²C devices | <br>5<br>0 | | µs |
| $t_{17}$ | DATA input set-up time | 250 | | ns |
| $t_{18}$ | Rise time of both SDATA and SCLK inputs | | 1 | µs |
| $t_{19}$ | Fall time of both SDATA and SCLK inputs | | 300 | ns |
| $t_{20}$ | Set-up time for stop condition | 4.0 | | µs |

## Switching Waveforms

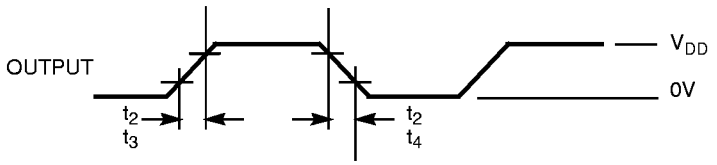
### Duty Cycle Timing



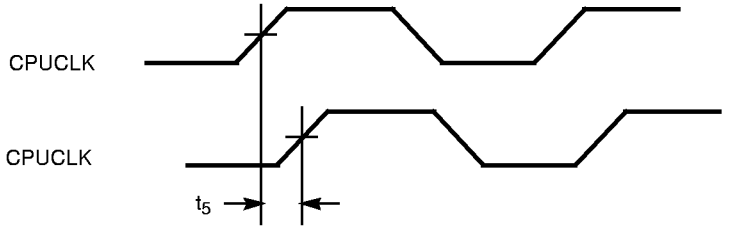

### CPUCLK Outputs HIGH/LOW Time




### All Outputs Rise/Fall Time

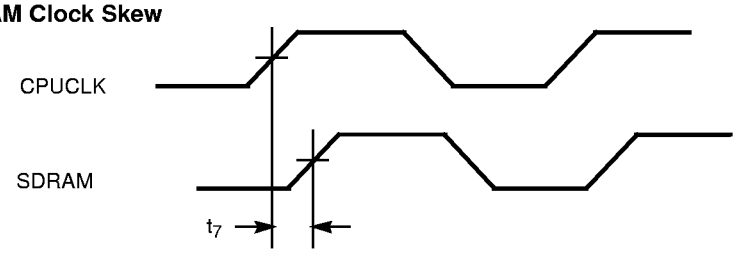



### CPU-CPU Clock Skew

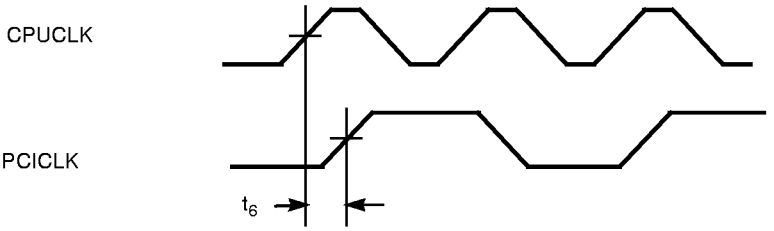


## Switching Waveforms (continued)

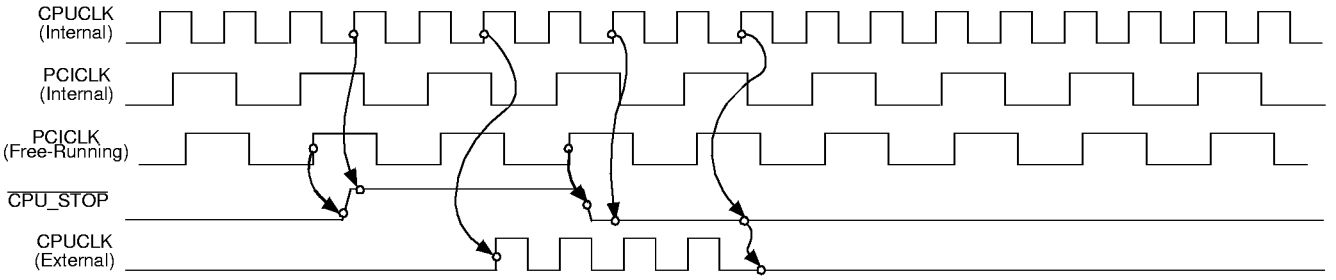
### CPU-SDRAM Clock Skew



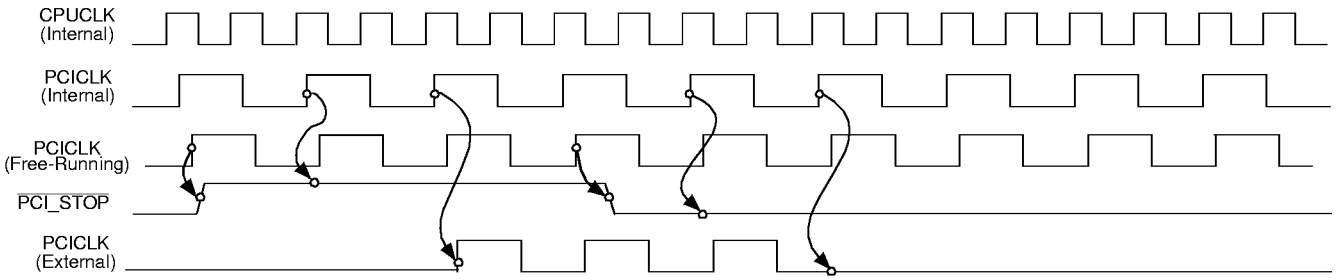

### CPU-PCI Clock Skew




### $\overline{\text{CPU\_STOP}}$ [7, 8]




### $\overline{\text{PCI\_STOP}}$ [9, 10]

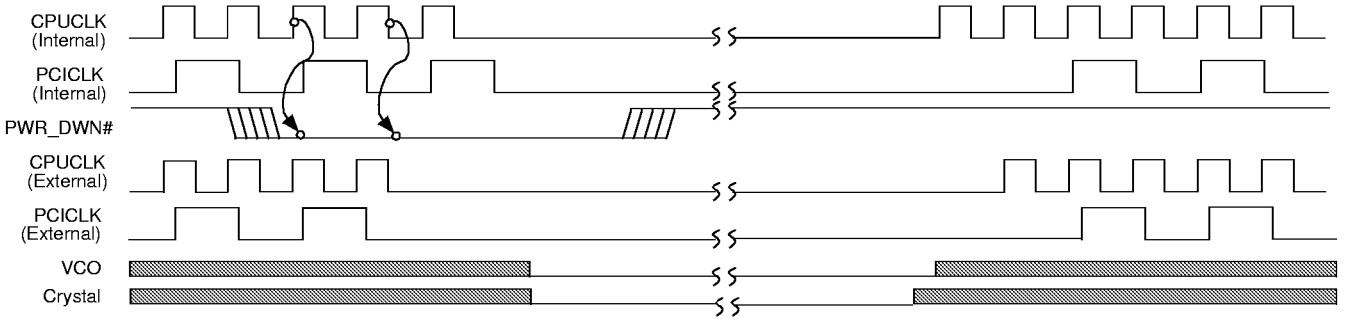



**Notes:**

7. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
8. CPU_STOP may be applied asynchronously. It is synchronized internally.
9. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
10. PCI_STOP may be applied asynchronously. It is synchronized internally.

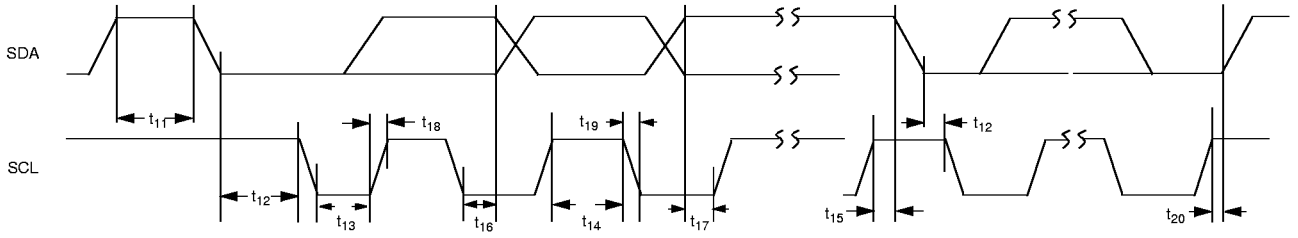
## Switching Waveforms (continued)

### PWR_DOWN




Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

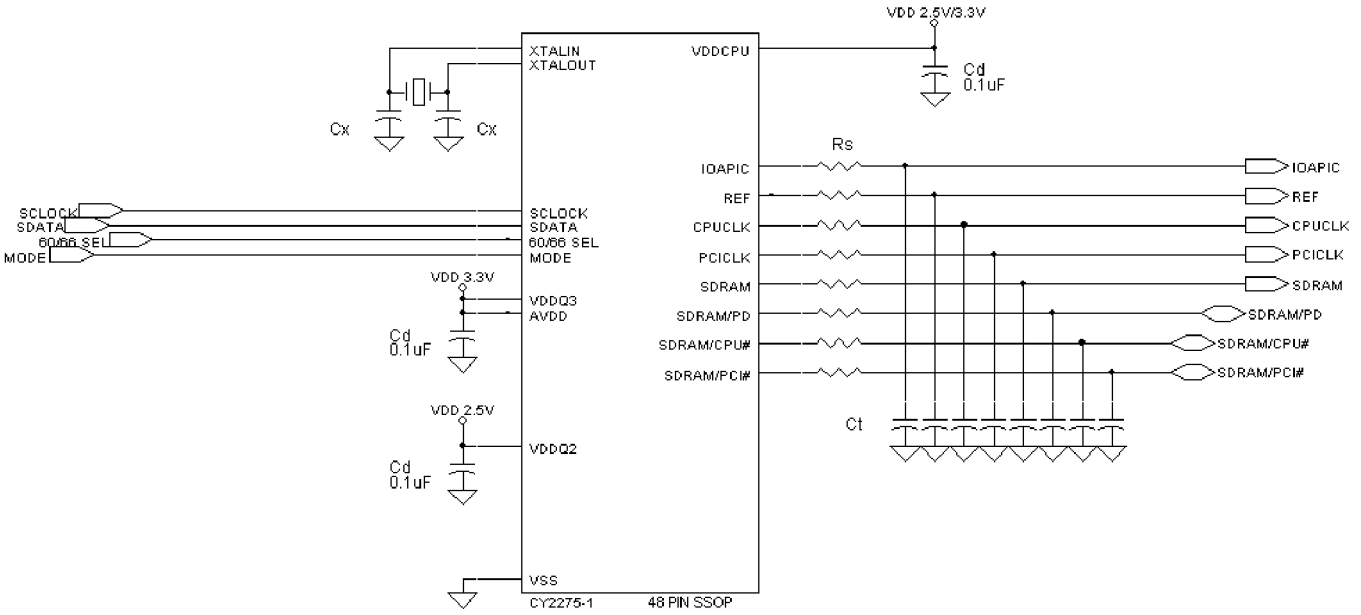
### Timing Requirements for the $I^2C$ Bus



## Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

## Application Circuit




Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

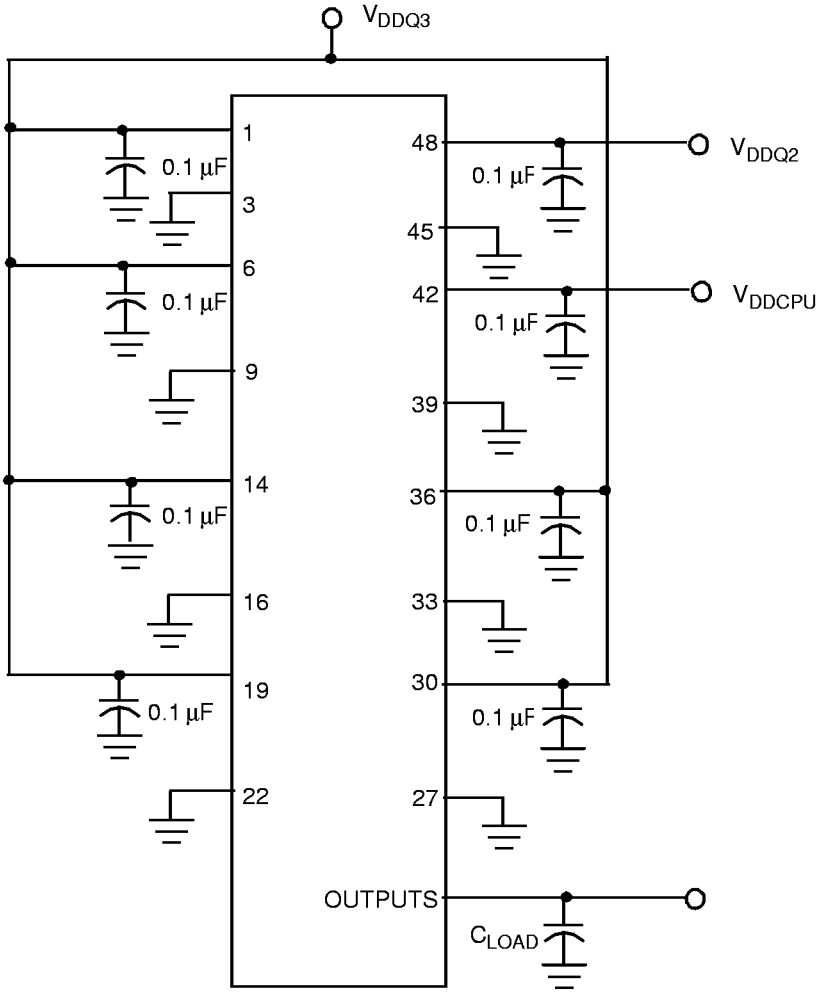
## Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and $C_{LOAD}$ of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different $C_{LOAD}$ is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where $R_{trace}$ is the loaded characteristic impedance of the trace, $R_{out}$ is the output impedance of the clock generator (specified in the data sheet), and $R_{series}$ is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board $V_{DD}$ from the clock generator $V_{DD}$ island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 µF–22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

## Test Circuit




Note: All capacitors should be placed as close to each pin as possible.

## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|
| CY2275APVC–11 | O48 | 48-Pin SSOP | Commercial |

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## Package Diagram

**48-Lead Shrunk Small Outline Package O48**