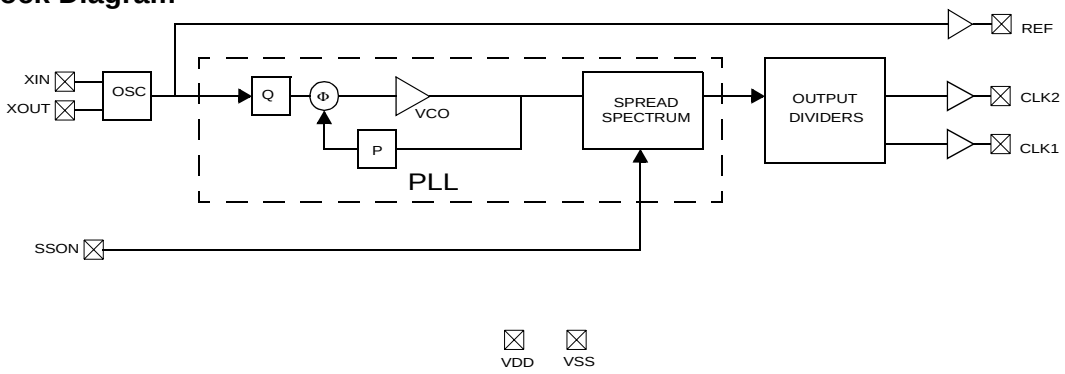
CY24210

100-MHz Clock Generator with Spread Spectrum

Features	Benefits
• **Integrated phase-locked loop (PLL)**	High-performance PLL tailored for multimedia applications
• **Low-jitter, high-accuracy outputs**	Meets critical timing requirements in complex system designs
• **Spread Spectrum**	Spread Spectrum outputs for EMI reduction
• **3.3V operation**	Enables application compatibility

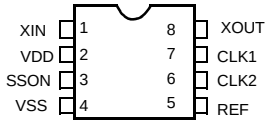
Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24210	3	14.31818 MHz	Two copies of 100 MHz, 14.31818 MHz

Logic Block Diagram



Pin Configurations

CY24210
8-pin SOIC



Spread Spectrum Profiles

Part Numbers	Center Spread Percentage
CY24210SC-3	± 1.875%
CY24210SC-4	± 1.375%
CY24210SC-5	± 2.375%
CY24210SC-6	± 2.875%
CY24210SC-7	± 3.375%

Pin Description

Pin Name	Pin Number	Description
X_{IN}	1	Reference Crystal Input
V_{DD}	2	Voltage Supply
SSON	3	Spread Spectrum Control for CLK1, CLK2, 0 = SS off, 1 = SS on, Internal Pull-up Resistor
V_{SS}	4	Ground
REF	5	Buffered Reference Clock Output
CLK2	6	100-MHz Clock Output with Spread Spectrum
CLK1	7	100-MHz Clock Output with Spread Spectrum
X_{OUT}[1]	8	Reference Crystal Output

Note:
1. Float X_{OUT} if X_{IN} is externally driven.

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	VDD + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	VDD + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	Reference Frequency		14.31818		MHz

DC Electrical Characteristics

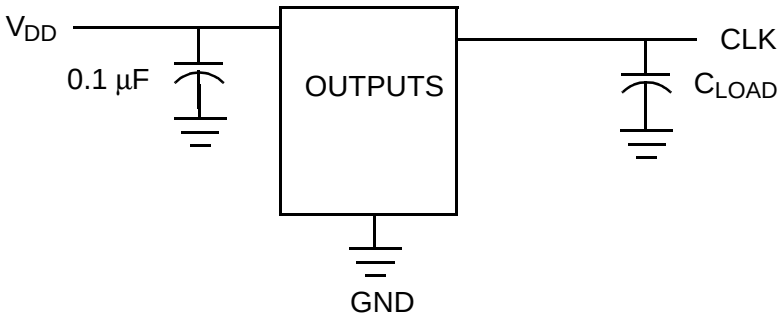
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V	12	24		mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$		5		µA
I_{IL}	Input Low Current	$V_{IL} = 0$V			50	µA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
C_{IN}	Input Capacitance				7	pF
I_{DD}	Supply Current	Sum of Core and Output Current			35	mA
R_{UP}	Pull-up Resistor on Input Pin		80	100	150	kΩ

AC Electrical Characteristics

Parameter[3]	Description	Conditions	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is Defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20%–80% of V_{DD}	0.8	1.4	2	V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80%–20% of V_{DD}	0.8	1.4	2	V/ns
t_5	Output to Output skew	CLK1 + CLK2 Equally Loaded			200	ps
t_9	Clock Jitter	Peak to Peak Period Jitter with Spread Off			300	ps
t_{10}	PLL Lock Time				3	ms

Note:
2. Rated for 10 years.
3. Not 100% tested.

Test Circuit



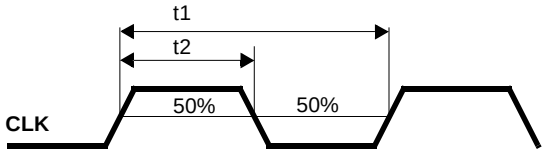


Figure 1. Duty Cycle Definition; DC = t2/t1

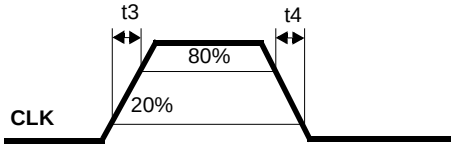


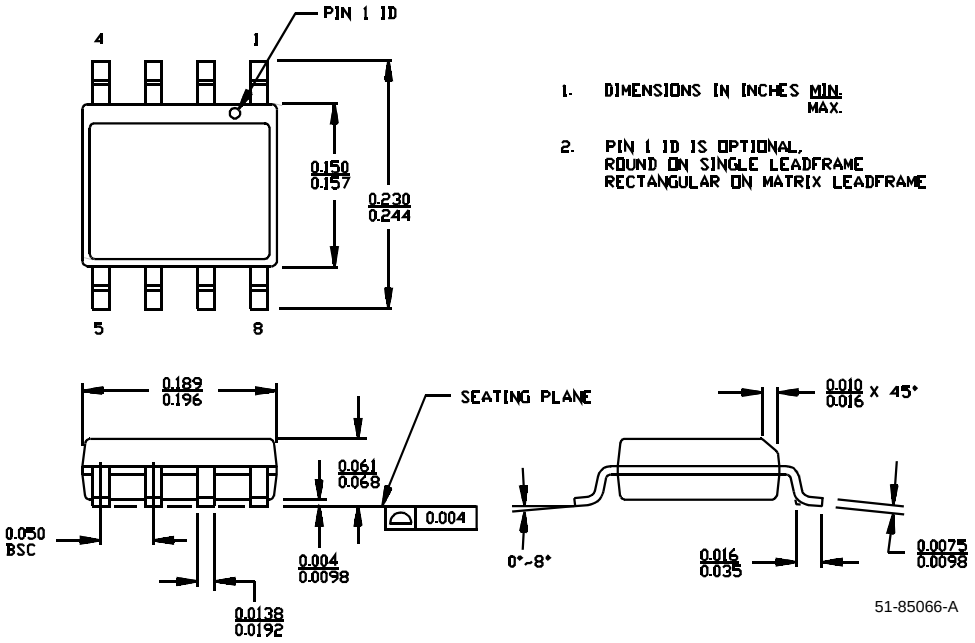
Figure 2. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24210-3	S8	8-pin SOIC	Commercial	3.3V
CY24210-4	S8	8-pin SOIC	Commercial	3.3V
CY24210-5	S8	8-pin SOIC	Commercial	3.3V
CY24210-6	S8	8-pin SOIC	Commercial	3.3V
CY24210-7	S8	8-pin SOIC	Commercial	3.3V

Package Diagram

8-lead (150-Mil) SOIC S8



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