Octal registered transceiver with 5-volt tolerant inputs/outputs; damping resistor; 3-state

74LVC22952A
74LVCH22952A

\FEATURES

- **5-volt tolerant inputs/outputs, for interfacing with 5-volt logic**
- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5V**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **3-state outputs**
- **Direct interface with TTL levels**
- **Bushold on all data inputs (LVCH22952A only).**
- **Integrated 30Ω damping resistor.**

DESCRIPTION

The 74LVC(H)22952A is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. The 74LVC(H)22952A is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs. The '22952A' is identical to the '22953A' but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP_{nn} to A_n, B_n	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)22952AD	24	SO24	plastic	SOT137-1
74LVC(H)22952ADB	24	SSOP24	plastic	SOT340-1
74LVC(H)22952APW	24	TSSOP24	plastic	SOT355-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	B_0 to B_7	B data inputs/outputs
12	GND	ground (0 V)
9, 15	$\overline{OE}_{AB}$, $\overline{OE}_{BA}$	output enable inputs (active LOW)
10, 14	CP_{AB}, CP_{BA}	clock inputs
11, 13	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	clock enable inputs
16, 17, 18, 19, 20, 21, 22, 23	A_0 to A_7	A data inputs/outputs
24	V_{CC}	positive supply voltage

FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	disable outputs
L	L	L	enable outputs
L	H	H	enable outputs

H = HIGH voltage level L = LOW voltage level ↑ = Low-to-High transition NC = no change
X = don't care Z = high impedance OFF-state

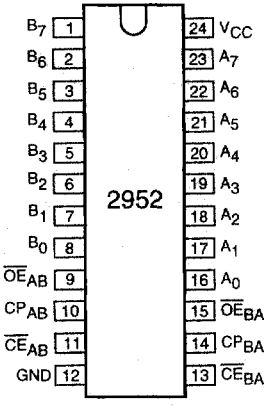


Fig.1 Pin configuration.

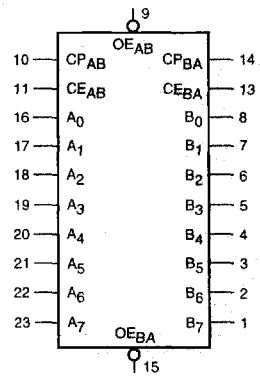


Fig.2 IEC logic symbol.

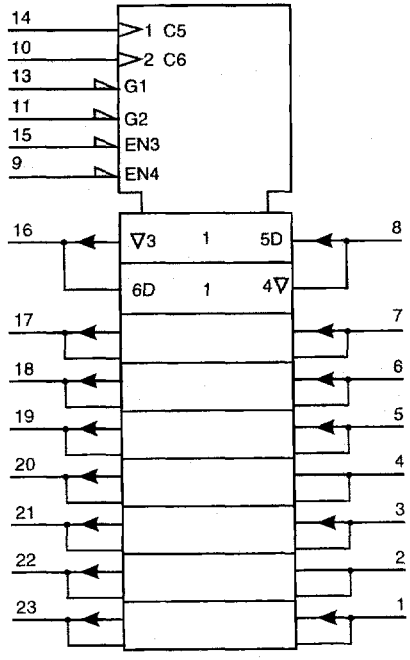


Fig.3 Logic symbol.

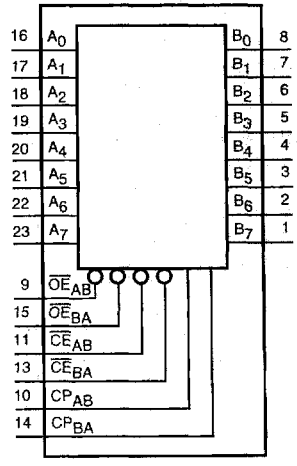


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC(H)22952A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC(H)22952A

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP_{BA}, CP_{AB} to A_n, B_n	–	–	–	ns	1.2	Figs 5, 8
		–	–	9.5		2.7	
		–	–	8.5		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	–	–	–	ns	1.2	Figs 7, 8
		–	–	9.5		2.7	
		–	–	8.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	–	–	–	ns	1.2	Figs 7, 8
		–	–	9.0		2.7	
		–	–	8.0		3.0 to 3.6	
t_w	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	3.3	–	–	ns	2.7	Fig. 5
		3.3	–	–		3.0 to 3.6	
t_{su}	set-up time, HIGH or LOW A_n, B_n to CP_{AB}, CP_{BA}	−2.5	–	–	ns	2.7	Fig. 6
		−2.5	–	–		3.0 to 3.6	
t_{su}	set-up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	2.5	–	–	ns	2.7	Fig. 6
		2.5	–	–		3.0 to 3.6	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	1.5	–	–	ns	2.7	Fig. 6
		1.5	–	–		3.0 to 3.6	
t_h	hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	1.5	–	–	ns	2.7	Fig. 6
		1.5	–	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	166	–	–	MHz	2.7	Fig. 6
		250	–	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

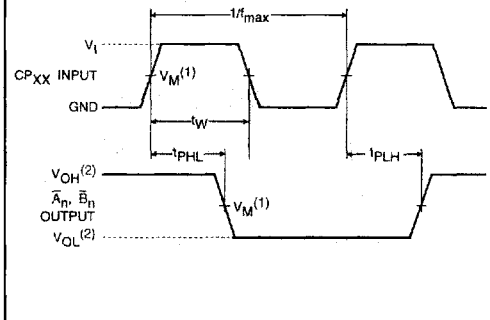


Fig. 5 Waveforms showing the clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

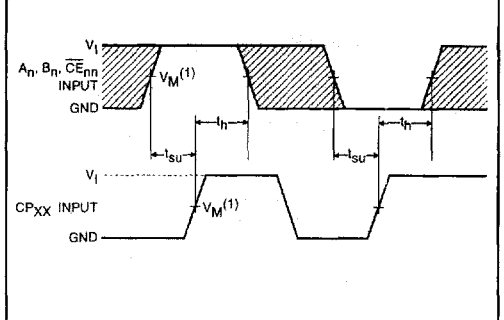


Fig.6 Waveforms showing the set-up and hold times for the A_n, B_n and $\overline{CE}_{nn}$ inputs.

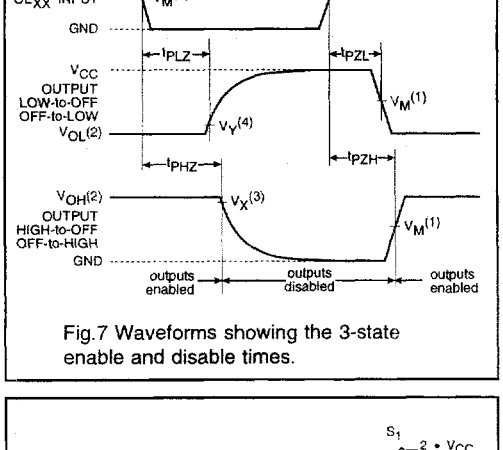
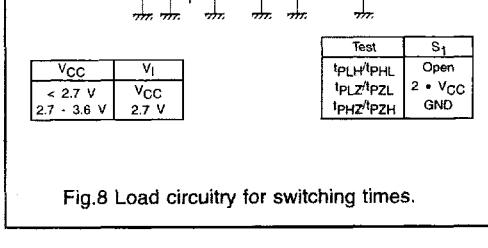


Fig.7 Waveforms showing the 3-state enable and disable times.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.



VCC	VI
< 2.7 V	VCC
2.7 - 3.6 V	2.7 V

Test	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 • VCC
tPHZ/tPZH	GND

Fig.8 Load circuitry for switching times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.