3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC16543A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC16543A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

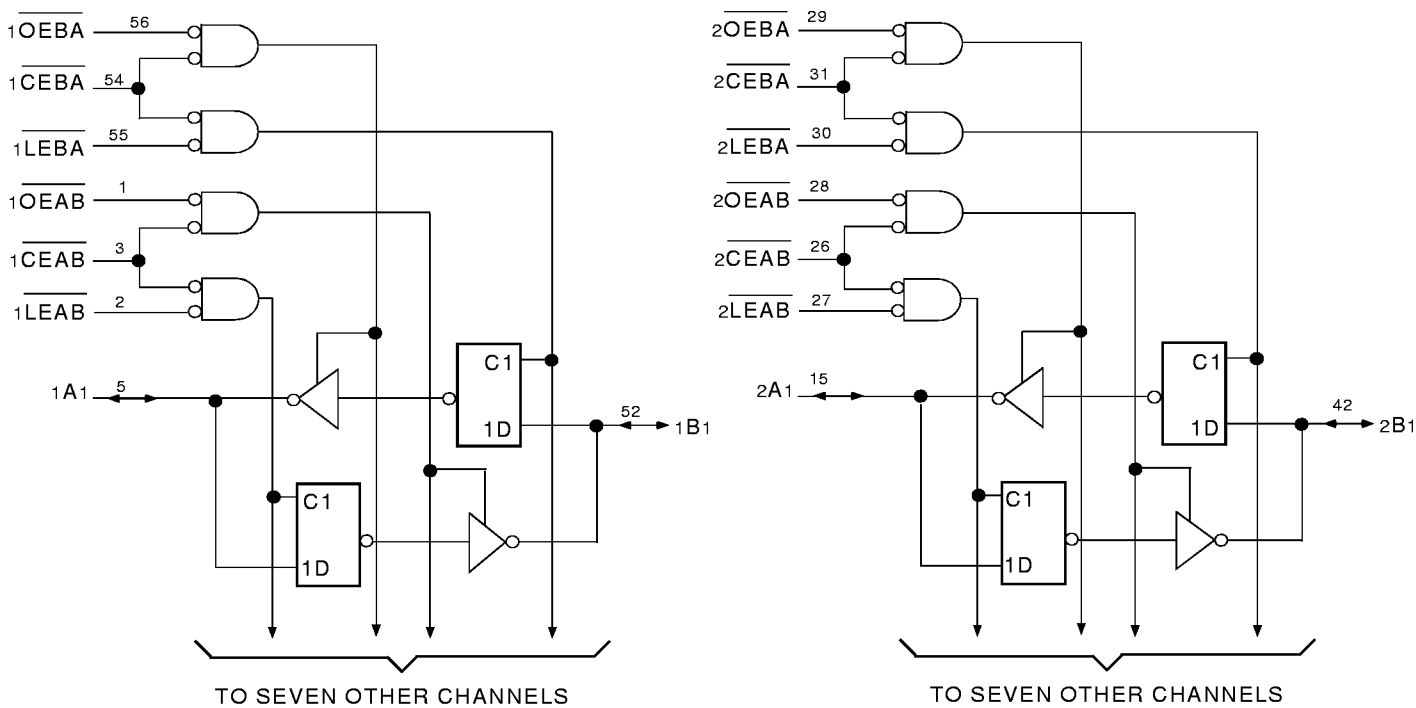
DESCRIPTION:

The LVC16543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low-power device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow. For example, the A-to-B enable ($\overline{CEAB}$) must be low to enter data from the A port or to output data from the B port. $\overline{LEAB}$ controls the latch function. When $\overline{LEAB}$ is low, the latches are transparent. A subsequent low-to-high transition of $\overline{LEAB}$ signal puts the A latches in the storage mode. $\overline{OEAB}$ performs the output enable function on the B port. Data flow from the B port to the A port is similar but requires using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

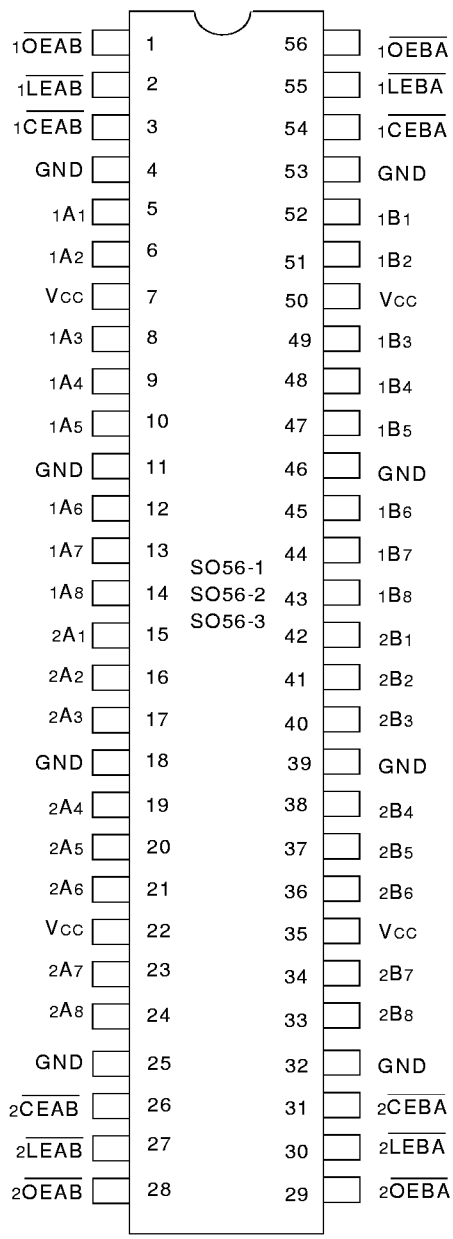
All pins of this 16-bit latched transceiver can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16543A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Functional Block Diagram



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

LVC Link

NOTE:
1. As applicable to the device type.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, V_I < 0 or V_O < 0	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

LVC Link

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

PIN DESCRIPTION

Pin Names	Description
x$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
x$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
x$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
x$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
x$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
x$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE (each 8-bit section) (1, 2)

Inputs				Outputs
x$\overline{CEAB}$	x$\overline{LEAB}$	x$\overline{OEAB}$	xAx	xBx
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0(3)
L	L	L	L	L
L	L	L	H	H

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. A-to-B data flow is shown; B-to-A flow control is the same except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
3. B_0 = Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: TA = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			$3.6 \leq V_{IN} \leq 5.5V$(2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V other inputs at V_{CC} or GND		—	—	500	µA

LVC Link

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

LVC Link

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per transceiver Outputs enabled	C_L = 0pF, f = 10Mhz	44	pF
C_{PD}	Power Dissipation Capacitance per transceiver Outputs disabled		4	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V_{CC} = 2.7V		V_{CC} = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xBx or xBx to xAx	—	6.1	1.2	5.4	ns
t_{PLH} t_{PHL}	Propagation Delay x$\overline{LEBA}$ or x$\overline{LEAB}$ to xAx or xBx	—	7.4	1.5	6.1	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx	—	7.9	1.2	6.6	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx	—	7.6	1	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx	—	7.1	1.5	6.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx	—	6.9	1.5	6.3	ns
t_{SU}	Set-up Time, data before $\overline{CE}\uparrow$	1.1	—	1.1	—	ns
t_{SU}	Set-up Time, data before $\overline{LE}\uparrow$, $\overline{CE}$ LOW	1.1	—	1.1	—	ns
t_H	Hold Time, data after $\overline{CE}\uparrow$	1.9	—	1.9	—	ns
t_H	Hold Time, data after $\overline{LE}\uparrow$, $\overline{CE}$ LOW	1.9	—	1.9	—	ns
t_W	Pulse Duration, x$\overline{LEAB}$ or x$\overline{LEBA}$, x$\overline{CEAB}$ or x$\overline{CEBA}$ LOW	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

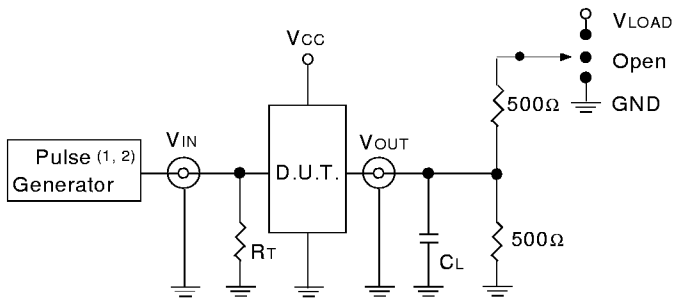
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V ±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$= 2.5V ±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

LVC Link

TEST CIRCUITS FOR ALL OUTPUTS



LVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

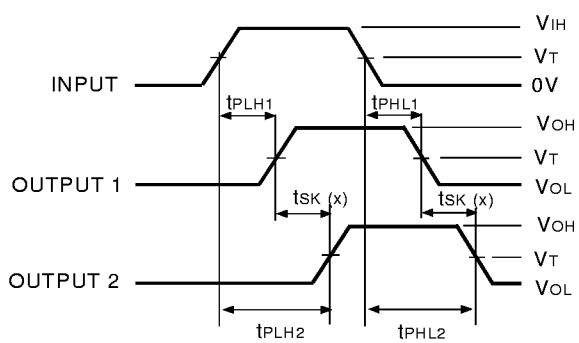
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

LVC Link

OUTPUT SKEW - tsk (x)



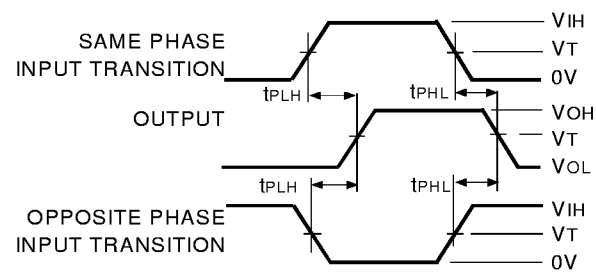
$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

LVC Link

NOTES:

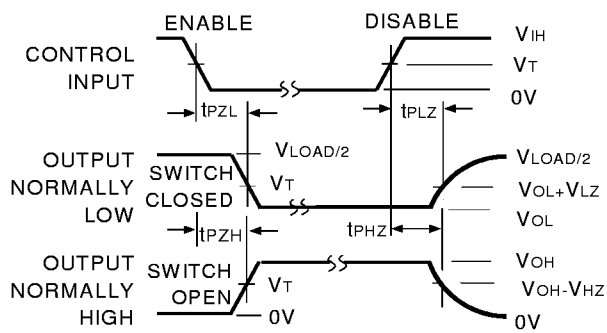
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



LVC Link

ENABLE AND DISABLE TIMES

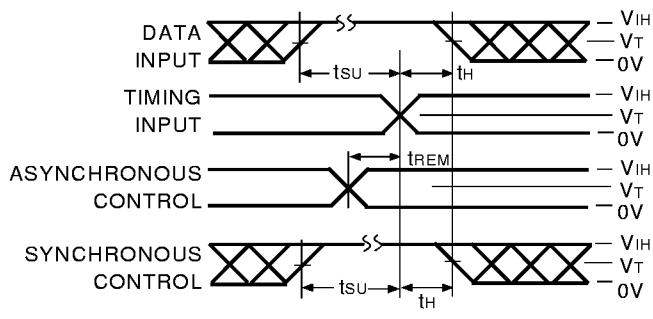


LVC Link

NOTE:

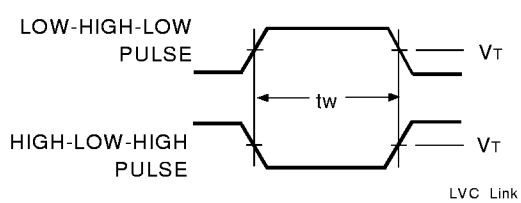
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



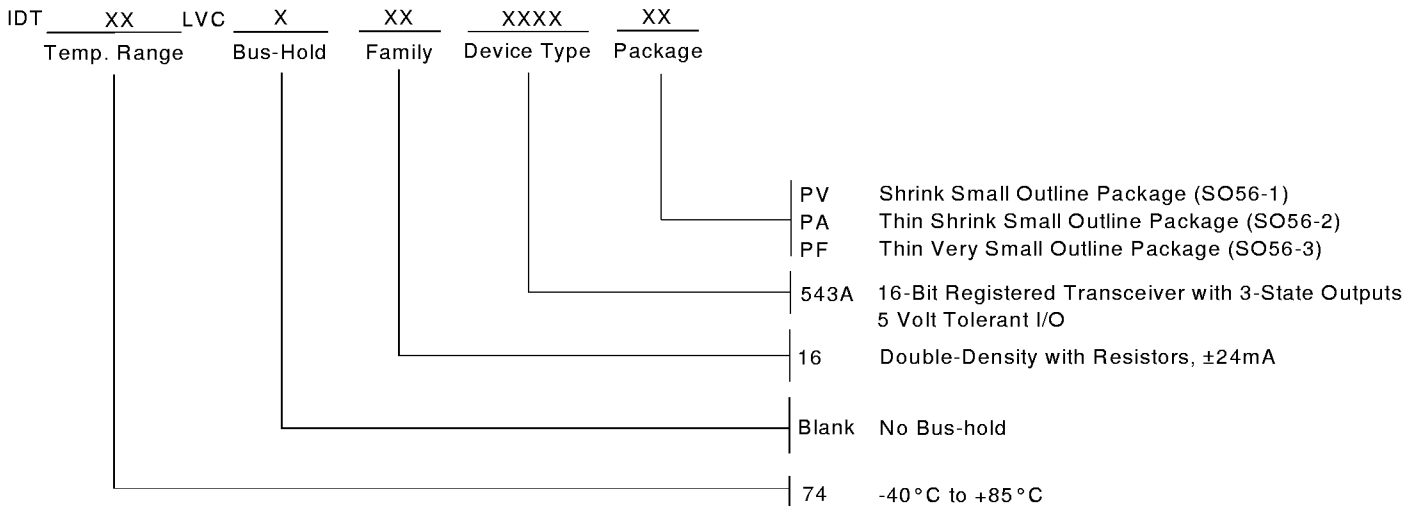
LVC Link

PULSE WIDTH



LVC Link

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*