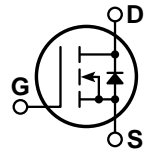
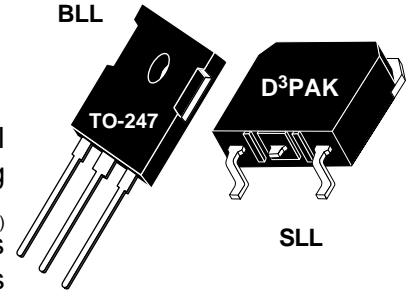


POWER MOS 7® MOSFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package


MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT1001R6BLL/SLL	UNIT
V_{DSS}	Drain-Source Voltage	1000	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	8	Amps
I_{DM}	Pulsed Drain Current ^①	32	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	266	Watts
	Linear Derating Factor	2.13	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	4	Amps
E_{AR}	Repetitive Avalanche Energy ^①	16	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	425	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	1000			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	8			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 4A$)			1.60	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 800V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 500V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1\text{mA}$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT1001R6BLL/SL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		1322		pF
C _{oss}	Output Capacitance			230		
C _{rss}	Reverse Transfer Capacitance			42		
Q _g	Total Gate Charge ③	V _{GS} = 10V V _{DD} = 500V I _D = 8A @ 25°C		53		nC
Q _{gs}	Gate-Source Charge			7		
Q _{gd}	Gate-Drain ("Miller") Charge			35		
t _{d(on)}	Turn-on Delay Time	V _{GS} = 15V V _{DD} = 500V _S I _D = 8A @ 25°C R _G = 0.6Ω		18		ns
t _r	Rise Time			18		
t _{d(off)}	Turn-off Delay Time			32		
t _f	Fall Time			19		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			8	Amps
I _{SM}	Pulsed Source Current ① (Body Diode)			32	
V _{SD}	Diode Forward Voltage ② (V _{GS} = 0V, I _S = -8A)			1.3	Volts
t _{rr}	Reverse Recovery Time (I _S = -8A, di _S /dt = 100A/μs)		630		ns
Q _{rr}	Reverse Recovery Charge (I _S = -8A, di _S /dt = 100A/μs)		6.1		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			10	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.47	°C/W
R _{θJA}	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 13.28mH, R_G = 25Ω, Peak I_L = 8A

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ -I_D 8A di/dt ≤ 700A/μs V_R ≤ V_{DSS} T_J ≤ 150°C

APT Reserves the right to change, without notice, the specifications and information contained herein.

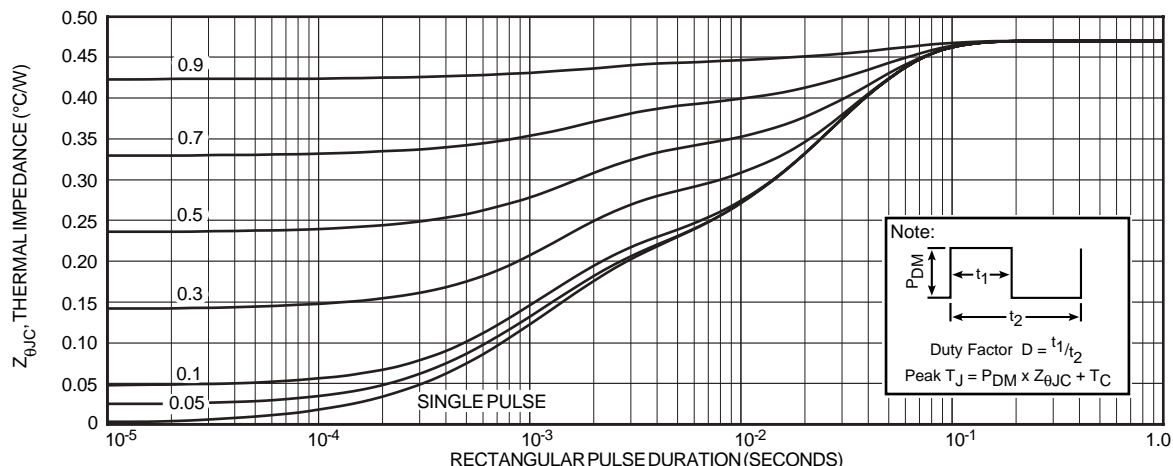


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT1001R6BLL/SLL

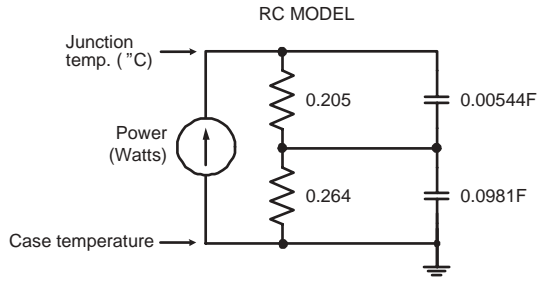


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

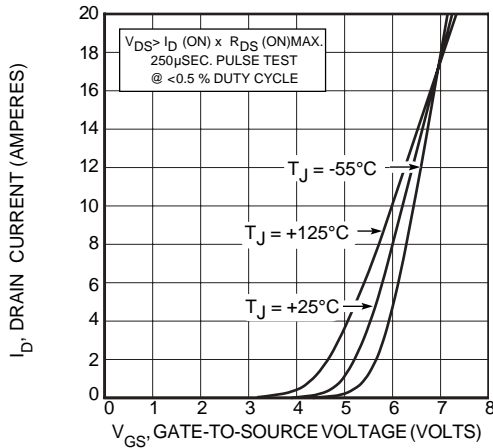


FIGURE 4, TRANSFER CHARACTERISTICS

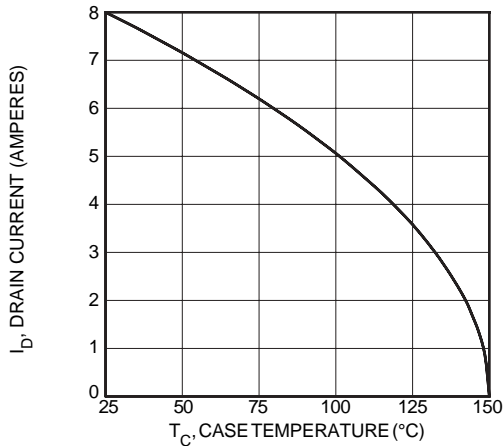


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

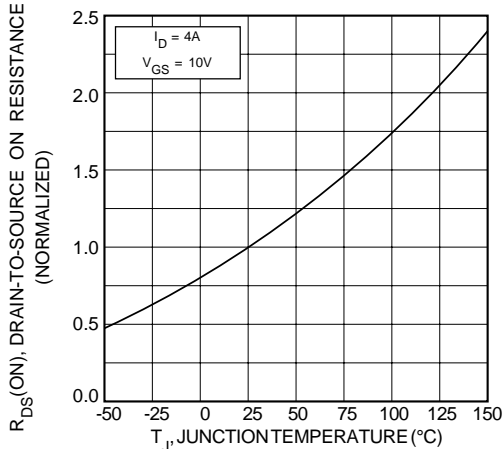


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

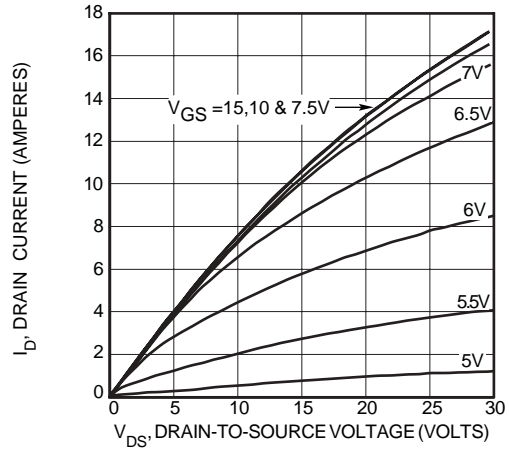


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

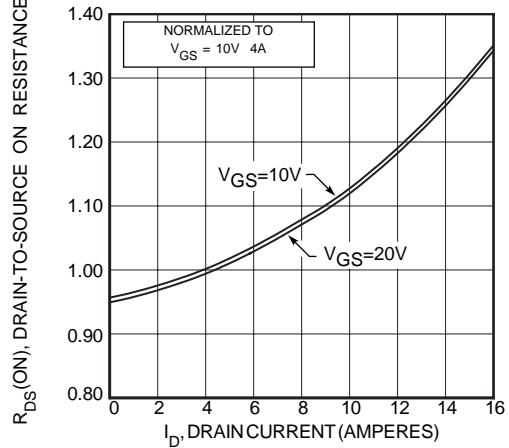


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

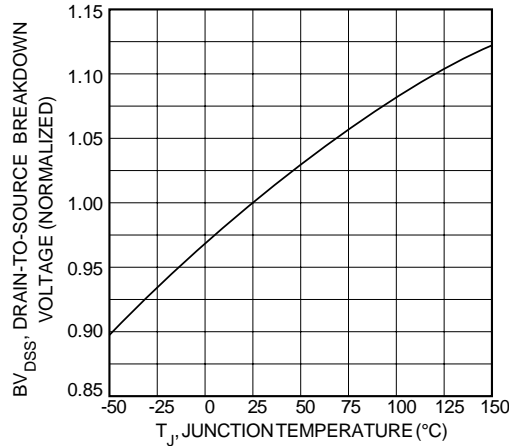


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

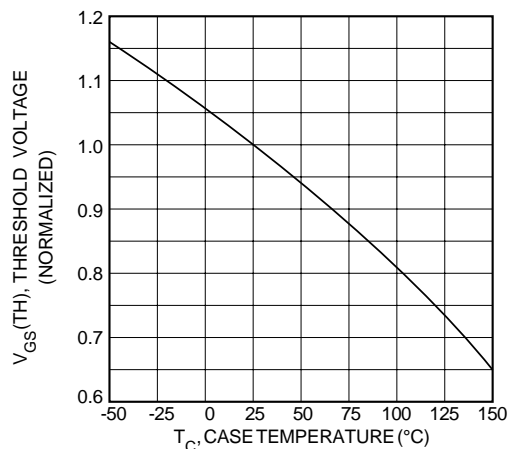


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

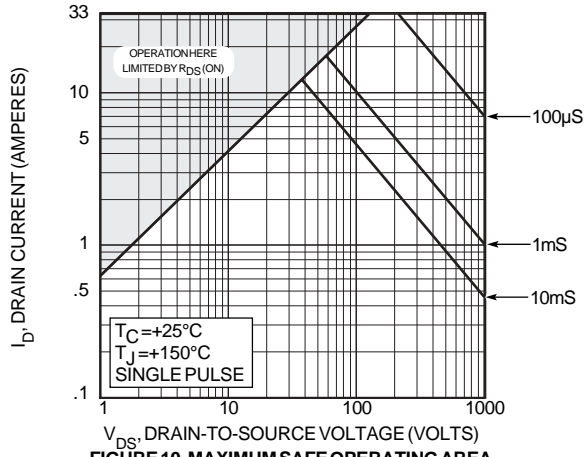


FIGURE 10, MAXIMUM SAFE OPERATING AREA

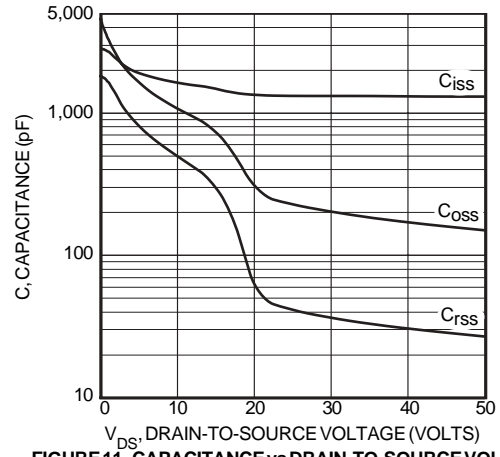


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

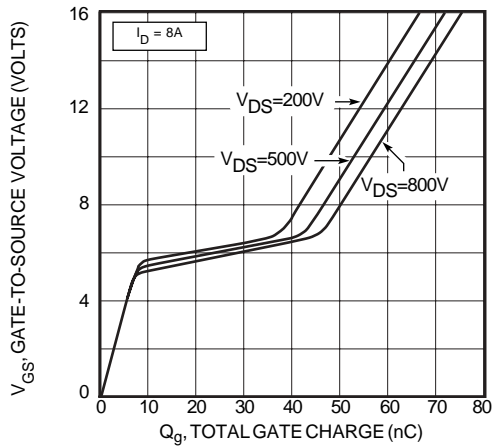


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

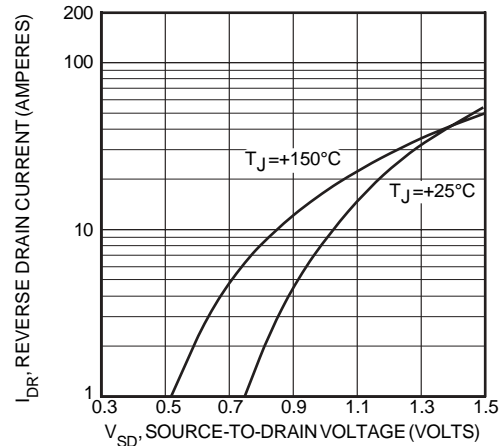
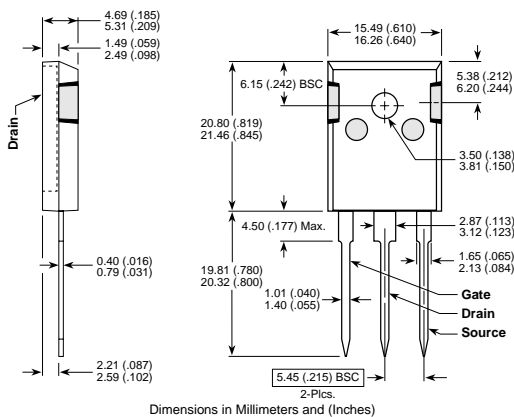


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline



D³PAK Package Outline

