

TC74LCX16646AFT

Low Voltage 16-Bit Bus Transceiver/Register with 5V Tolerant Inputs and Outputs

The TC74LCX16646AFT is a high performance CMOS 16-BIT BUS TRANSCEIVER/REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This device is a bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

All inputs are equipped with protection circuits against static discharge.

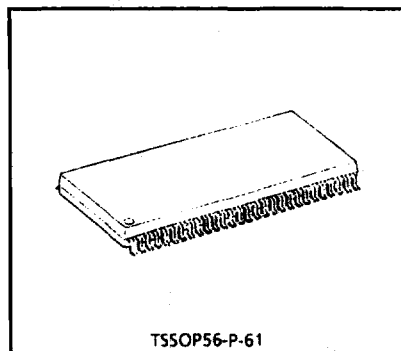
Features

- Low Voltage Operation: $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation: $t_{pd} = 6.0ns$ (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output Current: $I_{OH}/I_{OL} = 24mA$ (Min.) ($V_{CC} = 3.0V$)
- Latch-up Performance: $\pm 500mA$
- Package: TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 5V and 3.3V signals.
- Power down protection is provided on all inputs and outputs.

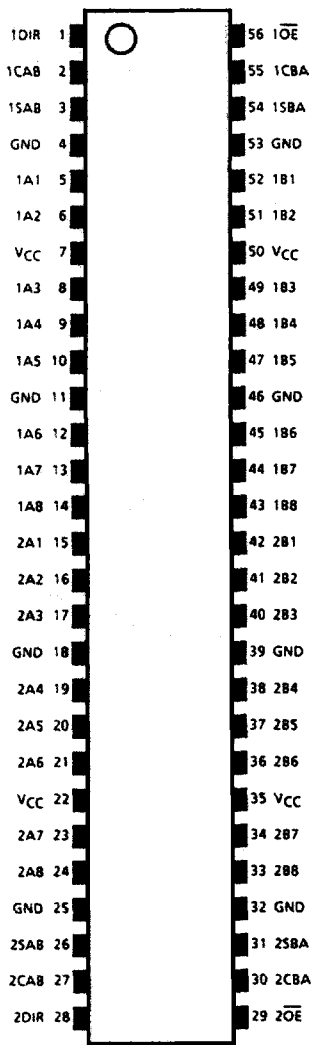
(Note)

Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminal must have their input level fixed by means of pull-up or pull-down resistors.

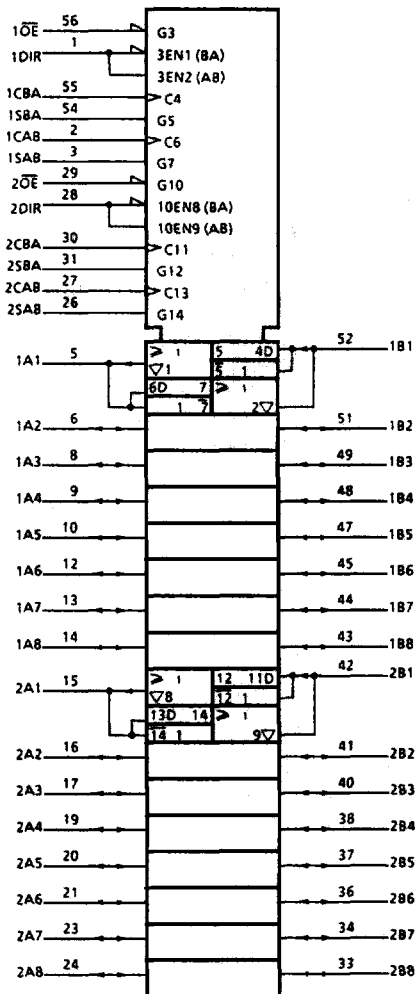


Weight : 0.25g (Typ.)



(TOP VIEW)

Pin Assignment



Symbol

Truth Table

Control Inputs						Bus		Function
\overline{OE}	DIR	CAB	CBA	SAB	SBA	A	B	
H	X	X*	X*	X	X	Input Z	Input Z	The output functions of A and B Busses are disabled.
		f	f	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	Input L H	Output L H	The data on the A bus are displayed on the B bus.
		f	X*	L	X	L H	L H	The data on the A bus are displayed on the B bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B bus.
		f	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	Output L H	Input L H	The data on the B Bus are displayed on the A bus.
		X*	f	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	f	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

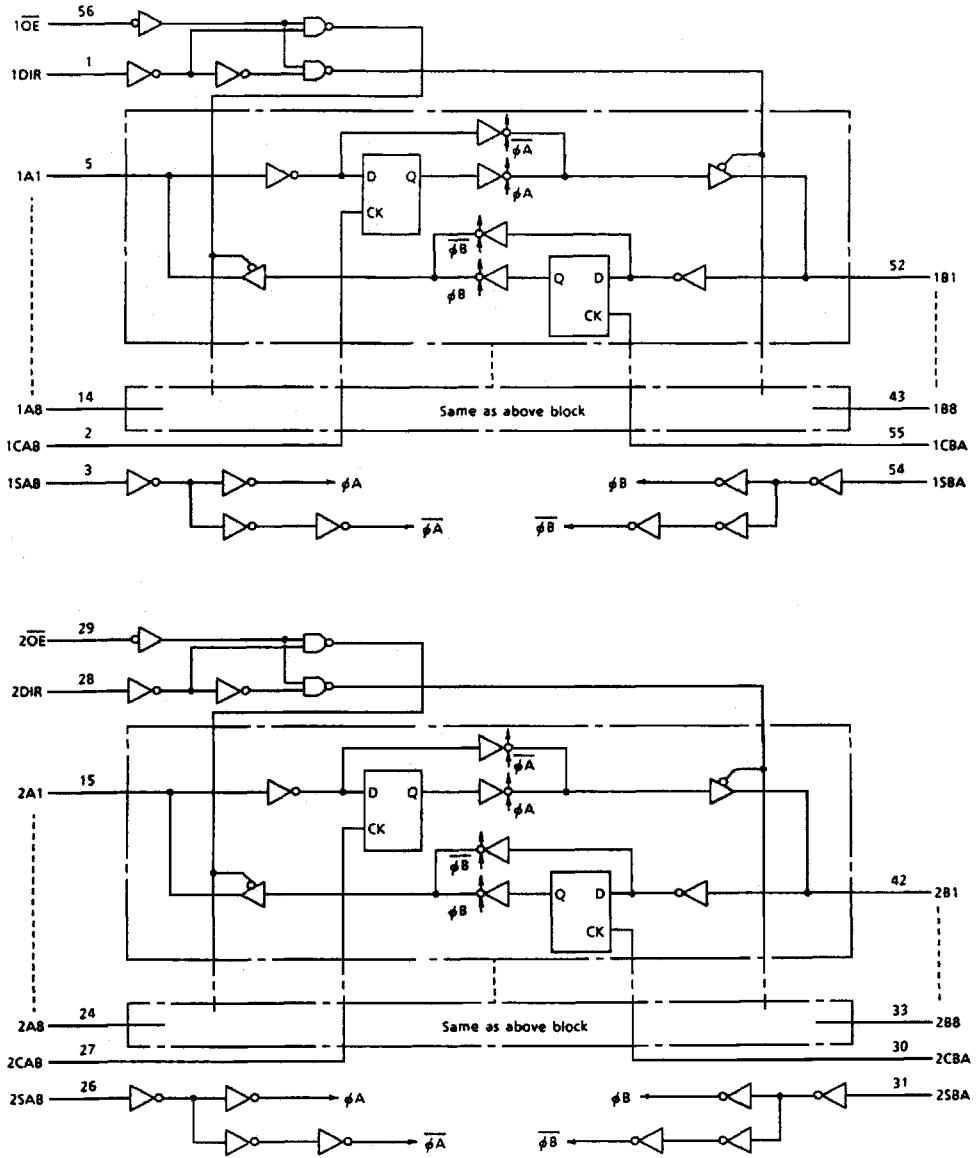
X: Don't Care

Z: High Impedance

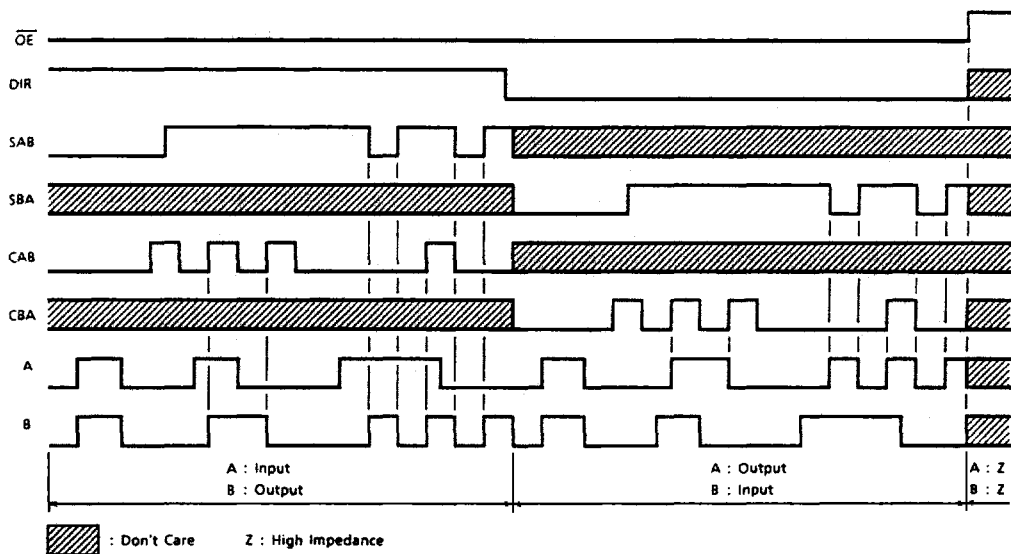
Qn: The data soted into the internal flip-flops by most recent low to high transition of the clock inputs.

*: The clocks are not internally gated with either \overline{OE} or DIR. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

System Diagram



Timing Chart



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 - 7.0	V
DC Input Voltage (DIR, \overline{OE} , CAB, CBA, SAB, SBA)	V_{IN}	-0.5 - 7.0	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5 - 7.0 (Note 1) -0.5 - V_{CC} + 0.5 (Note 2)	V
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} /Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	-65 - 150	°C

(Note 1) Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ **Recommended Operating Conditions**

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.0 - 3.6 1.5 - 3.6 (Note 4)	V
Input Voltage (DIR, \overline{OE} , CAB, CBA, SAB, SBA)	V_{IN}	0 - 5.5	V
Bus I/O Voltage	$V_{I/O}$	0 - 5.5 (Note 5) 0 - V_{CC} (Note 6)	V
Output Current	I_{OH}/I_{OL}	±24 (Note 7) ±12 (Note 8)	mA
Operating Temperature	T_{opr}	-40 - 85	°C
Input Rise and Fall Time	dt/dv	0 - 10 (Note 9)	ns/V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 - 3.6V$ (Note 8) $V_{CC} = 2.7 - 3.0V$ (Note 9) $V_{IN} = 0.8 - 2.0V$, $V_{CC} = 3.0V$

Electrical Characteristics

DC Characteristics (Ta = -40 ~ 85°C)

Parameter	Symbol	Test Condition		V _{CC} (V)	Min.	Max.	Unit	
Input Voltage	"H" Level	V _{IH}		2.7 - 3.6	2.0	-	V	
	"L" Level	V _{IL}		2.7 - 3.6	-	0.8		
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100µA	2.7 - 3.6	V _{CC} - 0.2	-	V
				I _{OH} = -12mA	2.7	2.2	-	
				I _{OH} = -18mA	3.0	2.4	-	
				I _{OH} = -24mA	3.0	2.2	-	
"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100µA	2.7 - 3.6	-	0.2		
			I _{OL} = 12mA	2.7 - 3.6	-	0.4		
			I _{OL} = 16mA	3.0	-	0.4		
			I _{OL} = 24mA	3.0	-	0.55		
Input Leakage Current	I _{IN}	V _{IN} = 0 - 5.5V		2.7 - 3.6	-	±5.0	µA	
3-State Output Off-State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 - 5.5V		2.7 - 3.6	-	±5.0	µA	
Power Off Leakage Current	I _{OFF}	V _{IN} /V _{OUT} = 5.5V		0	-	10.0	µA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND V _{IN} /V _{OUT} = 3.6 - 5.5V		2.7 - 3.6	-	20.0	µA	
				2.7 - 3.6	-	±20.0		
Increase in I _{CC} per Input	ΔI _{CC}	V _{IH} = V _{CC} - 0.6V		2.7 - 3.6	-	500		

AC Characteristics (Ta = -40 ~ 85°C)

Parameter	Symbol	Test Condition	V _{CC} (V)	Min.	Max.	Unit
Maximum Clock Frequency	f _{MAX}	(Fig. 1, 2)	2.7 3.3±0.3	— 170	— —	MHz
Propagation Delay Time (An, Bn - Bn, An)	t _{pLH} t _{pHL}	(Fig. 1, 2)	2.7 3.3±0.3	— 1.5	6.6 6.0	ns
Propagation Delay Time (CAB, CBA - Bn, An)	t _{pLH} t _{pLH}	(Fig. 1, 5)	2.7 3.3±0.3	— 1.5	8.3 7.5	ns
Propagation Delay Time (SAB, SBA - Bn, An)	t _{pLH} t _{pLH}	(Fig. 1, 2)	2.7 3.3±0.3	— 1.5	8.3 7.5	ns
Output Enable Time (OE, DIR - An, Bn)	t _{pZL} t _{pZH}	(Fig. 1, 3, 4)	2.7 3.3±0.3	— 1.5	8.3 7.5	ns
Output Disable Time (OE, DIR - An, Bn)	t _{pLZ} t _{pHZ}	(Fig. 1, 3, 4)	2.7 3.3±0.3	— 1.5	8.3 7.5	ns
Minimum Pulse Width	t _w (H) t _w (L)	(Fig. 1, 5)	2.7 3.3±0.3	4.0 3.0	— —	ns
Minimum Setup Time	t _s	(Fig. 1, 5)	2.7 3.3±0.3	2.5 2.5	— —	ns
Minimum Hold Time	t _h	(Fig. 1, 5)	2.7 3.3±0.3	1.5 1.5	— —	ns
Output to Output Skew	t _{osLH} t _{osHL}	(Note 10)	2.7 3.3±0.3	— —	— 1.0	ns

(Note 10) Parameter guaranteed by design. (t_{osLH} = t_{pLHm} - t_{pLHn}, t_{osHL} = t_{pHLm} - t_{pHLn})

Dynamic Switching Characteristics (Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

Parameter	Symbol	Test Condition	V _{CC} (V)	Typical	Unit
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

Capacitive Characteristics

Parameter	Symbol	Test Condition	Ta = 25°C		Unit
			V _{CC} (V)	Typical	
Input Capacitance	C _{IN}	DIR, OE, CAB, CBA, SAB, SBA	3.3 ± 0.3	7	pF
Bus Input Capacitance	C _{I/O}	An, Bn	3.3 ± 0.3	8	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 11)	3.3 ± 0.3	25	pF

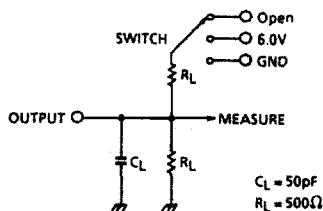
(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

TEST CIRCUIT

Fig. 1



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0V
t _{pHZ} , t _{pZH}	GND
t _w , t _s , t _r , t _{MAX}	Open

AC WAVEFORM

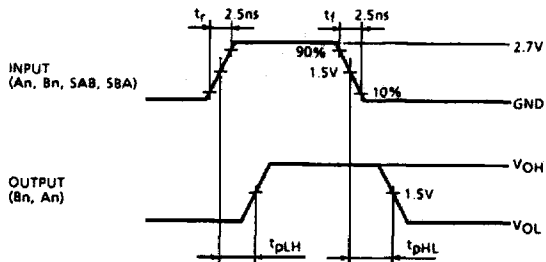
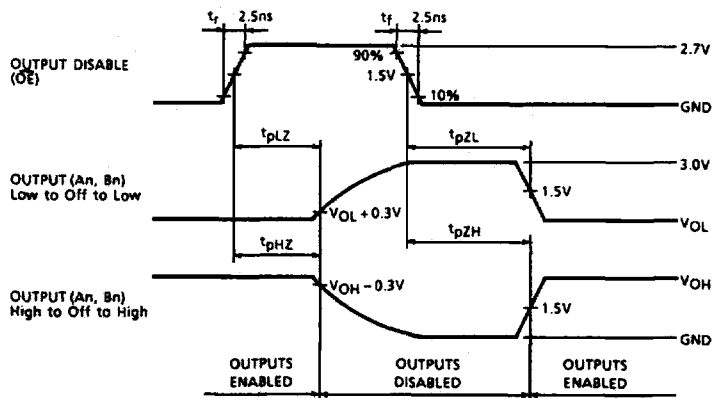
Fig.2 t_{pLH} , t_{pHL} Fig.3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} 

Fig.4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

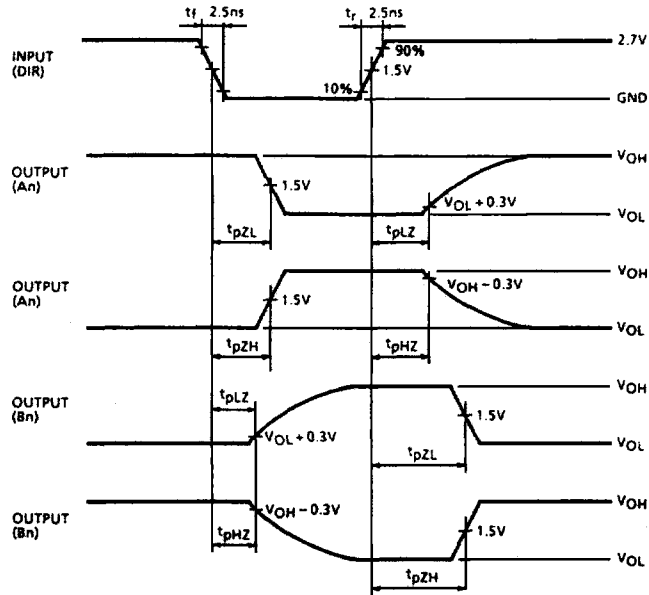
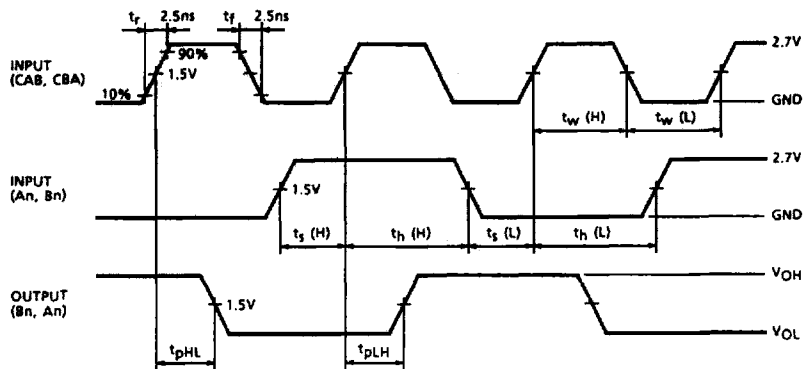


Fig.5 t_{pLH} , t_{pHL} , t_w , t_s , t_h



Notes

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