

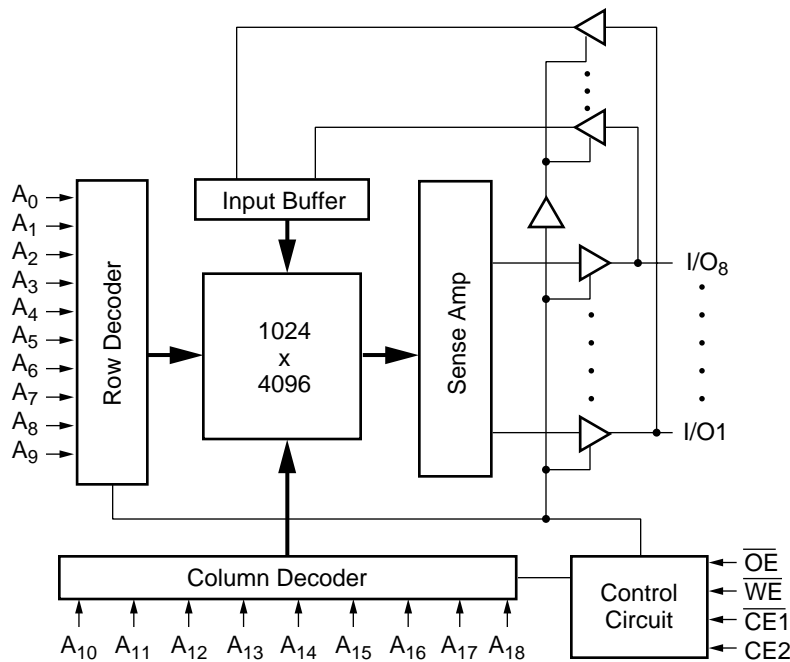
Features

- High-speed: 55, 70 ns
- Ultra low standby current of 10µA (max.)
- Fully static operation
- All inputs and outputs directly compatible
- Three state outputs
- Ultra low data retention current ($V_{CC} = 1.5V$)
- Operating voltage: 2.3V–2.8V
- Packages
 - 32-Pin TSOP (Standard)
 - 48-Ball CSP BGA (8mm x 10mm)

Description

The V62C2184096 is a very low power CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$, and active HIGH CE2, an active LOW \overline{OE} , and three static I/O's. This device has an automatic power-down mode feature when deselected.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power		Temperature Mark
	T	B	55	70	L	LL	
0°C to 70 °C	•	•	•	•	•	•	Blank
-40°C to +85°C	•	•	•	•		•	I

Pin Descriptions

A₀–A₁₈ Address Inputs

These 19 address inputs select one of the 512K x 8 bit segments in the RAM.

\overline{CE}_1 , CE₂* Chip Enable Inputs

\overline{CE}_1 is active LOW and CE₂ is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when deselected.

\overline{OE} Output Enable Input

The Output Enable input is active LOW. When \overline{OE} is LOW with \overline{CE} LOW and \overline{WE} HIGH, data of the selected memory location will be available on the I/O pins. When \overline{OE} is HIGH, the I/O pins will be in the high impedance state.

\overline{WE} Write Enable Input

An active LOW input, \overline{WE} input controls read and write operations. When \overline{CE} and \overline{WE} inputs are both LOW, the data present on the I/O pins will be written into the selected memory location.

I/O₁–I/O₈ Data Input and Data Output Ports

These 8 bidirectional ports are used to read data from and write data into the RAM.

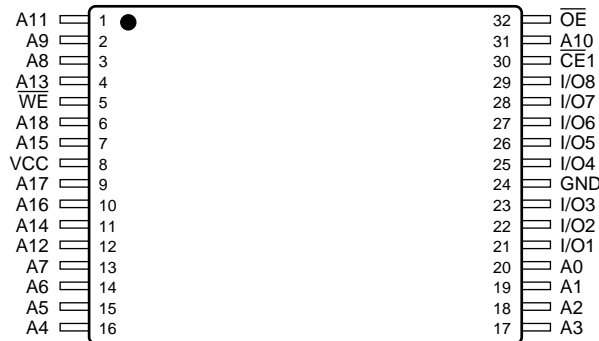
V_{CC} Power Supply

GND Ground

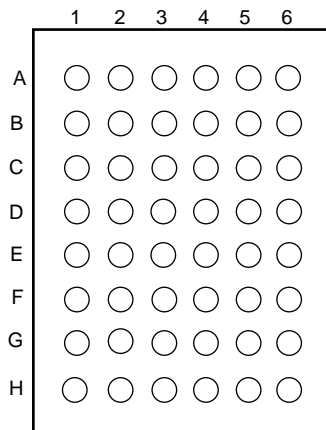
*CE₂ is available on BGA package only.

Pin Configurations (Top View)

32-Pin TSOP (Standard)



48 BGA



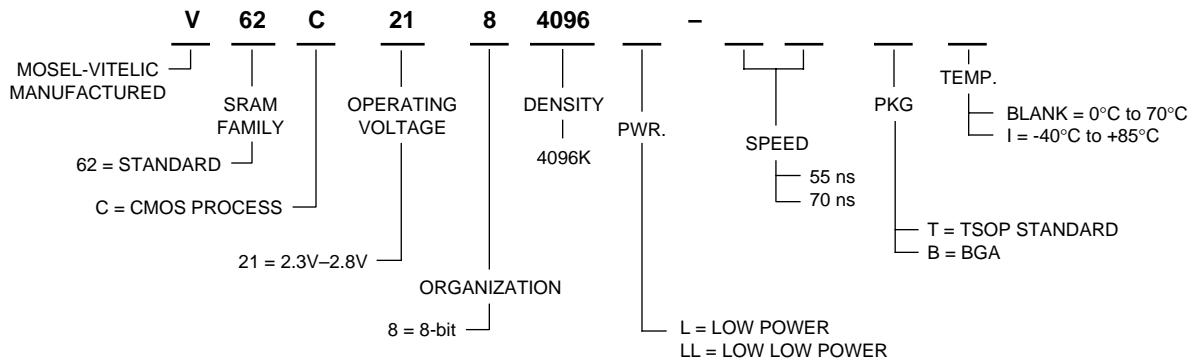
TOP VIEW

	1	2	3	4	5	6
A	A0	A1	CE2	A3	A6	A8
B	I/O5	A2	\overline{WE}	A4	A7	I/O1
C	I/O6	NC	NC	A5	NC	I/O2
D	VSS	NC	NC	NC	NC	VCC
E	VCC	NC	NC	NC	NC	VSS
F	I/O7	NC	A18	A17	NC	I/O3
G	I/O8	\overline{OE}	CE1	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

Note: NC means no connect.

TOP VIEW

Part Number Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Industrial	Units
V _{CC}	Supply Voltage	-0.5 to + V _{CC} + 0.5	-0.5 to + V _{CC} + 0.5	V
V _N	Input Voltage	-0.5 to + V _{CC} + 0.5	-0.5 to + V _{CC} + 0.5	V
V _{DQ}	Input/Output Voltage Applied	V _{CC} + 0.3	V _{CC} + 0.3	V
T _{BIAS}	Temperature Under Bias	-10 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C

NOTE:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{IO} = 0V	8	pF

NOTE:

- This parameter is guaranteed and not tested.

Truth Table

Mode	\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O Operation
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Output Disable	L	H	H	H	High Z
Read	L	H	L	H	D _{OUT}
Write	L	H	X	L	D _{IN}

NOTE:

X = Don't Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, $V_{CC} = 2.3V-2.8V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage ^(1,2)		-0.5	—	0.4	V
V_{IH}	Input HIGH Voltage ⁽¹⁾		2.0	—	$V_{CC}+0.3$	V
I_{IL}	Input Leakage Current	$V_{CC} = \text{Max}, V_{IN} = 0V \text{ to } V_{CC}$	—	—	1	μA
I_{OL}	Output Leakage Current	$V_{CC} = \text{Max}, \overline{CE}_1 = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	—	1	μA
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 2mA$	—	—	0.4	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -0.5mA$	$V_{CC}-0.4$	—	—	V

Symbol	Parameter	Comm.	Ind.	Units	
I_{CC1}	Average Operating Current, $\overline{CE}_1 = V_{IL}, CE_2 = V_{CC} - 0.2$, Output Open, $V_{CC} = \text{Max.}, f = f_{MAX}^{(3)}$	20	30	mA	
I_{SB}	TTL Standby Current $\overline{CE}_1 \geq V_{IH}, CE_2 \leq V_{IL}, V_{CC} = \text{Max.}, f = 0$	L	0.5	1	mA
		LL	0.3	1	
I_{SB1}	CMOS Standby Current, $\overline{CE}_1 \geq V_{CC} - 0.2V, CE_2 \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V, V_{CC} = \text{Max.}, f = 0$	L	20	30	μA
		LL	10	15	

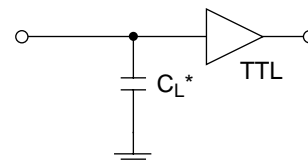
NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -3.0V for pulse width < $t_{RC}/2$.
3. $f_{MAX} = 1/t_{RC}$.

AC Test Conditions

Input Pulse Levels	0 to 2.0V
Input Rise and Fall Times	5 ns
Timing Reference Levels	1.1V
Output Load	see below

AC Test Loads and Waveforms



$$C_L = 30pF + 1TTL \text{ Load}$$

* Includes scope and jig capacitance

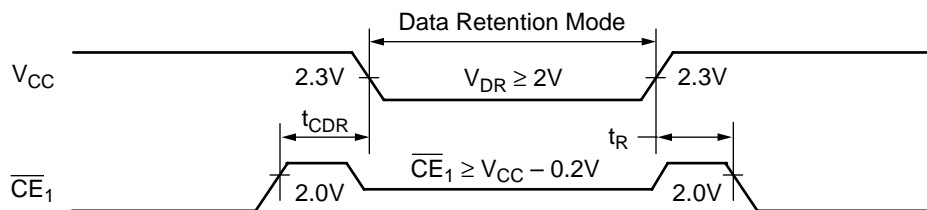
Data Retention Characteristics

Symbol	Parameter	Power	Min.	Typ. ⁽²⁾	Max.	Units	
V_{DR}	V_{CC} for Data Retention $CE_1 \geq V_{CC} - 0.2V$, $CE_2 < 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$		1.5	—	2.8	V	
I_{CCDR}	Data Retention Current $CE_1 \geq V_{DR} - 0.2V$, $CE_2 < 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	Com'l	L	—	1	3	μA
			LL	—	0.5	2	
		Ind.	L	—	—	5	
			LL	—	—	4	
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns	
t_R	Operation Recovery Time (see Retention Waveform)		$t_{RC}^{(1)}$	—	—	ns	

NOTES:

- t_{RC} = Read Cycle Time
- $T_A = +25^\circ C$.

Low V_{CC} Data Retention Waveform (1) (\overline{CE}_1 Controlled)



Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

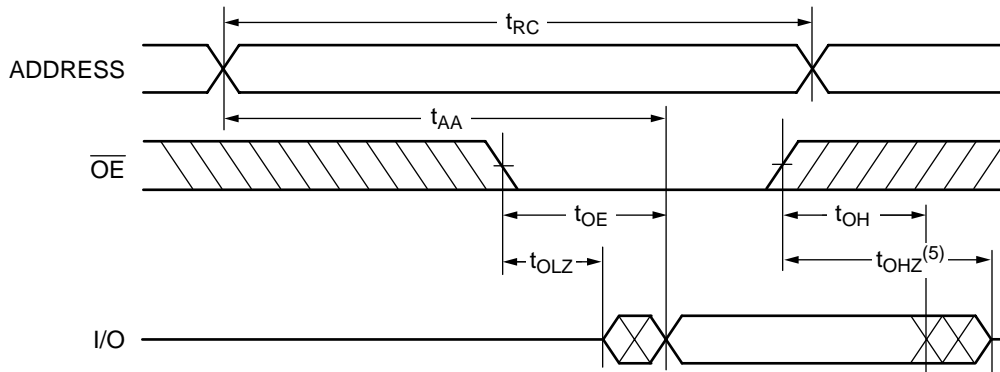
Parameter Name	Parameter	-55		-70		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{ACS1}	Chip Enable Access Time	—	55	—	70	ns
t_{ACS2}	Chip Enable Access Time	—	55	—	70	ns
t_{OE}	Output Enable to Output Valid	—	55	—	40	ns
t_{CLZ1}	Chip Enable to Output in Low Z	10	—	10	—	ns
t_{CLZ2}	Chip Enable to Output in Low Z	10	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	ns
t_{CHZ}	Chip Disable to Output in High Z	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z	—	25	—	25	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	ns

Write Cycle

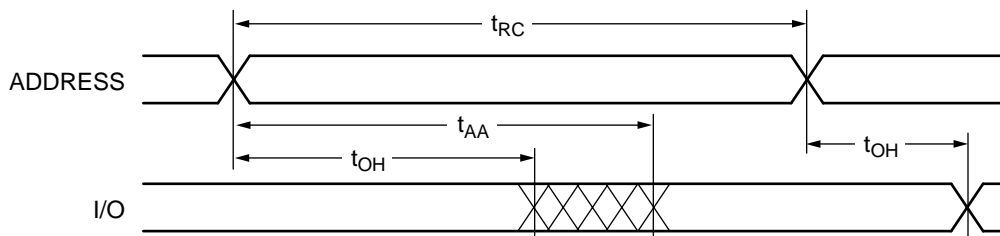
Parameter Name	Parameter	-55		-70		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{CW1}	Chip Enable to End of Write	45	—	60	—	ns
t_{CW2}	Chip Enable to End of Write	45	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	45	—	60	—	ns
t_{WP}	Write Pulse Width	45	—	50	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	ns
t_{WHZ}	Write to Output High-Z	—	25	—	30	ns
t_{DW}	Data Setup to End of Write	30	—	40	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High-Z	—	25	—	30	ns

Switching Waveforms (Read Cycle)

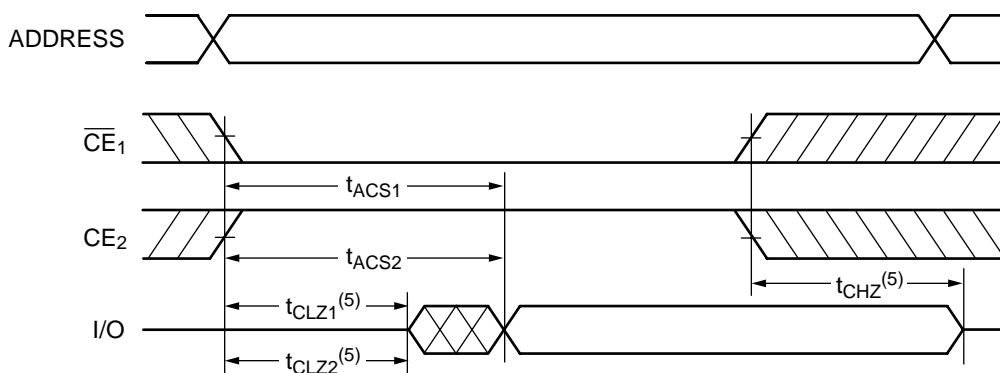
Read Cycle 1^(1, 2, 6)



Read Cycle 2^(1, 2, 4, 6)



Read Cycle 3^(1, 3, 4, 6)

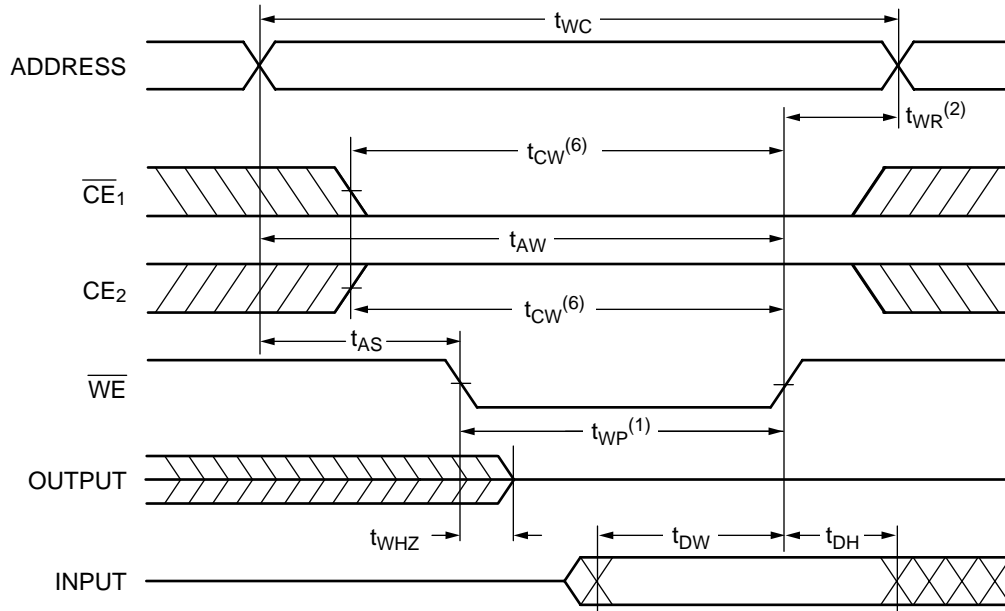


NOTES:

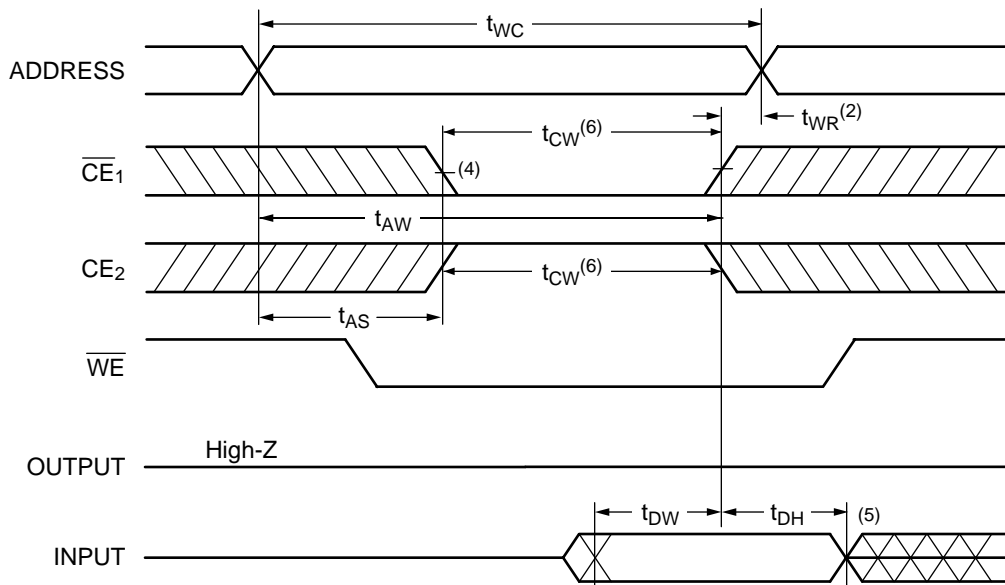
1. $\overline{WE} = V_{IH}$.
2. $\overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$.
3. Address valid prior to or coincident with \overline{CE}_1 transition LOW and/or CE_2 transition HIGH.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500mV$ from steady state with $C_L = 5pF$. This parameter is guaranteed and not 100% tested.
6. CE_2 is offered on BGA package only.

Switching Waveforms (Write Cycle)

Write Cycle 1 (\overline{WE} Controlled)^(4, 7)



Write Cycle 2 (CE Controlled)^(4, 7)



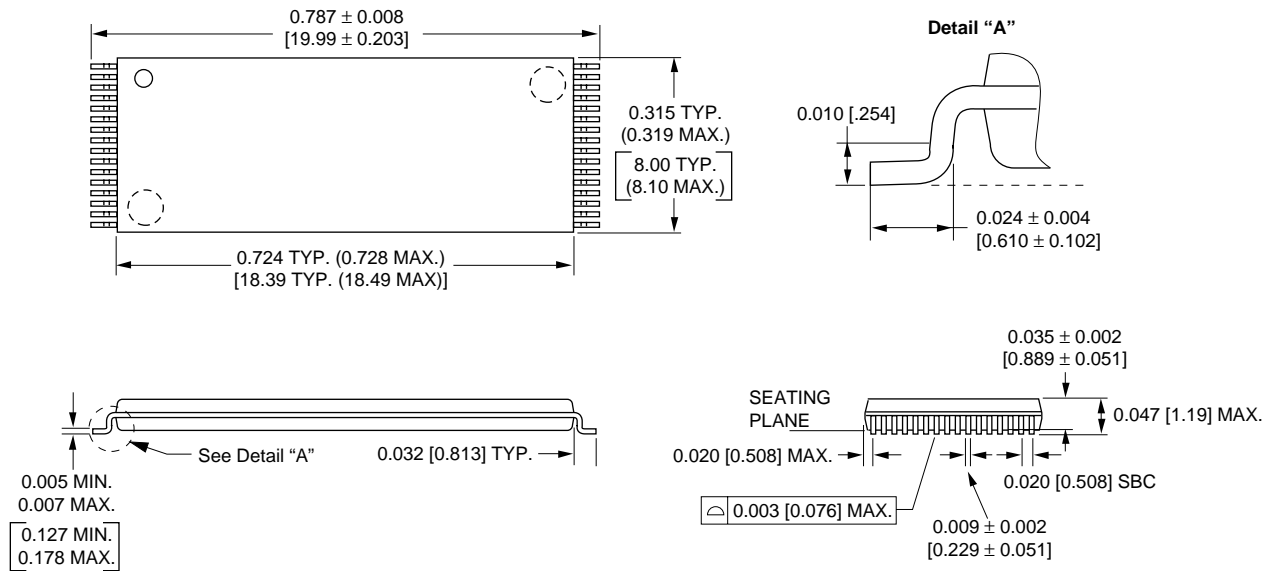
NOTES:

1. The internal write time of the memory is defined by the overlap of \overline{CE}_1 and CE_2 active and \overline{WE} low. All signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{WR} is measured from the earlier of \overline{CE}_1 or \overline{WE} going high, or CE_2 going LOW at the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE} = V_{IL}$ or V_{IH} . However it is recommended to keep \overline{OE} at V_{IH} during write cycle to avoid bus contention.
5. If \overline{CE}_1 is LOW and CE_2 is HIGH during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from \overline{CE}_1 going low or CE_2 going HIGH to the end of write.
7. CE_2 is offered on BGA package only.

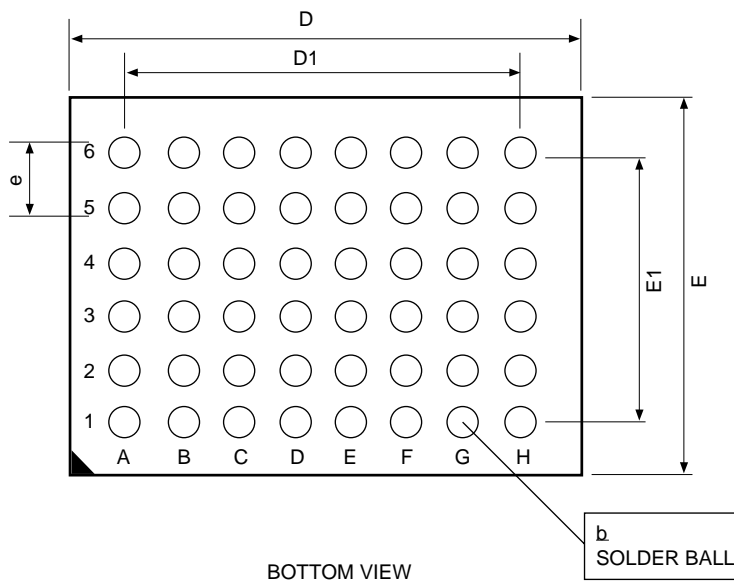
Package Diagrams

32-Pin TSOP (Standard)

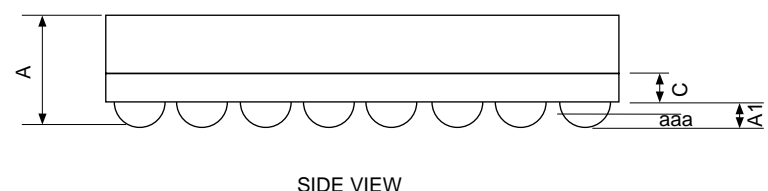
Units in inches [mm]



48 Ball—8x10 fpBGA



SYMBOL	UNIT.MM
A	1.05+0.15
A1	0.25±0.05
b	0.35±0.05
c	0.30(TYP)
D	10.00±0.10
D1	5.25
E	8.00±0.10
E1	3.75
e	0.75TYP
aaa	0.10



U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

HONG KONG

19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 852-2666-3307
FAX: 852-2770-8011

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

NO 19 LI HSIN RD.
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-579-5888
FAX: 886-3-566-5888

SINGAPORE

10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-3231801
FAX: 65-3237013

JAPAN

WBG MARIVE WEST 25F
6, NAKASE 2-CHOME
MIHAMA-KU, CHIBA-SHI
CHIBA 261-7125
PHONE: 81-43-299-6000
FAX: 81-43-299-6555

UK & IRELAND

SUITE 50, GROVEWOOD
BUSINESS CENTRE
STRATHCLYDE BUSINESS
PARK
BELLSHILL, LANARKSHIRE,
SCOTLAND, ML4 3NQ
PHONE: 01698-748515
FAX: 01698-748516

**GERMANY
(CONTINENTAL
EUROPE & ISRAEL)**

71083 HERRENBERG
BENZSTR. 32
GERMANY
PHONE: +49 7032 2796-0
FAX: +49 7032 2796 22

U.S. SALES OFFICES**NORTHWESTERN**

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

SOUTHWESTERN

302 N. EL CAMINO REAL #200
SAN CLEMENTE, CA 92672
PHONE: 949-361-7873
FAX: 949-361-7807

**CENTRAL,
NORTHEASTERN &
SOUTHEASTERN**

604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 972-690-1402
FAX: 972-690-0341

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.