



# AH5009/AH5010/AH5011/AH5012 Monolithic Analog Current Switches

## General Description

A versatile family of monolithic JFET analog switches economically fulfills a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

## Applications

- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition

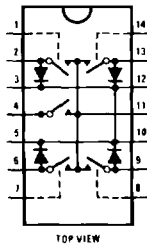
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

## Features

- Interfaces with standard TTL and CMOS
- "ON" resistance match 2Ω
- Low "ON" resistance 100Ω
- Very low leakage 50 pA
- Large analog signal range ± 10V peak
- High switching speed 150 ns
- Excellent isolation between channels 80 dB at 1 kHz

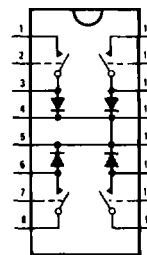
## Connection and Schematic Diagrams (All switches shown are for logical "1" input)

Dual-In-Line Package



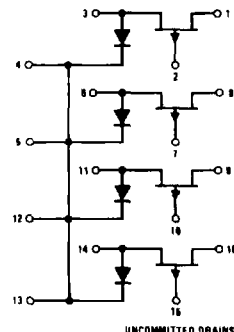
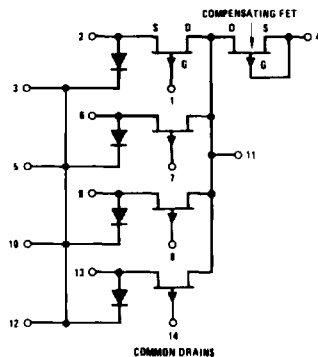
LOGIC DRIVE	4 CHANNEL MUX	4 SPST SWITCHES
5V LOGIC	AH5010C	AH5012C
15V LOGIC	AH5009C	AH5011C

Dual-In-Line Package



**AH5009C and AH5010C MUX Switches**  
 (4-Channel Version Shown)  
 Order Number AH5009CM,  
 AH5009CN, AH5010CM or AH5010CN  
 See NS Package Number M14A or N14A

**AH5011C and AH5012C SPST Switches**  
 (Quad Version Shown)  
 Order Number AH5011CM,  
 AH5011CN, AH5012CM or AH5012CN  
 See NS Package Number M16A or N16A



Note: All diode cathodes are internally connected to the substrate.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage AH5009/AH5010/AH5011/AH5012	30V	Drain Current	30 mA
Positive Analog Signal Voltage	30V	Soldering Information:	
Negative Analog Signal Voltage	- 15V	N Package 10 sec	300°C
Diode Current	10 mA	SO Package Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
		Power Dissipation	500 mW
		Operating Temperature Range	- 25°C to + 85°C
		Storage Temperature Range	- 65°C to + 150°C

### Electrical Characteristics AH5010 and AH5012 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I <sub>GSX</sub>	Input Current "OFF"	4.5V ≤ V <sub>GD</sub> ≤ 11V, V <sub>SD</sub> = 0.7V T <sub>A</sub> = 85°C	0.01	0.2 10	nA nA
I <sub>D(OFF)</sub>	Leakage Current "OFF"	V <sub>SD</sub> = 0.7V, V <sub>GS</sub> = 3.8V T <sub>A</sub> = 85°C	0.02	0.2 10	nA nA
I <sub>G(ON)</sub>	Leakage Current "ON"	V <sub>GD</sub> = 0V, I <sub>S</sub> = 1 mA T <sub>A</sub> = 85°C	0.08	1 200	nA nA
I <sub>G(ON)</sub>	Leakage Current "ON"	V <sub>GD</sub> = 0V, I <sub>S</sub> = 2 mA T <sub>A</sub> = 85°C	0.13	5 10	nA μA
I <sub>G(ON)</sub>	Leakage Current "ON"	V <sub>GD</sub> = 0V, I <sub>S</sub> = - 2 mA T <sub>A</sub> = 85°C	0.1	10 20	nA μA
r <sub>DS(ON)</sub>	Drain-Source Resistance	V <sub>GS</sub> = 0.35V, I <sub>S</sub> = 2 mA T <sub>A</sub> = + 85°C	90	150 240	Ω Ω
V <sub>DIODE</sub>	Forward Diode Drop	I <sub>D</sub> = 0.5 mA		0.8	V
r <sub>DS(ON)</sub>	Match	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1 mA	4	20	Ω
T <sub>ON</sub>	Turn "ON" Time	See AC Test Circuit	150	500	ns
T <sub>OFF</sub>	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit	120		dB

### Electrical Characteristics AH5009 and AH5011 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I <sub>GSX</sub>	Input Current "OFF"	11V ≤ V <sub>GD</sub> ≤ 15V, V <sub>SD</sub> = 0.7V T <sub>A</sub> = 85°C	0.01	0.2 10	nA nA
I <sub>D(OFF)</sub>	Leakage Current "OFF"	V <sub>SD</sub> = 0.7V, V <sub>GS</sub> = 10.3V T <sub>A</sub> = 85°C	0.01	0.2 10	nA nA
I <sub>G(ON)</sub>	Leakage Current "ON"	V <sub>GD</sub> = 0V, I <sub>S</sub> = 1 mA T <sub>A</sub> = 85°C	0.04	0.5 100	nA nA
I <sub>G(ON)</sub>	Leakage Current "ON"	V <sub>GD</sub> = 0V, I <sub>S</sub> = 2 mA T <sub>A</sub> = 85°C		2 1	nA μA
I <sub>G(ON)</sub>	Leakage Current "ON"	V <sub>GD</sub> = 0V, I <sub>S</sub> = - 2 mA T <sub>A</sub> = 85°C		5 2	nA μA
r <sub>DS(ON)</sub>	Drain-Source Resistance	V <sub>GS</sub> = 1.5V, I <sub>S</sub> = 2 mA T <sub>A</sub> = 85°C	60	100 160	Ω Ω
V <sub>DIODE</sub>	Forward Diode Drop	I <sub>D</sub> = 0.5 mA		0.8	V
r <sub>DS(ON)</sub>	Match	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1 mA	2	10	Ω
T <sub>ON</sub>	Turn "ON" Time	See AC Test Circuit	150	50	ns
T <sub>OFF</sub>	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit. f = 100 Hz.	120		dB

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

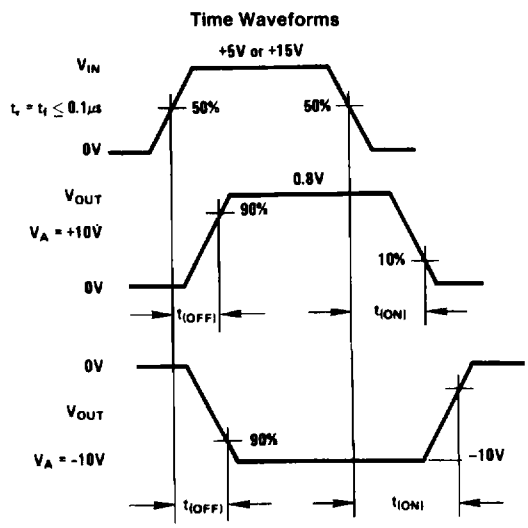
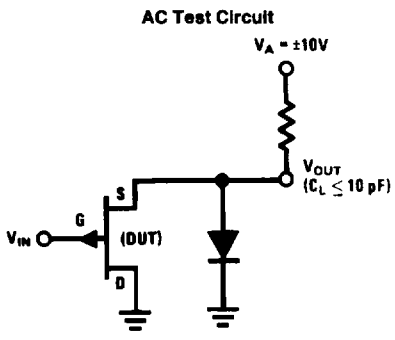
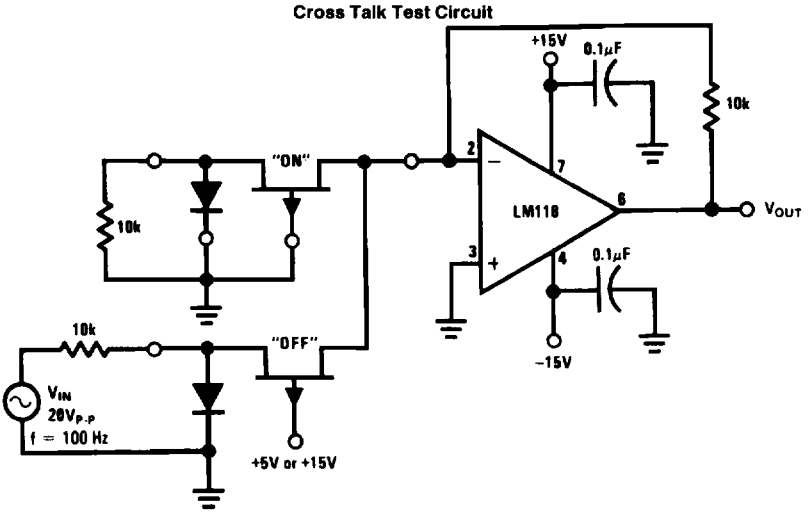
**Note 2:** Test conditions 25°C unless otherwise noted.

**Note 3:** "OFF" and "ON" notation refers to the conduction state of the FET switch.

**Note 4:** Thermal Resistance:

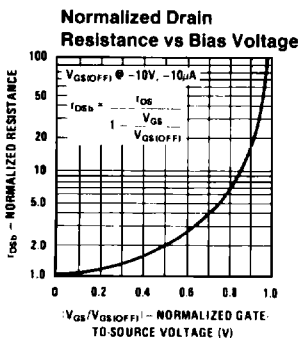
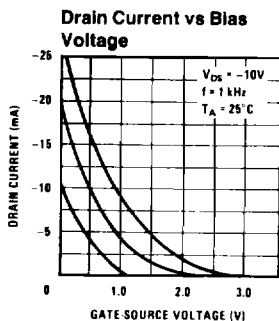
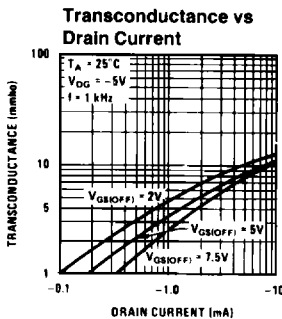
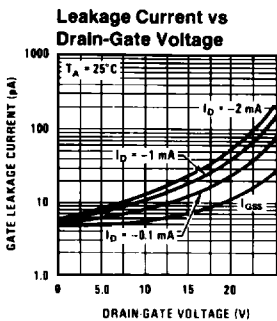
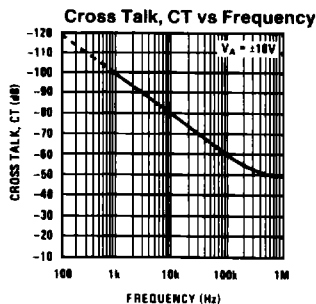
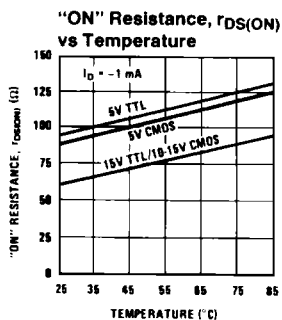
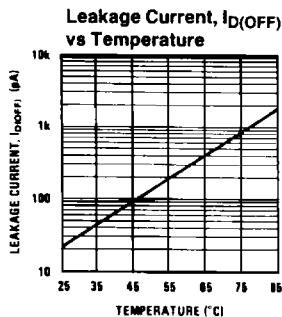
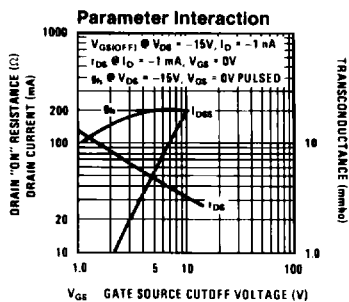
N14A, N16A	$\theta_{JA}$
M14A, M16A	92°C/W
	115°C/W

**Test Circuits and Switching Time Waveforms**



TL/H/5659-2

## Typical Performance Characteristics



# Applications Information

## Theory of Operation

The AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AH5010), 5V-10V CMOS (AH5010), open collector 15V TTL/CMOS (AH5009).

Two basic switch configurations are available: 4 independent switches (SPST) and 4 pole switches used for multiplexing (4 PST-MUX). The MUX versions such as the AH5009 offer common drains and include a series FET operated at  $V_{GS} = 0V$ . The additional FET is placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R_2 + r_{DS(ON)Q2}}{R_1 + r_{DS(ON)Q1}}$$

For  $R_1 = R_2$ , gain accuracy is determined by the  $r_{DS(ON)}$  match between  $Q_1$  and  $Q_2$ . Typical match between  $Q_1$  and  $Q_2$  is 4 ohms resulting in a gain accuracy of 0.05% (for  $R_1 = R_2 = 10\text{ k}\Omega$ ).

## Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the

"OFF" state. With  $V_{IN} = 15V$  and the  $V_A = 10V$ , the source of  $Q_1$  is clamped to about 0.7V by the diode ( $V_{GS} = 14.3V$ ) ensuring that ac signals imposed on the 10V input will not gate the FET "ON."

## Selection of Gain Setting Resistors

Since the AH series of analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*,  $I_{G(ON)}$  represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the  $r_{DS(ON)}$  of the FET begins to "round" as  $I_S$  approaches  $I_{DSS}$ . A practical rule of thumb is to maintain  $I_S$  at less than  $1/10$  of  $I_{DSS}$ .

Combining the criteria from the above discussion yields:

$$R_{1min} \geq \frac{V_A(MAX) A_D}{I_{G(ON)}} \tag{2a}$$

or:

$$\geq \frac{V_A(MAX)}{I_{DSS}/10} \tag{2b}$$

whichever is larger.

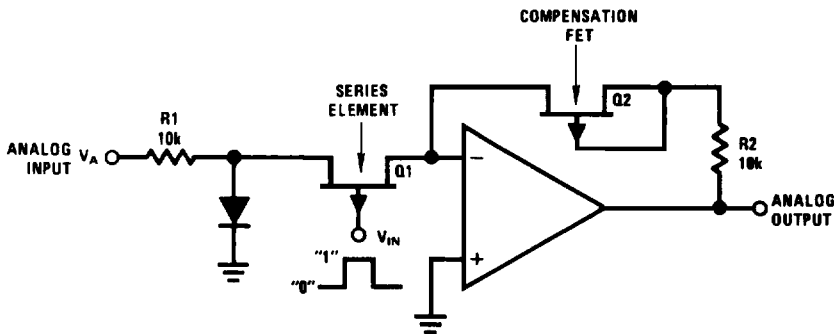


FIGURE 1. Use of Compensation FET

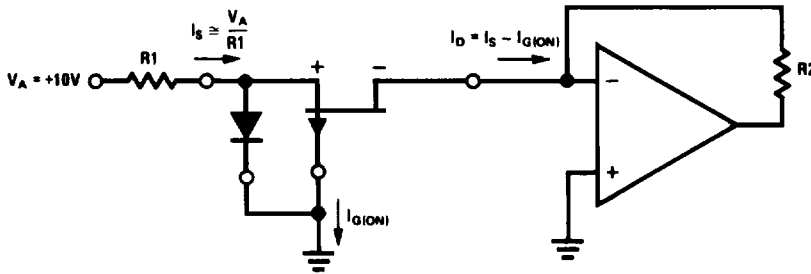


FIGURE 2. On Leakage Current,  $I_{G(ON)}$

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## Applications Information (Continued)

- Where:  $V_{A(MAX)}$  = Peak amplitude of the analog input signal  
 $A_D$  = Desired accuracy  
 $I_{G(ON)}$  = Leakage at a given  $I_S$   
 $I_{DSS}$  = Saturation current of the FET switch  
 $\approx 20 \text{ mA}$

In a typical application,  $V_A$  might =  $\pm 10V$ ,  $A_D = 0.1\%$ ,  $0^\circ C \leq T_A \leq 85^\circ C$ . The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{(10V)}{\left(\frac{20 \text{ mA}}{10}\right)} = 5 \text{ k}\Omega$$

For  $R1 = 5k$ ,  $I_S \approx 10V/5k$  or 2 mA. The electrical characteristics guarantee an  $I_{G(ON)} \leq 1 \mu A$  at  $85^\circ C$  for the AH5010. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10 \text{ k}\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in Figure 3, the leakage across Q2,  $I_{D(OFF)}$  represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)} A_D}{(N) I_{D(OFF)}}$$

- Where:  $V_{A(MIN)}$  = Minimum value of the analog input signal  
 $A_D$  = Desired accuracy  
 $N$  = Number of channels  
 $I_{D(OFF)}$  = "OFF" leakage of a given FET switch

As an example, if  $N = 10$ ,  $A_D = 0.1\%$ , and  $I_{D(OFF)} \leq 10 \text{ nA}$  at  $85^\circ C$  for the AH5009.  $R1_{(MAX)}$  is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of  $R2$ , of course, depends on the gain desired and for unity gain  $R1 = R2$ .

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

### TTL Compatibility

The AH series can be driven with two different logic voltage swings: the even numbered part types are specified to be driven from standard 5V TTL logic and the odd numbered types from 15V open collector TTL.

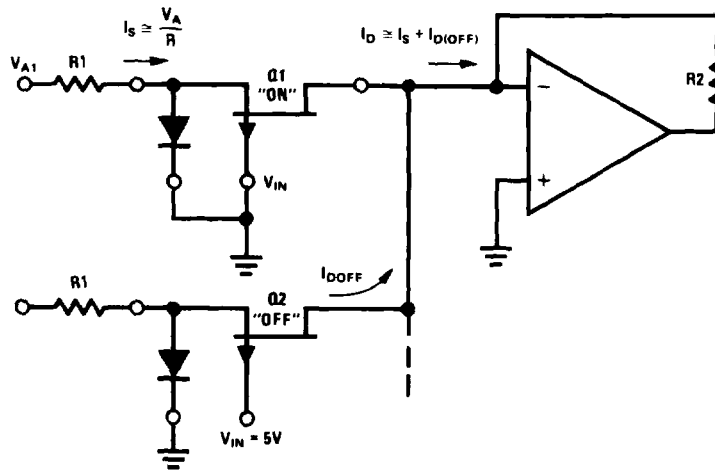


FIGURE 3

TL/H/5659-5

### Applications Information (Continued)

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor,  $R_{EXT}$ , of at least 10 k $\Omega$  should be placed between the 5V  $V_{CC}$  and the gate output as shown in Figure 4.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in Figure 5. In

both cases,  $t_{(OFF)}$  is improved for lower values of  $R_{EXT}$  at the expense of power dissipation in the low state.

#### Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in Figure 6.

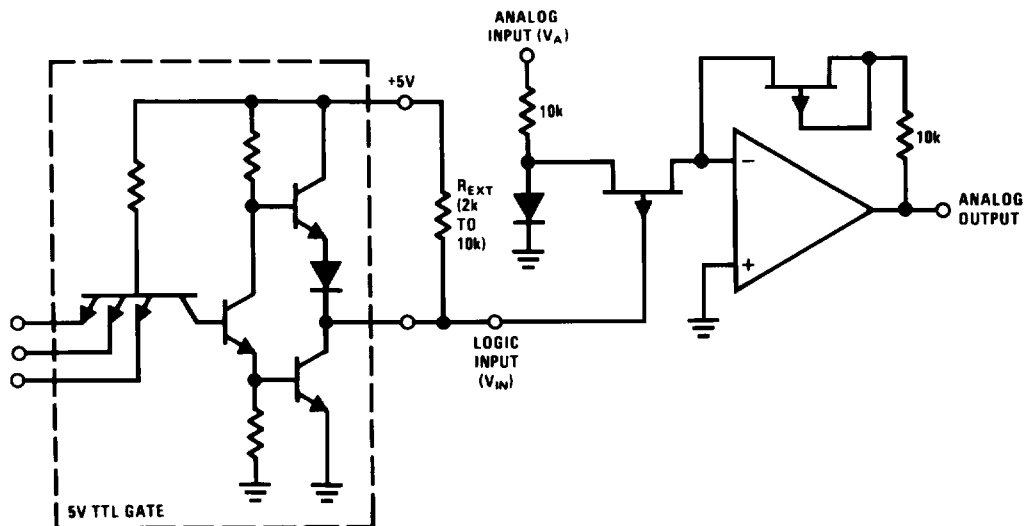


FIGURE 4. Interfacing with +5V TTL

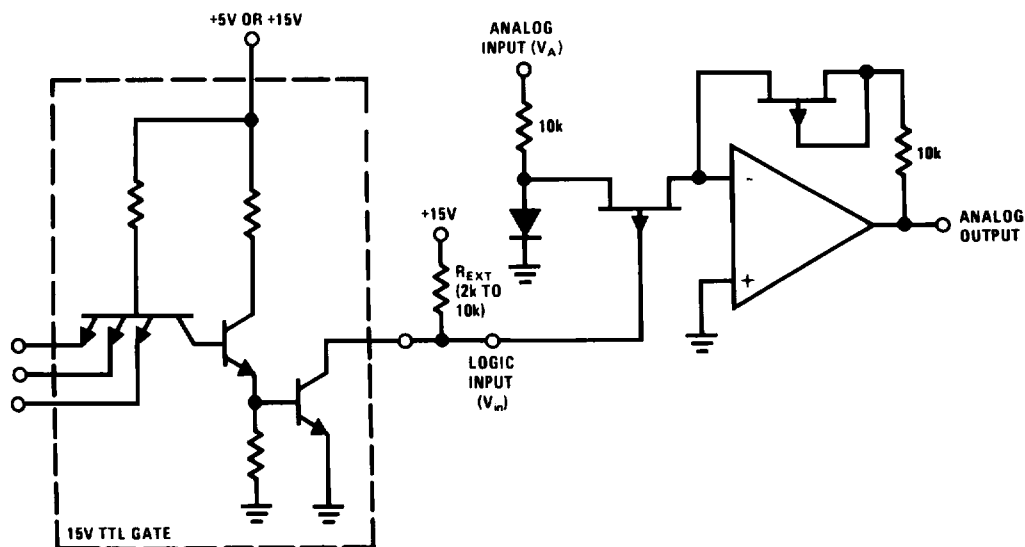


FIGURE 5. Interfacing with +15V Open Collector TTL

TL/H/5659-6

Applications Information (Continued)

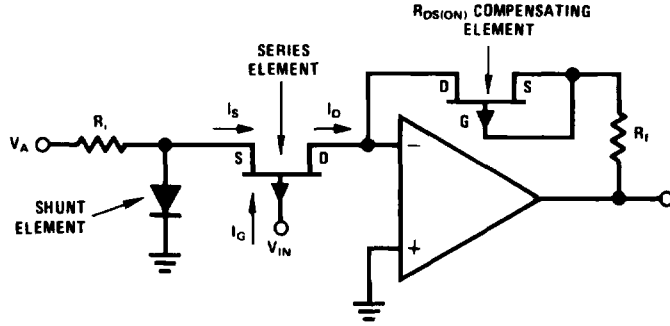
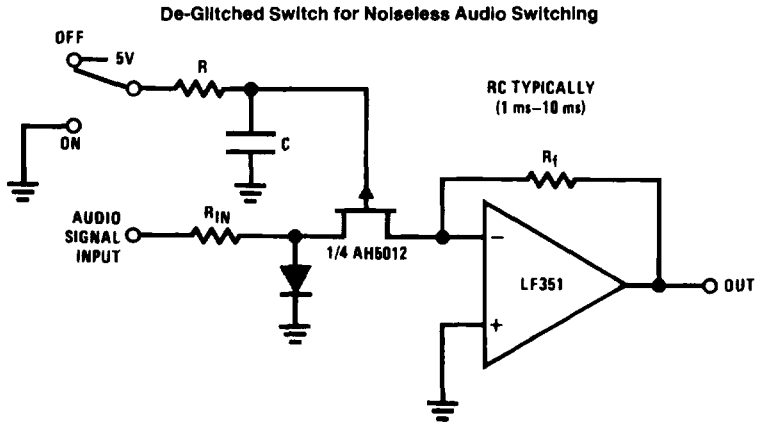


FIGURE 6. Definition of Terms

Typical Applications

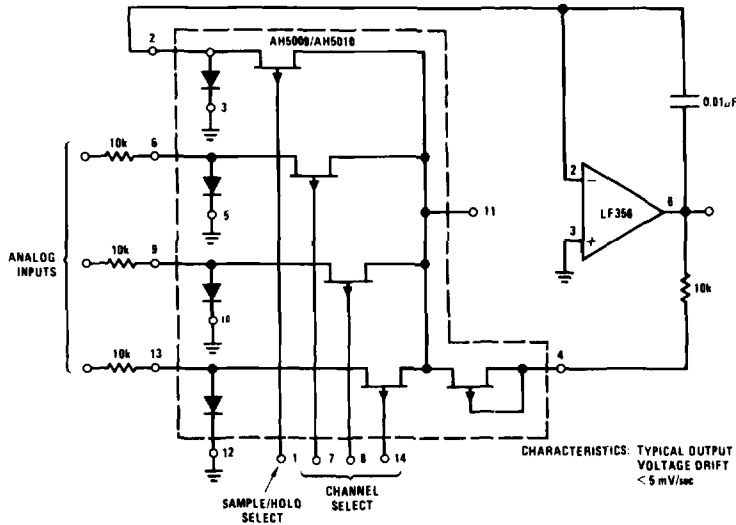


TL/H/5859-7

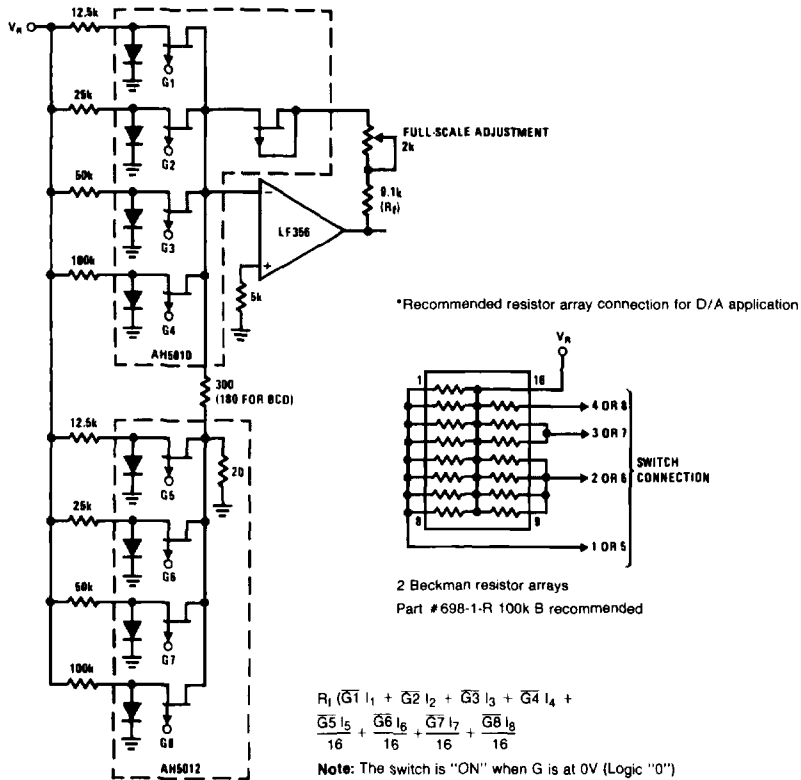


Typical Applications (Continued)

3-Channel Multiplexer with Sample and Hold



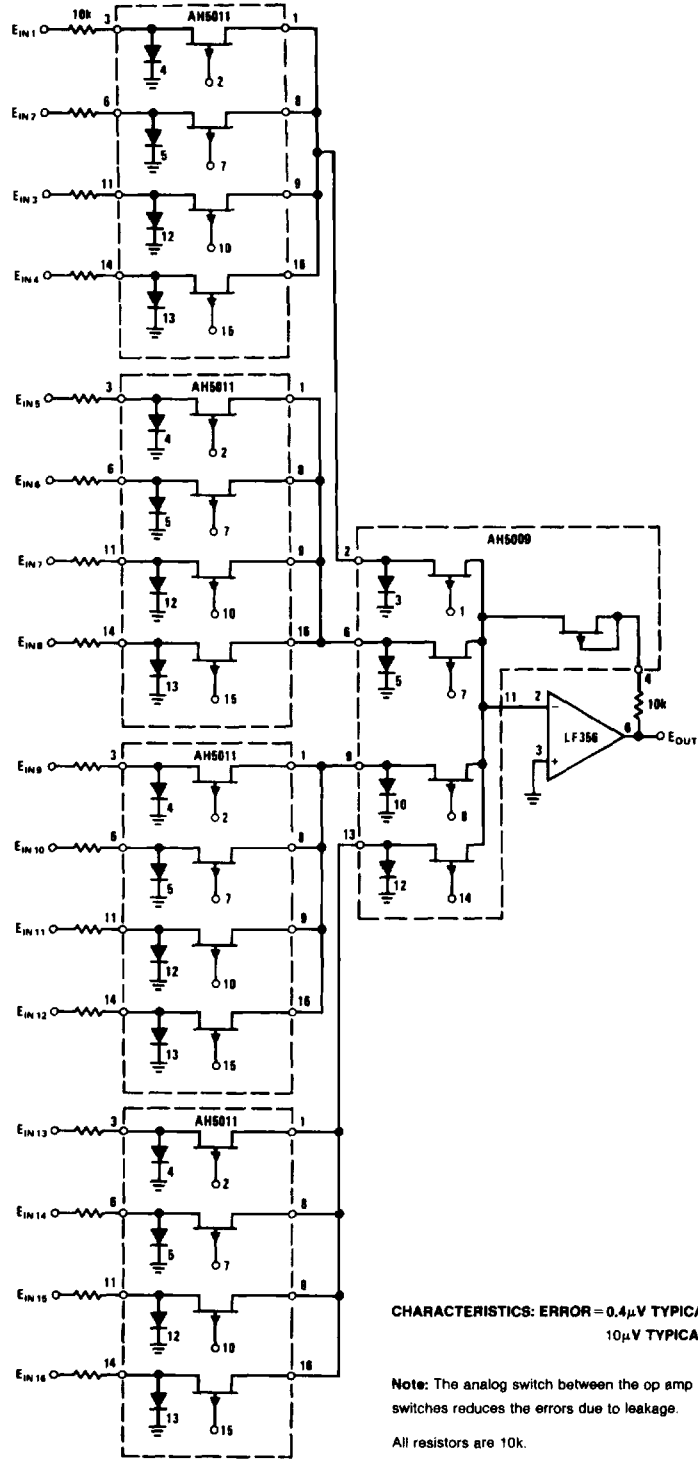
8-Bit Binary (BCD) Multiplying D/A Converter\*



2

TL/H/5659-8

**Typical Applications (Continued) 16-Channel Multiplexer**



**CHARACTERISTICS: ERROR = 0.4 $\mu$ V TYPICAL @ 25°C  
10 $\mu$ V TYPICAL @ 70°C**

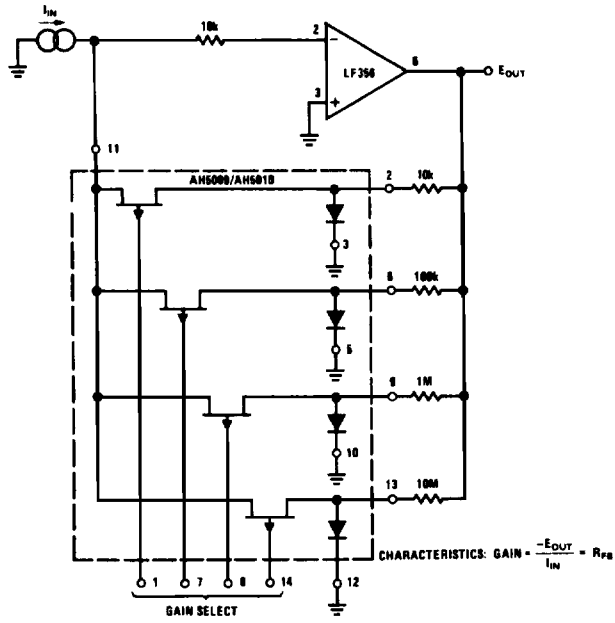
**Note:** The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k.

TL/H/5659-9

Typical Applications (Continued)

Gain Programmable Amplifier



TL/H/5659-10