CY2276-2
CY2276-3
CY2276-4

PRELIMINARY

Pentium II™ Clock Synthesizer/Driver for Intel 82440LX Chipset with 3 or 4 DIMM and USB/IO Support

Features

- **Mixed 2.5V and 3.3V operation**
- **Single-chip clock solution to meet requirements of Pentium II™ motherboards**
  - **Multiple CPU clocks at 2.5V**
  - **Seven synchronous PCI clocks, one free-running**
  - **Multiple 2.5V IOAPIC clocks at 14.318 MHz**
  - **Multiple 3.3V SDRAM clocks**
  - **Multiple 3.3V USB and I/O clocks**
  - **Multiple 3.3V Ref. clocks at 14.318 MHz**
- **1 ns–4 ns CPU-PCI delay, factory-EPROM programmable**
- **I²C™ Serial Configuration Interface**
- **Ability to stop CPU clocks (-3 and -4)**
- **Factory-EPROM programmable output drive and slew rate for optimal EMI control. Improved output drivers are designed for low EMI.**
- **Factory-EPROM programmable clock frequencies for custom configurations**
- **Low CPU clock jitter ≤ 250 ps cycle-cycle.**
- **Low skew outputs**
- **Available in space-saving 56-pin SSOP package**

Functional Description

The CY2276-2, CY2276-3, and CY2276-4 are single-chip clock generators for the Pentium II. They differ in the number of outputs available from each device, as shown in the Selector Guide.

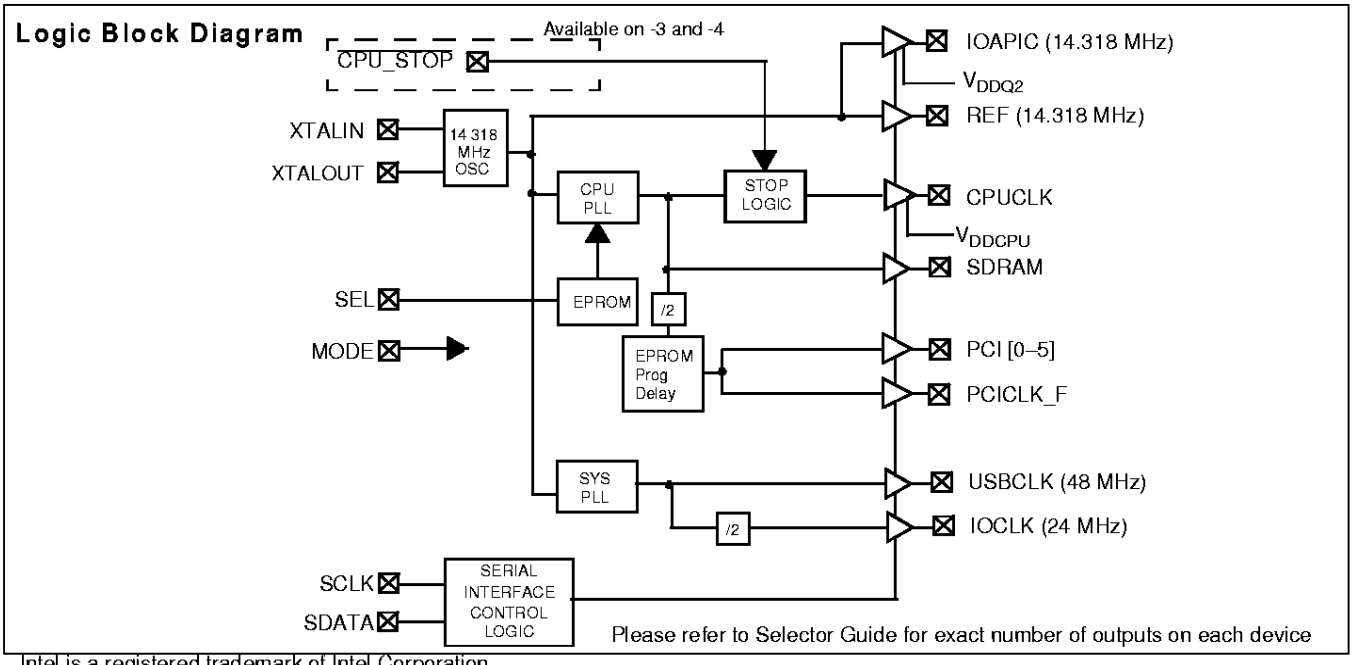
The CY2276-2 is ideal for four-SDRAM module or server applications that require sixteen SDRAM clocks, and do not require the ability to stop CPU clocks. The CY2276-3 is ideal for single-processor or dual processor desktop systems, which require an extra CPU clock. Finally, the CY2276-4 is ideally for desktop systems that use newer I/O devices requiring a 48-MHz reference clock.

All the output clocks meet Intel's jitter, accuracy, rise, and fall time requirements. All outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative layout techniques enable these devices to have lower EMI than those from other manufacturers. Finally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations for EMI control.

Selector Guide

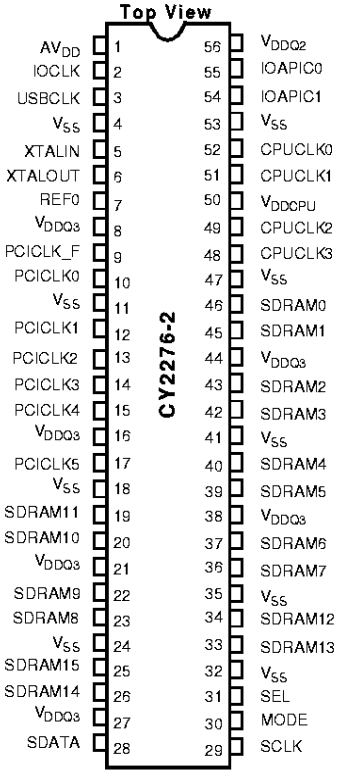
Clocks	CY2276-2 # Outputs	CY2276-3 # Outputs	CY2276-4 # Outputs
CPU	4	5	4
PCI	7	7	7
SDRAM	16	13	12
IOAPIC	2	2	2
48 MHz	1	2	3
24 MHz	1	0	0
Ref.	1	2	3

Logic Block Diagram

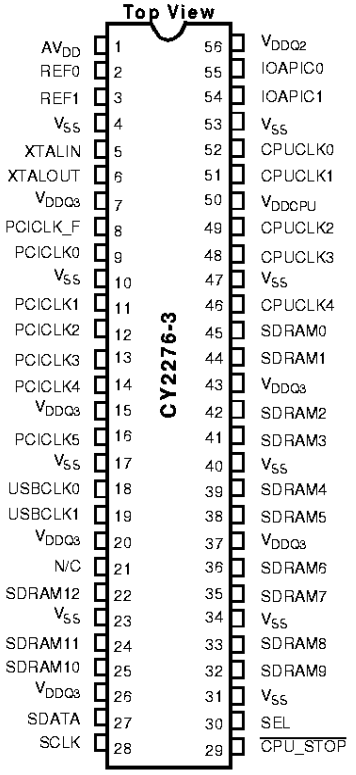


Pin Configurations

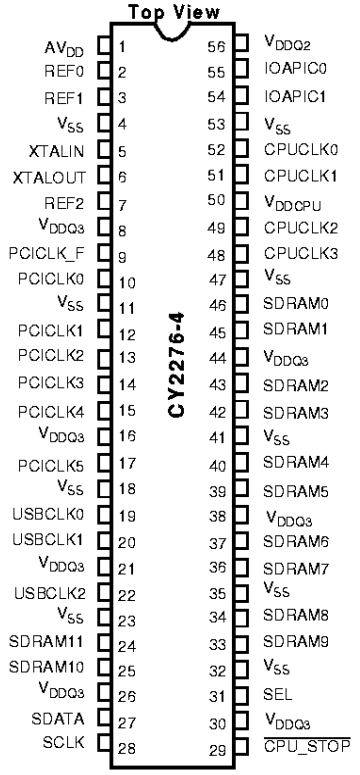
SSOP
Top View



SSOP
Top View



SSOP
Top View



Pin Summary

Name	Pins (-2)	Pins (-3)	Pins (-4)	Description
V_{DDQ3}	8, 16, 21, 27, 38, 44	7, 15, 20, 26, 37, 43	8, 16, 21, 26, 30, 38, 44	3.3V Digital voltage supply
V_{DDQ2}	56	56	56	IOAPIC Digital voltage supply, 2.5V
V_{DDCPU}	50	50	50	CPU Digital voltage supply, 2.5V
AV_{DD}	1	1	1	Analog voltage supply, 3.3V
V_{SS}	4, 11, 18, 24, 32, 35, 41, 47, 53	4, 10, 17, 23, 31, 34, 40, 47, 53	4, 11, 18, 23, 32, 35, 41, 47, 53	Ground
XTALIN[1]	5	5	5	Reference crystal input
XTALOUT[1]	6	6	6	Reference crystal feedback
SDRAM[0-15] *(-2)* SDRAM [0-12] *(-3)* SDRAM [0-11] *(-4)*	46, 45, 43, 42, 40, 39, 37, 36, 23, 22, 20, 19, 34, 33, 26, 25	45, 44, 42, 41, 39, 38, 36, 35, 33, 32, 25, 24, 22	46, 45, 43, 42, 40, 39, 37, 36, 34, 33, 25, 24	SDRAM clock outputs
SEL	31	30	31	CPU frequency select input (See table below.)
CPUCLK [0-3] *(-2)* CPUCLK [0-4] *(-3)* CPUCLK [0-3] *(-4)*	52, 51, 49, 48	52, 51, 49, 48, 46	52, 51, 49, 48	CPU clock outputs
PCICLK [0-5] *(All)*	10, 12, 13, 14, 15, 17	9, 11, 12, 13, 14, 16	10, 12, 13, 14, 15, 17	PCI clock outputs, running at one-half the CPU frequency
PCICLK_F *(All)*	9	8	9	Free-running PCI clock output
IOAPIC [0-1] *(All)*	55, 54	55, 54	55, 54	IOAPIC clock outputs
REF0 *(-2)* REF [0-1] *(-3)* REF [0-2] *(-4)*	7	2, 3	2, 3, 7	Reference clock outputs, 14.318 MHz. REF0 drives 45 pF load
USBCLK *(-2)* USBCLK [0-1] *(-3)* USBCLK [0-2] *(-4)*	3	18, 19	19, 20, 22	48 MHz USB clock output.
IOCLK	2	N/A	N/A	24 MHz I/O clock output
SDATA	28	27	27	Serial data input for serial configuration port
SCLK	29	28	28	Serial clock input for serial configuration port
$\overline{\text{CPU\_STOP}}$	N/A	29	29	Active LOW input, disables CPU clocks when asserted
MODE	30	N/A	N/A	Mode input, not used, tie to V_{SS}
N/C	N/A	21	N/A	Not connected. Tie to V_{SS}

Note:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Function Table

SEL	XTALIN	CPUCLK SDRAM	PCICLK PCICLK_F	REF IOAPIC
0	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz
1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	–195
CPUCLK	60.0	60.0	0

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0".
- I^2C Address for the CY2276-2,-3,-4 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Select Functions

Functional Description	Outputs				
	CPU	PCI, PCI_F	SDRAM	Ref	IOAPIC
Three-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2[2]	TCLK/4	TCLK/2	TCLK	TCLK

Note:
2. TCLK supplied on the XTALIN pin in Test Mode.

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)

Bit	Pin #	Description	
Bit 7	--	(Reserved) drive to '0'	
Bit 6	--	(Reserved) drive to '0'	
Bit 5	--	(Reserved) drive to '0'	
Bit 4	--	(Reserved) drive to '0'	
Bit 3	--	(Reserved) drive to '0'	
Bit 2	--	(Reserved) drive to '0'	
Bit 1 Bit 0	--	Bit 1 1 1 0 0	Bit 0 1 - Three-State 0 - N/A 1 - Testmode 0 - Normal Operation

Byte 1: CPU Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Description
Bit 7	IOCLK (Active/Inactive) (-2 ONLY) USBCLK0 (Active/Inactive) (-3 and -4 ONLY)
Bit 6	USBCLK (Active/Inactive) (-2 ONLY) USBCLK1 (Active/Inactive) (-3 and -4 ONLY)
Bit 5	USBCLk2 (Active/Inactive) (-4 ONLY)
Bit 4	CPUCLK4 (Active/Inactive) (-3 ONLY) Not available on -2 and -4
Bit 3	CPUCLK3 (Active/Inactive)
Bit 2	CPUCLK2 (Active/Inactive)
Bit 1	CPUCLK1 (Active/Inactive)
Bit 0	CPUCLK0 (Active/Inactive)

Byte 3: SDRAM Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Description
Bit 7	SDRAM7 (Active/Inactive)
Bit 6	SDRAM6 (Active/Inactive)
Bit 5	SDRAM5 (Active/Inactive)
Bit 4	SDRAM4 (Active/Inactive)
Bit 3	SDRAM3 (Active/Inactive)
Bit 2	SDRAM2 (Active/Inactive)
Bit 1	SDRAM1 (Active/Inactive)
Bit 0	SDRAM0 (Active/Inactive)

Byte 5: Peripheral Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Description
Bit 7	(Reserved drive to '0')
Bit 6	(Reserved) drive to '0'
Bit 5	IOAPIC1 (Active/Inactive)
Bit 4	IOAPIC0 (Active/Inactive)
Bit 3	(Reserved) drive to '0'
Bit 2	REF2 (Active/Inactive) (-4 only)
Bit 1	REF1 (Active/Inactive)(-3 and -4)
Bit 0	REF0 (Active/Inactive)

Byte 2: PCI Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Description
Bit 7	(Reserved) drive to '0'
Bit 6	PCICLK_F (Active/Inactive)
Bit 5	PCICLK5 (Active/Inactive)
Bit 4	PCICLK4 (Active/Inactive)
Bit 3	PCICLK3 (Active/Inactive)
Bit 2	PCICLK2 (Active/Inactive)
Bit 1	PCICLK1 (Active/Inactive)
Bit 0	PCICLK0 (Active/Inactive)

Byte 4: SDRAM Active/Inactive Register
(1 = Active, 0 = Inactive), Default = Active

Bit	Description
Bit 7	SDRAM15 (Active/Inactive) (-2 ONLY) Not available on -3 and -4
Bit 6	SDRAM14 (Active/Inactive) (-2 ONLY) Not available on -3 and -4
Bit 5	SDRAM13 (Active/Inactive) (-2 ONLY) Not available on -3 and -4
Bit 4	SDRAM12 (Active/Inactive) (-2 and -3) Not available on -4
Bit 3	SDRAM11 (Active/Inactive)
Bit 2	SDRAM10 (Active/Inactive)
Bit 1	SDRAM9 (Active/Inactive)
Bit 0	SDRAM8 (Active/Inactive)

Byte 6: Reserved, for future use

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDQ3}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.9	V
V_{DDQ2}	IOAPIC Supply Voltage	2.375	2.9	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK, USBCLK, IOCLK, REF[1:2], IOAPIC[0:1] PCICLK, SDRAM REF0	 10 30, 20 20	 20 30 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DDCPU} = 2.375V, V_{DDQ2} = 2.375V	I_{OH} = 16 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	IOAPIC			
V_{OL}	Low-level Output Voltage	V_{DDCPU} = 2.375V, V_{DDQ2} = 2.375V	I_{OL} = 27 mA	CPUCLK		0.4	V
			I_{OL} = 29 mA	IOAPIC			
V_{OH}	High-level Output Voltage	V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V	I_{OH} = 36 mA	SDRAM	2.4		V
			I_{OH} = 32 mA	PCICLK			
			I_{OH} = 36 mA	REF0			
V_{OL}	Low-level Output Voltage	V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V	I_{OL} = 29 mA	SDRAM		0.4V	V
			I_{OL} = 26 mA	PCICLK			
			I_{OL} = 29 mA	REF0			
I_{IH}	Input High Current	V_{IH} = V_{DD}			–5	+5	µA
I_{IL}	Input Low Current	V_{IL} = 0V				5	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current[4]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU clocks = 66.67 MHz				300	mA
I_{DD}	Power Supply Current[4]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				120	mA
I_{DDS}	Power-down Current	Current draw in power-down state				50	µA

Notes:

3. Electrical parameters are guaranteed with these operating conditions.
4. Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: TBD

Switching Characteristics[5] Over the Operating Range

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[6]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_{1C}	CPUCLK	CPU Clock HIGH Time	Above 2.0V, 66.6 MHz, V_{DDCPU} = 2.5V Above 2.0V, 60.0 MHz, V_{DDCPU} = 2.5V	5.2 6.0			ns
t_{1C}	PCICLK	PCI Clock HIGH Time	Above 2.4V, 33.3 MHz Above 2.4V, 30.0 MHz	12.0 13.3			ns
t_{1D}	CPUCLK	CPU Clock LOW Time	Below 0.4V, 66.6 MHz, V_{DDCPU} = 2.5V Below 0.4V, 60.0 MHz, V_{DDCPU} = 2.5V	5.0 5.8			ns
t_{1D}	PCICLK	PCI Clock LOW Time	Below 0.4V, 33.3 MHz Below 0.4V, 30.0 MHz	12.0 13.3			ns
t_2	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	1.0		4.0	V/ns
t_2	PCICLK, REF0	PCI, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	SDRAM	SDRAM Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.5		4.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V	0.4		1.6	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V_{DDCPU} = 2.5V	0.4		1.6	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V_{DDCPU} = 2.5V		100	250	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.5	4.0	ns
t_7	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			500	ps
t_8	CPUCLK, SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			250	ps
t_8	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t_9	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabilization from power-up			3	ms

Notes:

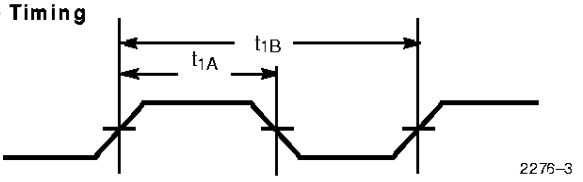
5. All parameters specified with loaded outputs.
6. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DDCPU} = 2.5V, CPUCLK duty cycle is measured at 1.25V.

Timing Requirement for the I²C Bus

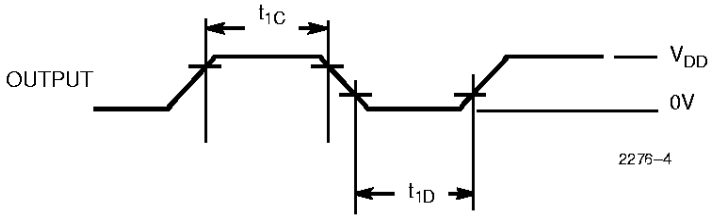
Parameter	Description	Min.	Max.	Unit
t_{10}	SCLK Clock Frequency	0	100	kHz
t_{11}	Time the bus must be free before a new transmission can start	4.7		µs
t_{12}	Hold time start condition. After this period the first clock pulse is generated.	4		µs
t_{13}	The Low period of the clock.	4.7		µs
t_{14}	The High period of the clock.	4		µs
t_{15}	Setup time for start condition. (Only relevant for a repeated start condition.)	4.7		µs
t_{16}	Hold time DATA for CBUS compatible masters. for I²C devices	 5 0		µs
t_{17}	DATA input setup time	250		ns
t_{18}	Rise time of both SDATA and SCLK inputs		1	µs
t_{19}	Fall time of both SDATA and SCLK inputs		300	ns
t_{20}	Setup time for stop condition	4.0		µs

Switching Waveforms

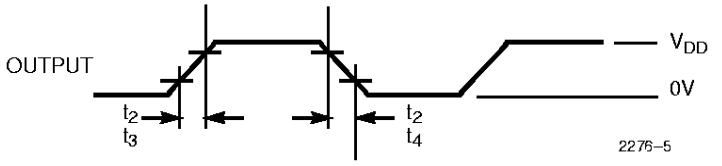
Duty Cycle Timing



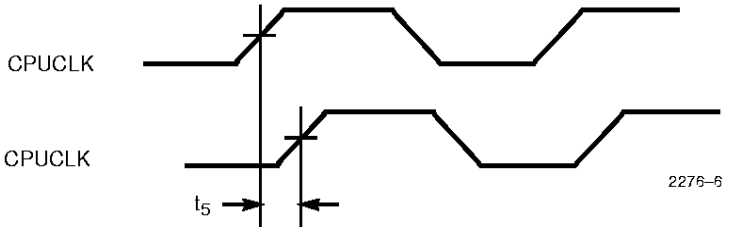
CPUCLK Outputs HIGH/LOW Time



All Outputs Rise/Fall Time

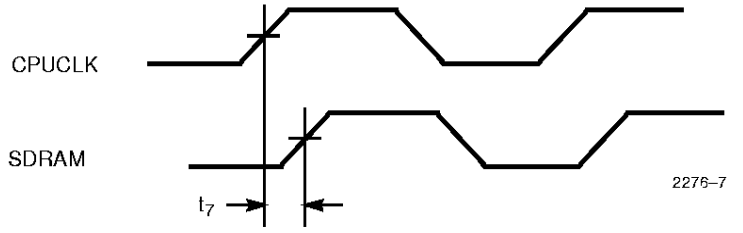


CPU-CPU Clock Skew

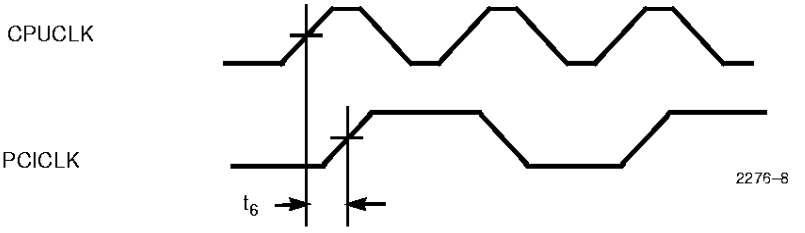


Switching Waveforms (continued)

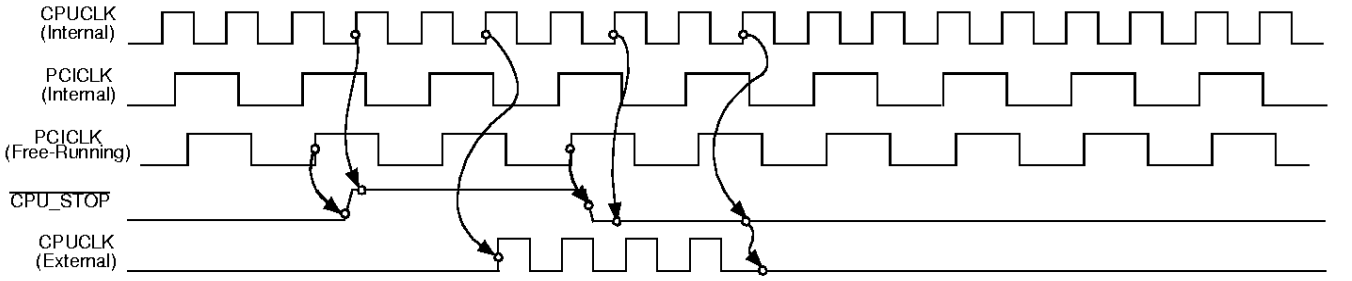
CPU-SDRAM Clock Skew



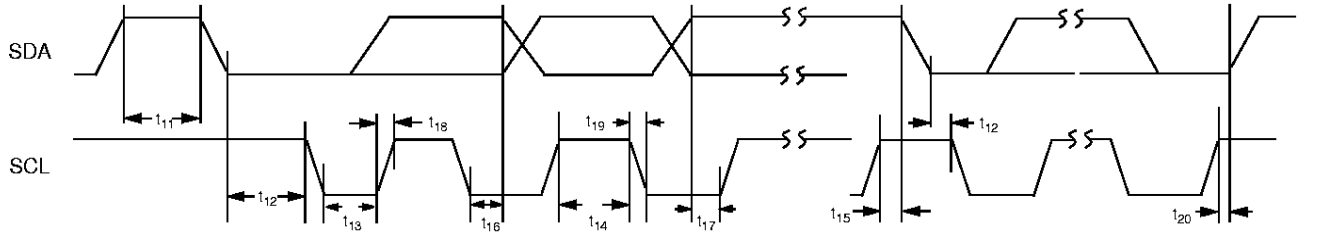
CPU-PCI Clock Skew



$\overline{\text{CPU\_STOP}}$ Timing (-3, -4 only) [7, 8]



Timing Requirements for the I^2C Bus



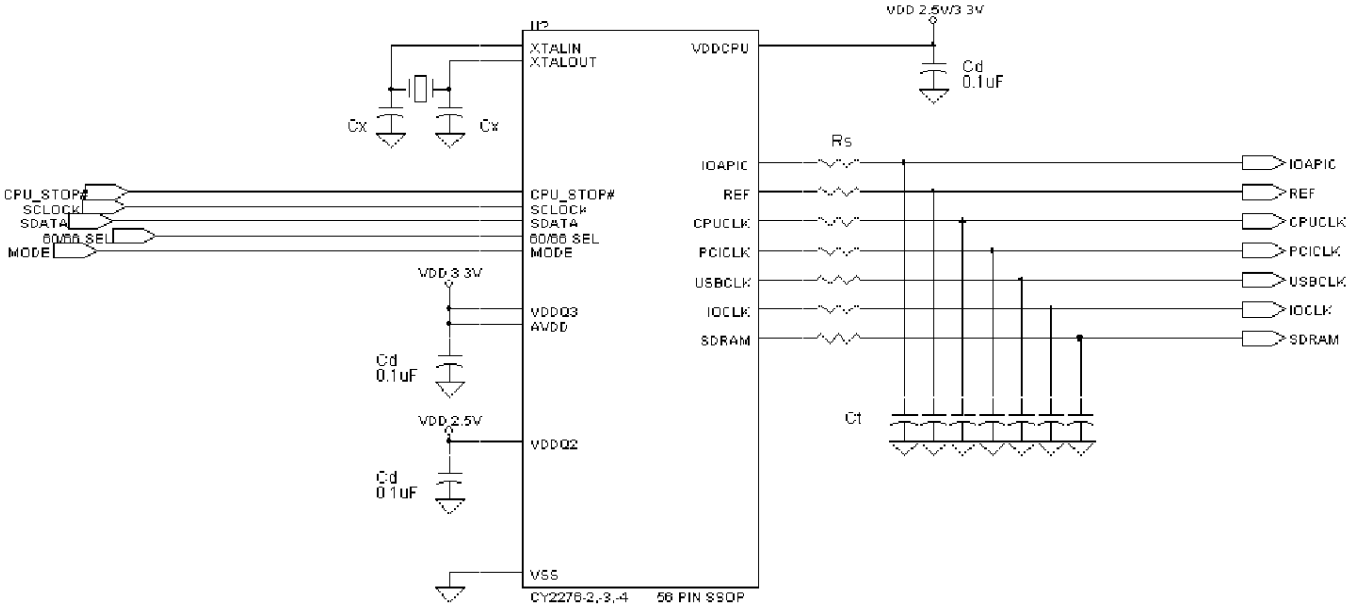
Notes:

7. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
8. $\overline{\text{CPU\_STOP}}$ may be applied asynchronously. It is synchronized internally.

Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

NOTE: 1) CPU_STOP# INPUT NOT AVAILABLE ON -2 OPTION
2) IOCLK OUTPUT NOT AVAILABLE ON -3, -4 OPTIONS

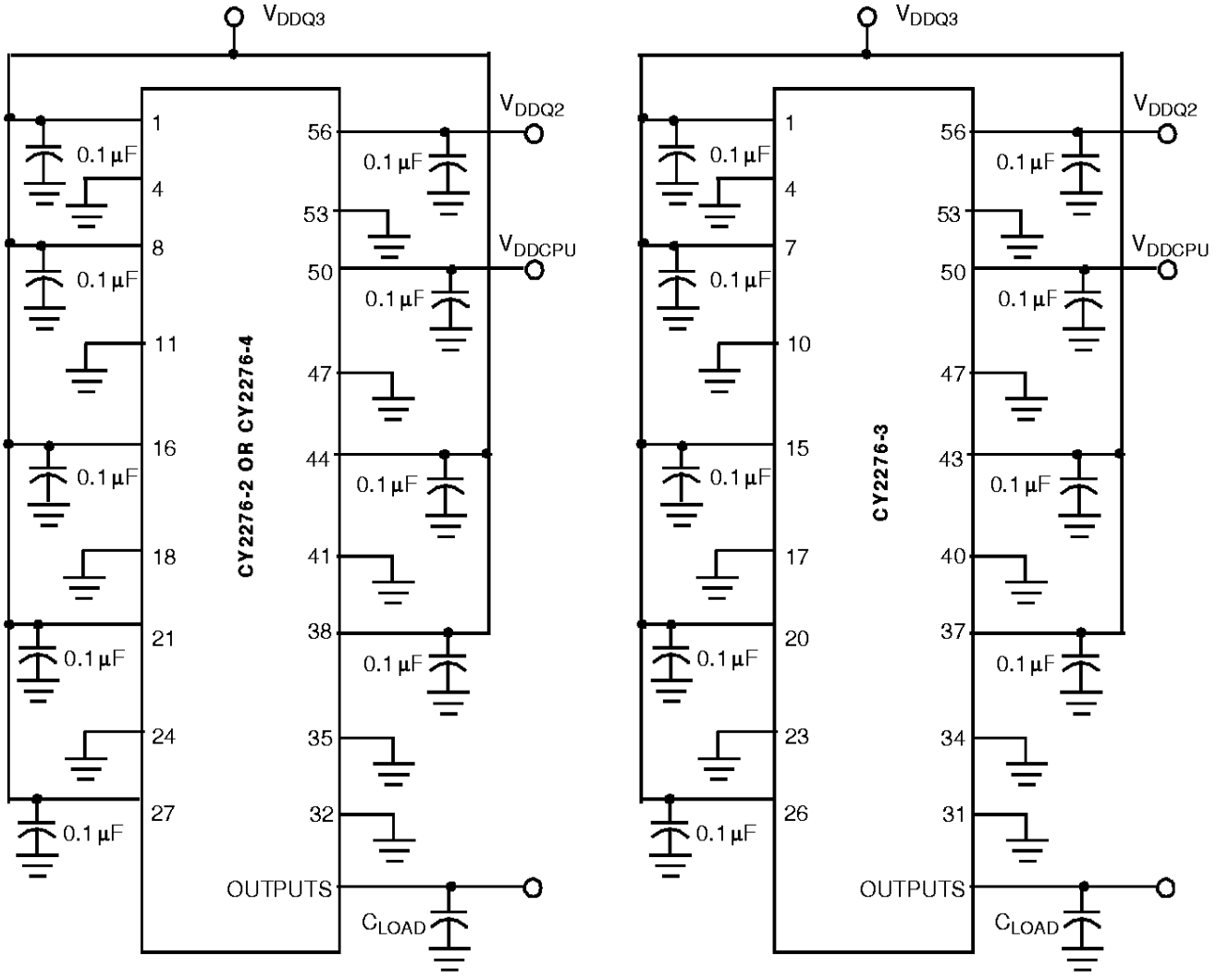
Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All Capacitors must be placed as close to the pins as is physically possible

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2276PVC–2	O56	56-Pin SSOP	Commercial
CY2276PVC–3	O56	56-Pin SSOP	Commercial
CY2276PVC–4	O56	56-Pin SSOP	Commercial

Document #: 38–00582–A

Package Diagram

56-Lead Shrunk Small Outline Package O56