

74107, LS107 Flip-Flops

Dual J-K Flip-Flop Product Specification

Logic Products

DESCRIPTION

The '107 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 74107 is a positive pulse-triggered flip-flop. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS107 is a negative edge-triggered flip-flop. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \bar{Q} output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74107	20MHz	20mA
74LS107	45MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74107N, N74LS107N
Plastic SO	N74LS107D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Manual.

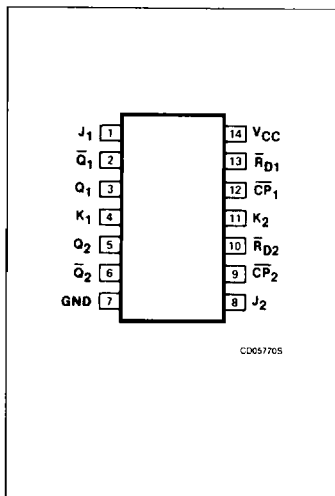
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
$\bar{C}P$	Clock input	2ul	4LSul
\bar{R}_D	Reset input	2ul	3LSul
J, K	Data inputs	1ul	1LSul
Q, \bar{Q}	Outputs	10ul	10LSul

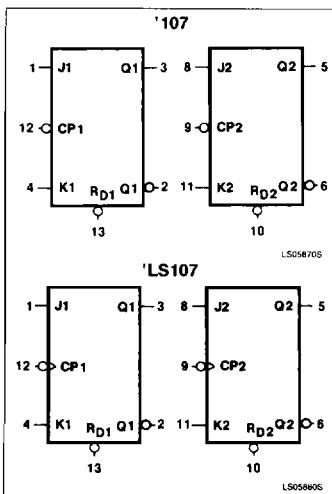
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

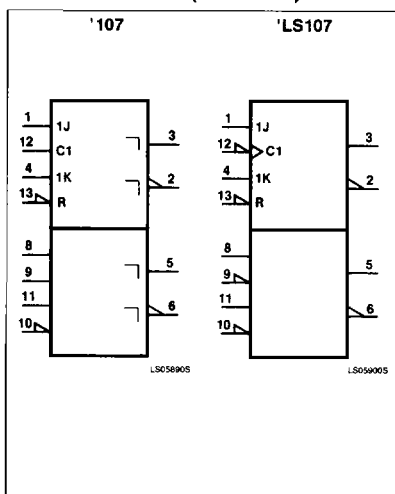
PIN CONFIGURATION



LOGIC SYMBOL



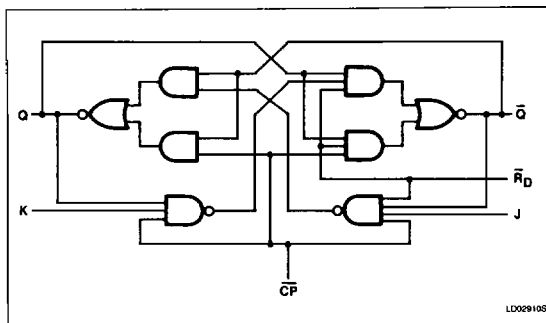
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{R}_D	$\overline{CP}^{(2)}$	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	\bar{L}	H
Toggle	H	\square	h	h	\bar{q}	q
Load "0" (Reset)	H	\square	l	h	L	H
Load "1" (Set)	H	\square	h	l	H	L
Hold "no change"	H	\square	l	l	q	\bar{q}

- H = HIGH voltage level steady state.
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.⁽²⁾
- L = LOW voltage level steady state.
- l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.⁽²⁾
- q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
- X = Don't care.
- \square = Positive Clock pulse.

NOTES:

1. The J and K inputs of the 74107 must be stable while the Clock is HIGH for conventional operation.
2. The 74LS107 is edge-triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8	V
I_{IK} Input clamp current			-12			-18	mA
I_{OH} HIGH-level output current			-400			-400	μA
I_{OL} LOW-level output current			16			8	mA
T_A Operating free-air temperature	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74107			74LS107			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4	0.35	0.5	V	
		I _{OL} = 4mA (74LS)				0.25	0.4	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	J, K Inputs				0.1	mA	
			\overline{R}_D Inputs				0.3	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, K Inputs		40			μ A	
			\overline{R}_D Inputs		80			μ A	
			\overline{CP} Inputs		80			μ A	
		V _I = 2.7V	J, K Inputs					20	μ A
			\overline{R}_D Inputs					60	μ A
			\overline{CP} Inputs					80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, K Inputs		-1.6			-0.4	mA	
		\overline{R}_D Inputs		-3.2			-0.8	mA	
		\overline{CP} Inputs		-3.2			-0.8	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			40			8	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 3	15		30		MHz
t _{PLH} Propagation delay	Waveform 1, 'LS107 Waveform 3, '107		25		20	ns
t _{PHL} Clock to output			40		30	
t _{PLH} Propagation delay	Waveform 2		25		20	ns
t _{PHL} Reset to output			40		30	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

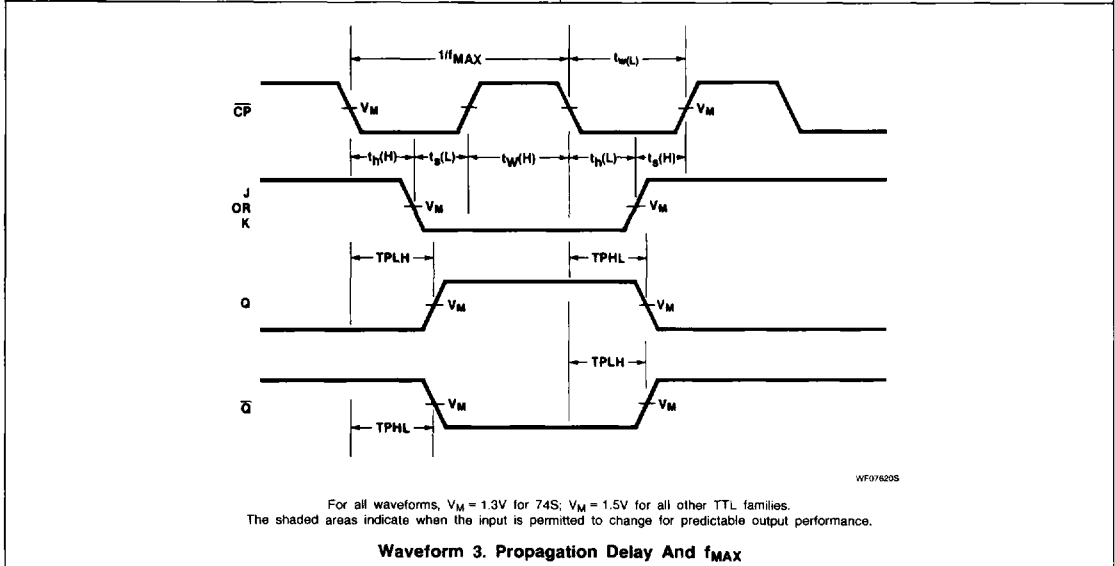
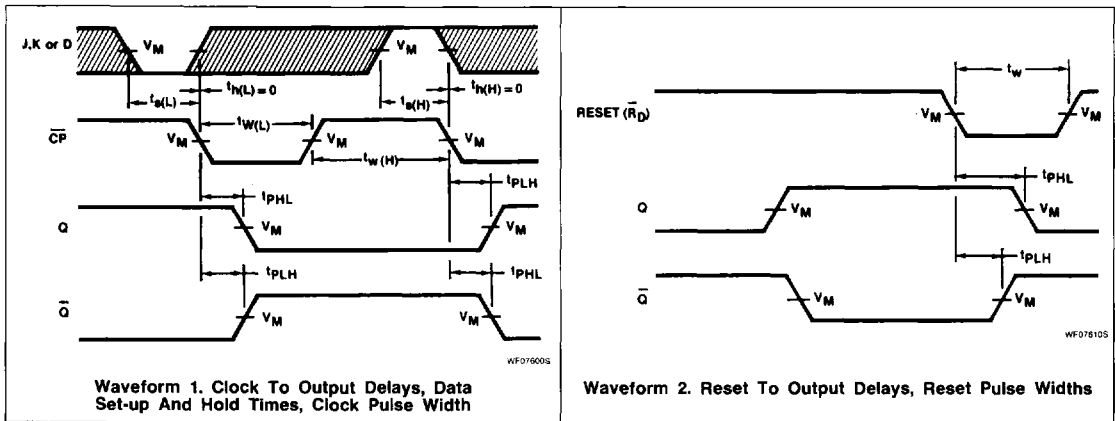
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AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	47		13		ns
$t_{w(L)}$ Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s Setup time J or K to clock ^(b)	Waveform 1	0		20		ns
t_h Hold time J or K to clock	Waveform 1	0		0		ns

AC WAVEFORMS

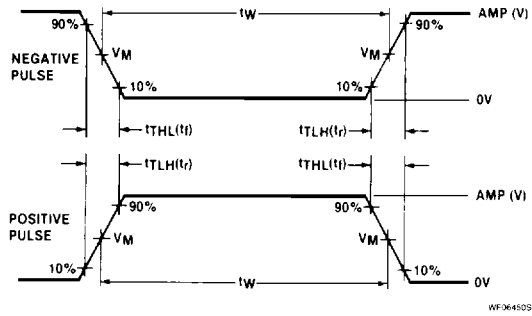
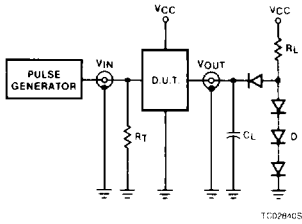


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TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns