

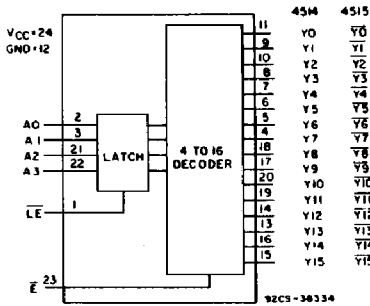
**CD54/74HC4514, CD54/74HCT4514
CD54/74HC4515, CD54/74HCT4515**



Data sheet acquired from Harris Semiconductor
SCHS280

High-Speed CMOS Logic

**4-to-16 Line Decoder/Demultiplexer
with Input Latches**



FUNCTIONAL DIAGRAM

- Type Features:**
- Multifunction capability:
Binary to 1-of-16 decoder
1-to-16 line demultiplexer

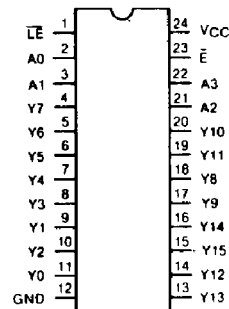
The RCA CD54/74HC4514, 4515 and CD54/74HCT4514, 4515 are high-speed silicon gate devices consisting of a 4-bit strobed latch and a 4-to-16 line decoder. The selected output is enabled by a low on the enable input (\overline{E}). A high on \overline{E} inhibits selection of any output. Demultiplexing is accomplished by using the \overline{E} input as the data input and the select inputs (A0-A3) as addresses. This \overline{E} input also serves as a chip select when these devices are cascaded.

When Latch Enable (\overline{LE}) is high the output follows changes in the inputs (see truth table). When \overline{LE} is low the output is isolated from changes in the input and remains at the level (high for the 4514, low for the 4515) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.

The CD54HC4514, 4515 and CD54HCT4514, 4515 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4514, 4515 and CD74HCT4514, are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features

- Fanout (over temperature range):
Standard outputs — 10 LSTTL loads
Bus driver outputs — 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to +85°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
2 to 6 V operation
High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$;
@ $V_{CC} = 5V$
- CD54HCT/CD74HCT types:
4.5 to 5.5 V operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8 V \text{ max.}$, $V_{IH} = 2 V \text{ min.}$
CMOS input compatibility
 $I_i \leq 1 \mu A @ V_{OL}, V_{OH}$



92CS 36877

TERMINAL ASSIGNMENT

This data sheet is applicable to the CD54HC4514, CD54HCT4514, and CD74HCT4514. The CD54HC4515, CD54HCT4515, and CD74HCT4515 were not acquired from Harris Semiconductor. See SCHS215 for information on the CD74HC4514 and CD74HC4515.

CD54/74HC4514, CD54/74HCT4514 CD54/74HC4515, CD54/74HCT4515

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC}):		
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):		
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg}):		-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

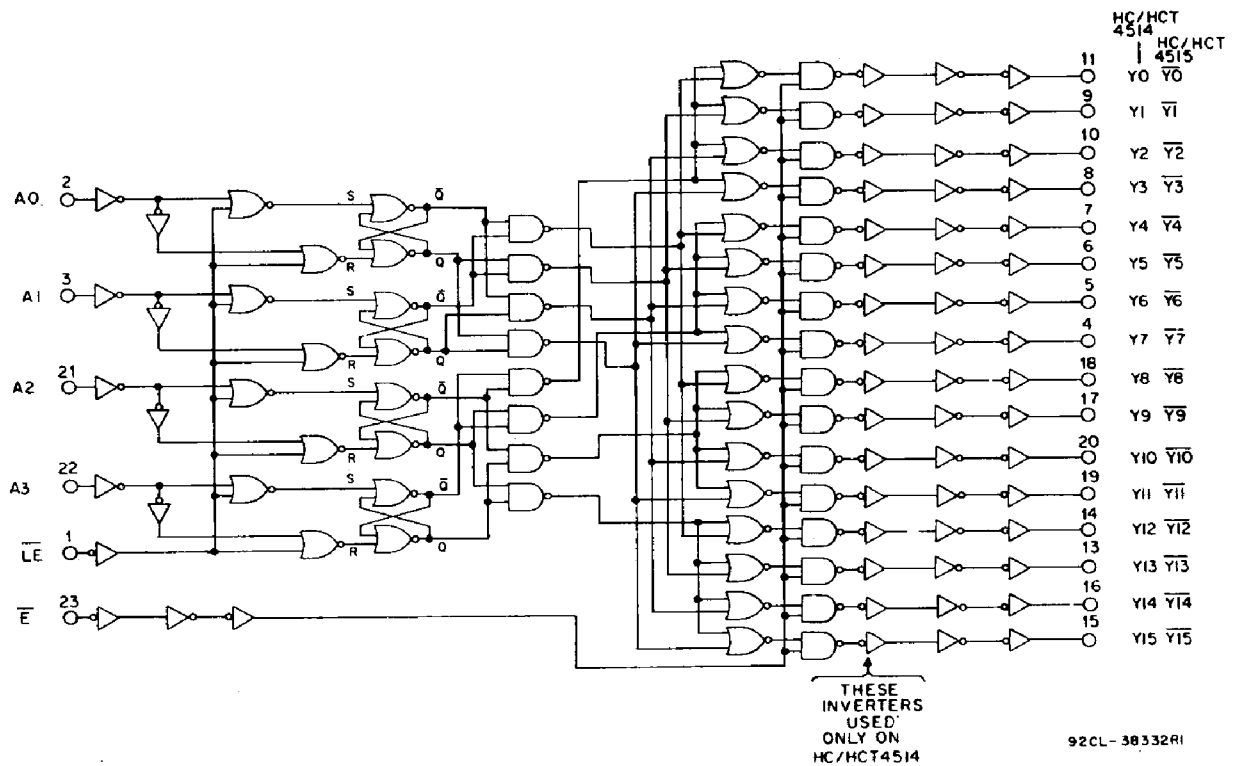


Fig. -- Logic diagram for CD54/74HC4514, 4515 and CD54/74HCT4514, 4515.

CD54/74HC4514, CD54/74HCT4514 CD54/74HC4515, CD54/74HCT4515

DECODE TRUTH TABLE ($\overline{LE} = 1$)

ENABLE	DECODER INPUTS				ADDRESSED OUTPUT 4514 = Logic 1 (High) 4515 = Logic 0 (Low)
	A3	A2	A1	A0	
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All Outputs = 0, 4514 All Outputs = 1, 4515

X = Don't Care Logic 1 = High Logic 0 = Low

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC} :* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A : CD74 Types CD54 Types	-40 -55	+85 +125	°C °C
Input Rise and Fall Times, t_r, t_f at 2V at 4.5 V at 6V	0 0 0	1000 500 400	ns ns ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4514, CD54/74HCT4514 CD54/74HC4515, CD54/74HCT4515

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay Select to Output	t_{PHL}	15	23	25	ns
	t_{PLH}				
\overline{LE} to Output	t_{PHL}	15	19	21	ns
	t_{PLH}				
\overline{E} to Output	t_{PHL}	15	14	17	ns
	t_{PLH}				
Power Dissipation Capacitance*	C_{PD}	—	70	75	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$PD = V_{CC}^2 f_i (C_{PD} + C_L)$ where:

f_i = input frequency,

C_L = output load capacitance

V_{CC} = supply voltage

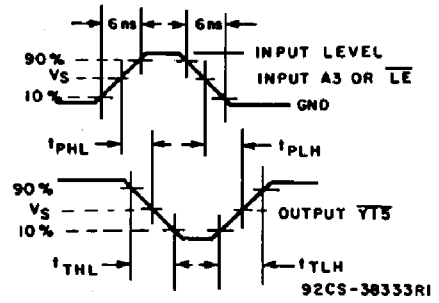
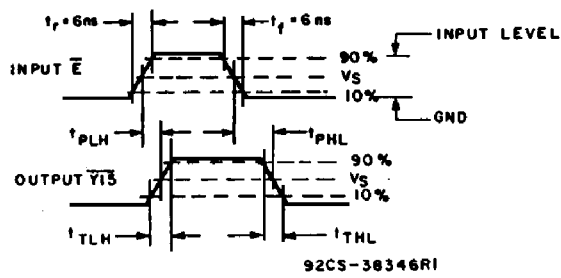
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS	
			HC		HCT		74HC		74HCT		54HC		54HCT			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
\overline{LE} Pulse Width	t_w	2	75	—	—	—	—	95	—	—	—	—	110	—	—	ns
		4.5	15	—	30	—	—	19	—	38	—	—	22	—	45	
		6	13	—	—	—	—	16	—	—	—	—	19	—	—	
Select to \overline{LE} Set-up time	t_{su}	2	100	—	—	—	—	125	—	—	—	—	150	—	—	ns
		4.5	20	—	20	—	—	25	—	25	—	—	30	—	30	
		6	17	—	—	—	—	21	—	—	—	—	26	—	—	
Select to \overline{LE} Hold Time	t_H	2	0	—	—	—	—	0	—	—	—	—	0	—	—	ns
		4.5	0	—	5	—	—	0	—	5	—	—	0	—	5	
		6	0	—	—	—	—	0	—	—	—	—	0	—	—	

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS	
			HC		HCT		74HC		74HCT		54HC		54HCT			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay Select to Outputs	t_{PLH} t_{PHL}	2	—	275	—	—	—	345	—	—	—	—	115	—	—	ns
		4.5	—	55	—	55	—	69	—	69	—	—	83	—	83	
		6	—	47	—	—	—	59	—	—	—	—	71	—	—	
\overline{LE} to Outputs	t_{PLH} t_{PHL}	2	—	225	—	—	—	280	—	—	—	—	340	—	—	ns
		4.5	—	45	—	50	—	56	—	63	—	—	68	—	75	
		6	—	38	—	—	—	48	—	—	—	—	58	—	—	
\overline{E} to Outputs	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	—	265	—	—	ns
		4.5	—	35	—	40	—	44	—	50	—	—	53	—	60	
		6	—	30	—	—	—	37	—	—	—	—	45	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	—	19	—	—	
Input Capacitance	C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF	

CD54/74HC4514, CD54/74HCT4514 CD54/74HC4515, CD54/74HCT4515



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Propagation delay times and transition times for HC/HCT4515.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.