DRAM

1 MEG x 16 DRAM

3.3V, FAST PAGE MODE, OPTIONAL EXTENDED REFRESH

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN; optional Extended
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 0.3mW standby; 250mW active, typical
- 5V-tolerant inputs and I/Os

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Refresh Rate
  - Standard 16ms period — None
  - Extended 128ms period — L
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Part Number Example: MT4LC1M16C3DJ-6 L

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

42-Pin SOJ (DA-7)

Vcc	1	42	Vss
DQ1	2	41	DQ16
DQ2	3	40	DQ15
DQ3	4	39	DQ14
DQ4	5	38	DQ13
Vcc	6	37	Vss
DQ5	7	36	DQ12
DQ6	8	35	DQ11
DQ7	9	34	DQ10
DQ8	10	33	DQ9
NC	11	32	NC
NC	12	31	$\overline{CASL}$
$\overline{WE}$	13	30	$\overline{CASH}$
$\overline{RAS}$	14	29	$\overline{OE}$
NC	15	28	A9
NC	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
Vcc	21	22	Vss

44/50-Pin TSOP (DB-5)

Vcc	1	50	Vss
DQ1	2	49	DQ16
DQ2	3	48	DQ15
DQ3	4	47	DQ14
DQ4	5	46	DQ13
Vcc	6	45	Vss
DQ5	7	44	DQ12
DQ6	8	43	DQ11
DQ7	9	42	DQ10
DQ8	10	41	DQ9
NC	11	40	NC
NC	15	36	NC
NC	16	35	$\overline{CASL}$
$\overline{WE}$	17	34	$\overline{CASH}$
$\overline{RAS}$	18	33	$\overline{OE}$
NC	19	32	A9
NC	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
Vcc	25	26	Vss

GENERAL DESCRIPTION

The MT4LC1M16C3(L) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4LC1M16C3(L) has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins ($\overline{CASL}$ and $\overline{CASH}$). These function in an identical manner to a single $\overline{CAS}$ of other DRAMs in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4LC1M16C3(L) $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last $\overline{CAS}$ to transition back HIGH. Use of only one of the two results in a BYTE access cycle. $\overline{CASL}$ transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. The $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The $\overline{CAS}$ function also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{RAS}$ goes LOW.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input of other DRAMs. The key difference is each $\overline{CAS}$ input ($\overline{CASL}$ and $\overline{CASH}$) controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16. The two $\overline{CAS}$ controls give the MT4LC1M16C3(L) BYTE WRITE cycle capabilities.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$,

GENERAL DESCRIPTION (continued)

whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on the "L" version), regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

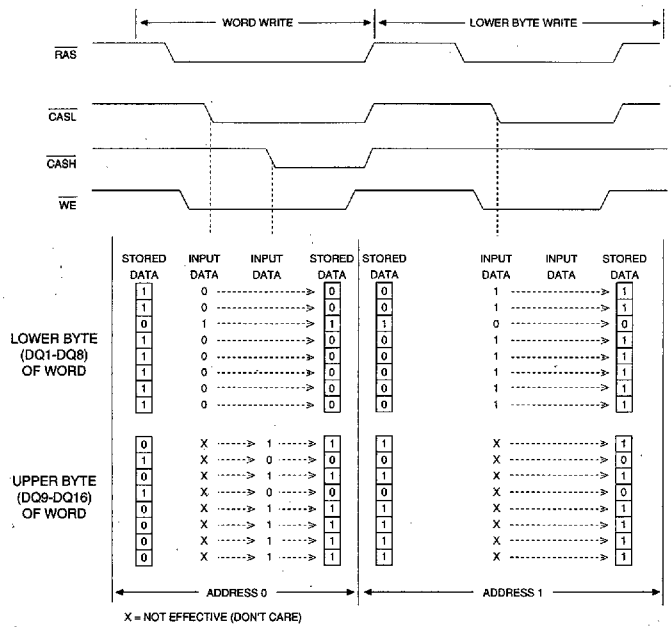


Figure 1
WORD AND BYTE WRITE EXAMPLE

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE access (DQ1-DQ8). Enabling $\overline{CASH}$ will select an upper BYTE access (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4LC1M16C3 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{CAS}$ inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A $\overline{CAS}$ precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte is not allowed during the same cycle. However, an EARLY WRITE on one byte and, after a $\overline{CAS}$ precharge has been satisfied, a LATE WRITE on the other byte is permissable.

REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing. An optional "L" version allows the user to refresh all 1,024 rows every 128ms.

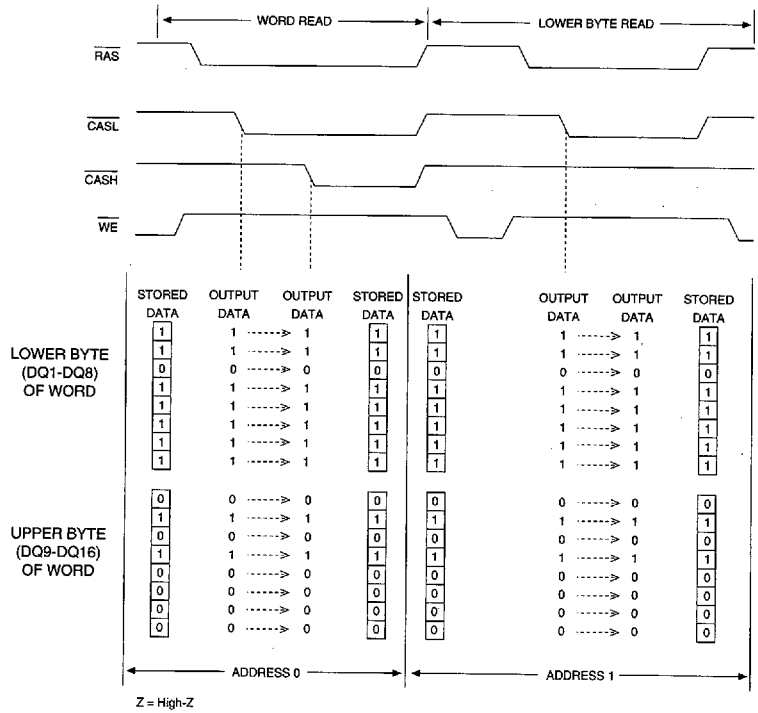
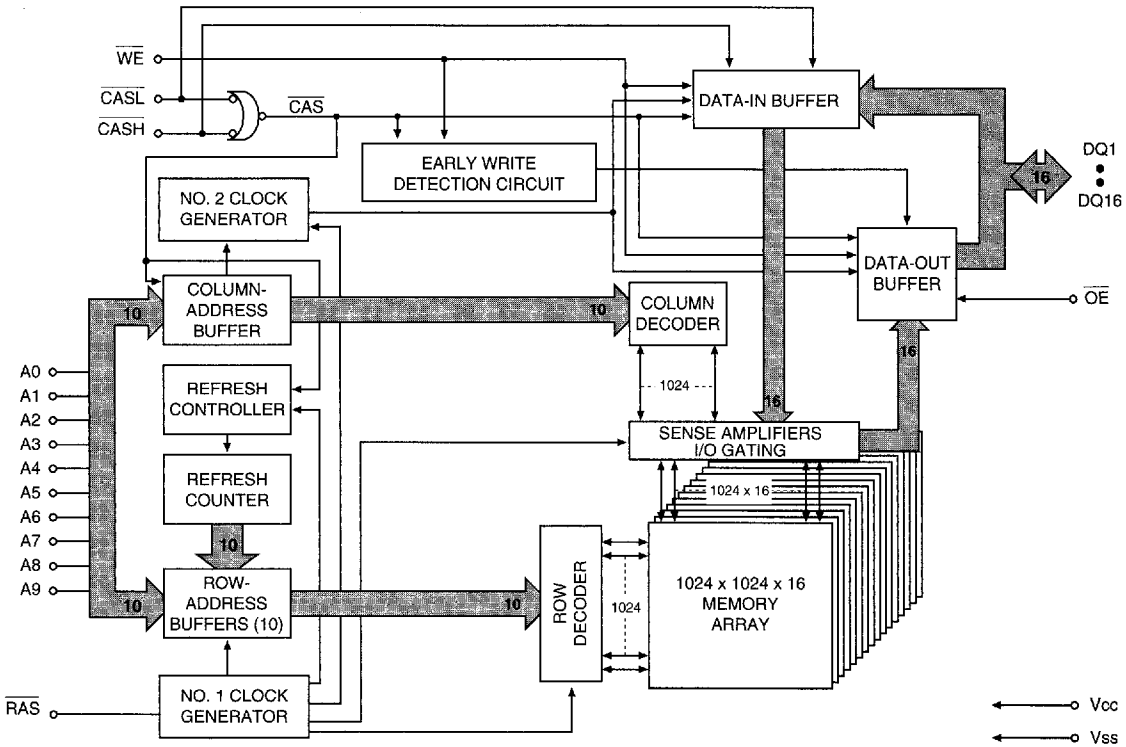


Figure 2
WORD READ EXAMPLE

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, Data-Out	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	3

NOTE: 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. EARLY WRITE only.
3. Only one CAS must be active (CASL or CASH).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} pin Relative to V_{SS} ..... -1V to 4.6V
Voltage on NC, Inputs or I/O pins
Relative to V_{SS} ..... -1V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	5.5V	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.0mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION		SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS)		I_{CC2}	500	500	µA	24
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	L only	I_{CC2}	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ address cycling: ^tRC = ^tRC [MIN])		I_{CC3}	170	155	mA	3, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)		I_{CC4}	100	90	mA	3, 25
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	160	145	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ address cycling: ^tRC = ^tRC [MIN])		I_{CC6}	150	140	mA	3, 4
REFRESH CURRENT: Extended (L version only) Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A9, $\overline{OE}$ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)		I_{CC7} (L only)	300	300	µA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	29
Row-address setup time	^tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	20
Access time from $\overline{CAS}$	^tCAC		15		20	ns	14, 31
Column-address hold time	^tCAH	10		15		ns	29
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	37
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	4, 30
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		ns	33
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	28, 31
$\overline{CAS}$ precharge time	^tCP	10		10		ns	15, 34
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	32
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	31
$\overline{CAS}$ hold time	^tCSH	60		70		ns	31
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	4, 29
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	20, 29
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	25, 32
Data-in hold time	^tDH	10		15		ns	21, 31
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	21, 31
Output disable	^tOD	3	15	3	20	ns	27, 28, 39
Output enable	^tOE		15		20	ns	32
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		ns	27
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	19, 28, 31
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

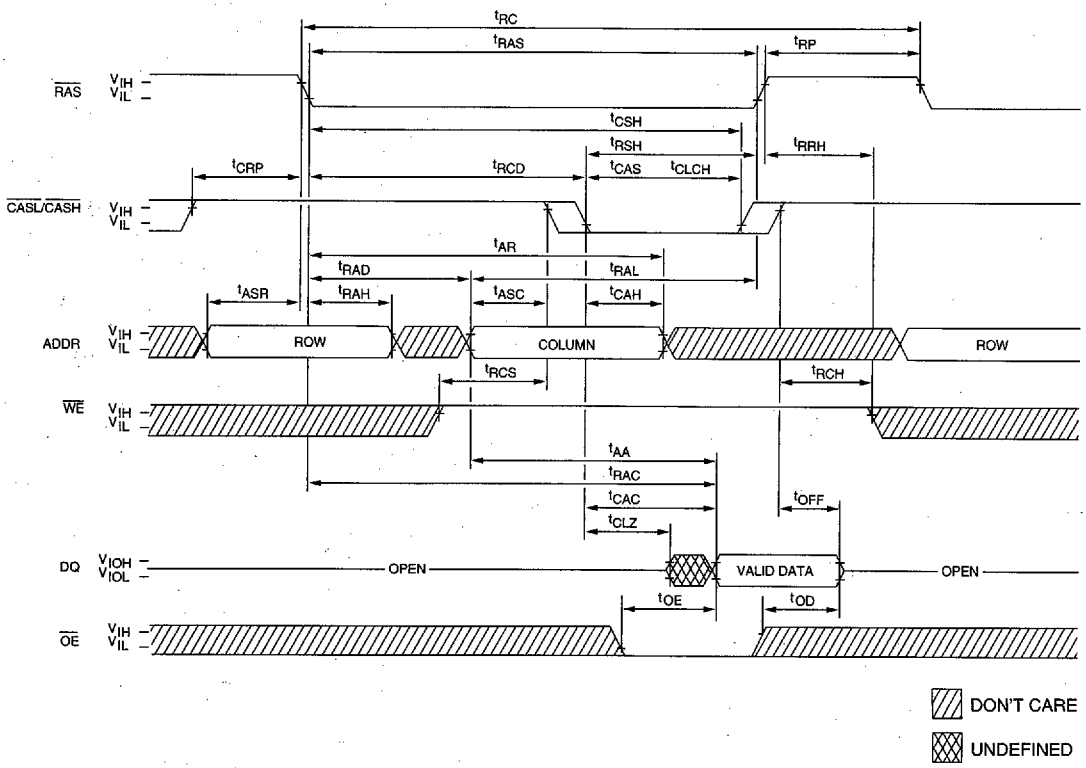
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		ns	33
Access time from $\overline{RAS}$	tRAC		60		70	ns	13
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	ns	17
Row-address hold time	tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	ns	16, 29
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	18, 30
Read command setup time	tRCS	0		0		ns	29
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (1,024 cycles) L version	tREF		128		128	ms	
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	18
$\overline{RAS}$ hold time	tRSH	15		20		ns	38
READ WRITE cycle time	tRWC	150		180		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		95		ns	20
Write command to $\overline{RAS}$ lead time	tRWL	15		20		ns	
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	38
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		ns	
$\overline{WE}$ command setup time	tWCS	0		0		ns	20, 29
Write command pulse width	tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		ns	

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.0V; f = 1 MHz.
3. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
6. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
9. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. If $\overline{CAS}$ = VIH, data output is High-Z.
11. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to one TTL gate, 50pF and VOL = 0.8V and VOH = 2.0V.
13. Assumes that $^{t}RCD < ^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
14. Assumes that $^{t}RCD \ge ^{t}RCD$ (MAX).
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
16. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
17. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
18. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.
20. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $^{t}WCS \ge ^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \ge ^{t}RWD$ (MIN), $^{t}AWD \ge ^{t}AWD$ (MIN) and $^{t}CWD \ge ^{t}CWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
22. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. All other inputs at 0.2V or Vcc -0.2V.
25. Column-address changed once each cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
28. The 3ns minimum is a parameter guaranteed by design.
29. The first $\overline{CAS}$x edge to transition LOW.
30. The last $\overline{CAS}$x edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
32. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
33. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
35. First DQs controlled by the first $\overline{CAS}$x to go LOW.
36. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
37. Each $\overline{CAS}$x must meet minimum pulse width.
38. Last $\overline{CAS}$x to go LOW.
39. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.

READ CYCLE

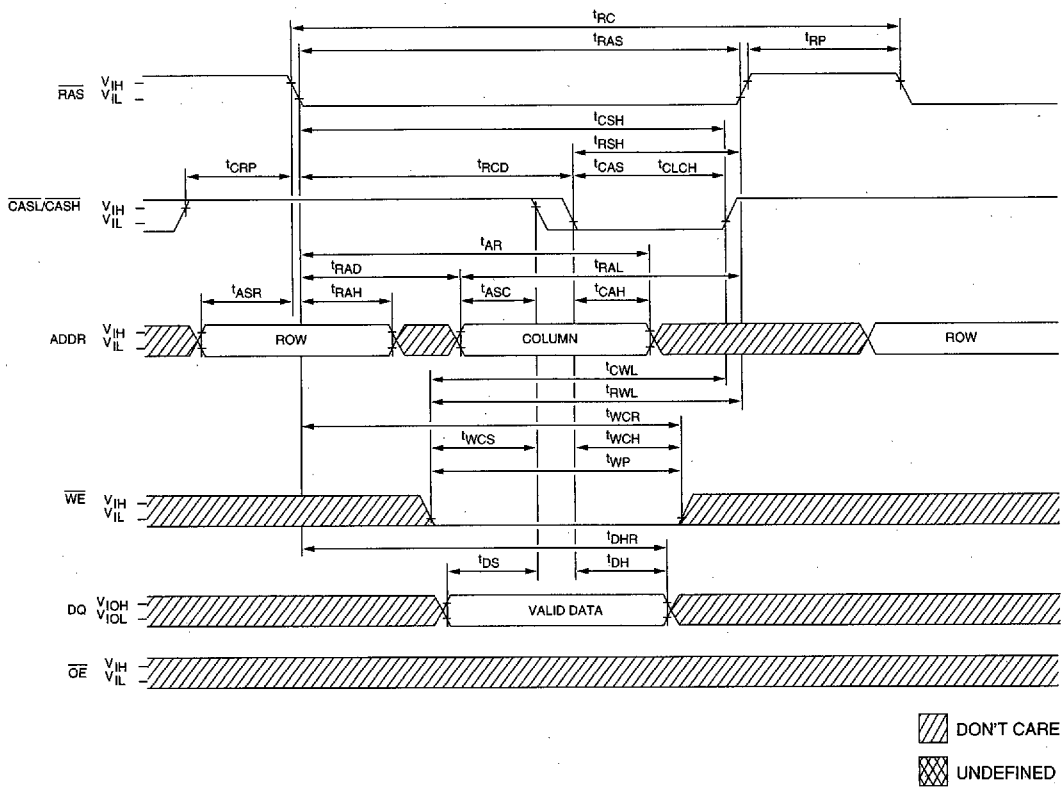


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLCH	10		10		ns
tCLZ	3		3		ns
tCRP	5		5		ns
tCSH	60		70		ns
tOD	3	15	3	20	ns
tOE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOFF	3	15	3	20	ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

EARLY WRITE CYCLE

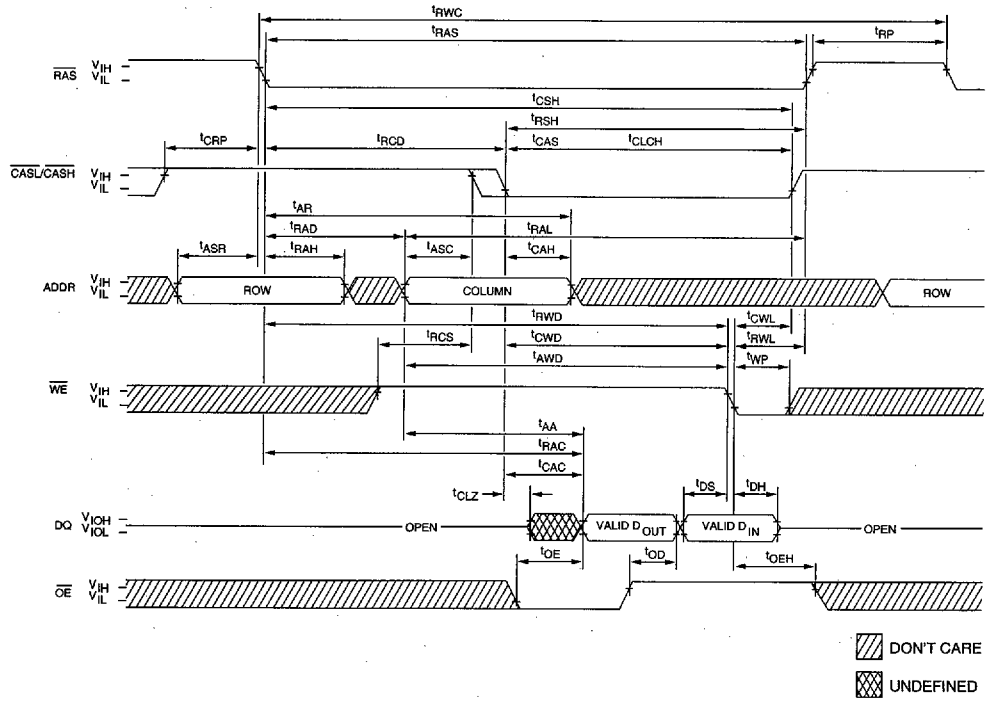


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLCH	10		10		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDHR	45		55		ns
tDS	0		0		ns
tRAD	15	30	15	35	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		15		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

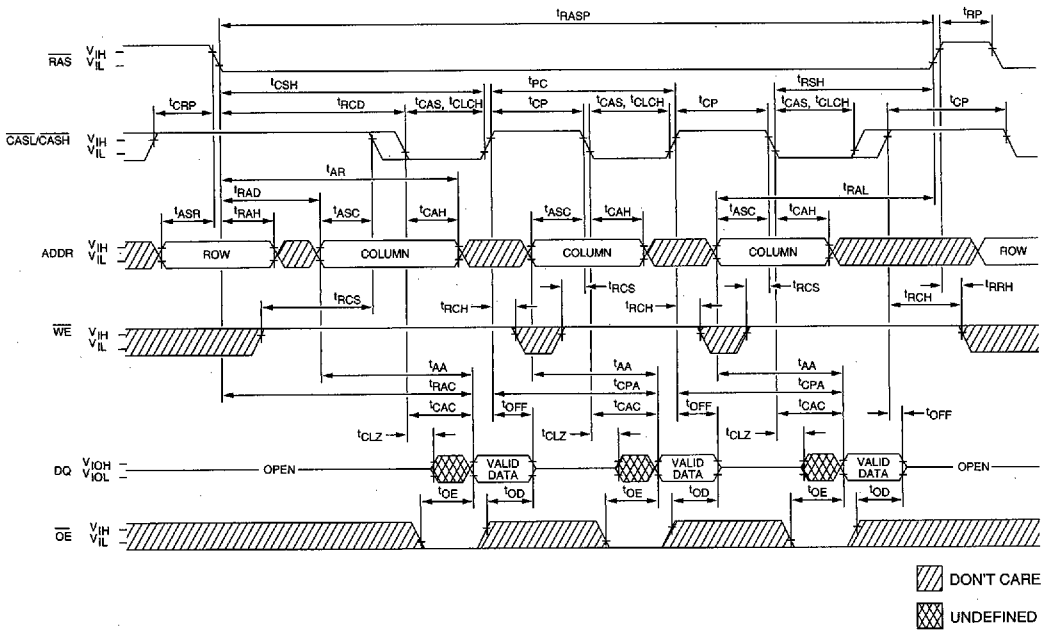


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLCH	10		10		ns
tCLZ	3		3		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWD	40		45		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOD	3	15	3	20	ns
tOE		15		20	ns
tOEH	15		20		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWC	150		180		ns
tRWD	85		95		ns
tRWL	15		20		ns
tWP	10		15		ns

FAST-PAGE-MODE READ CYCLE

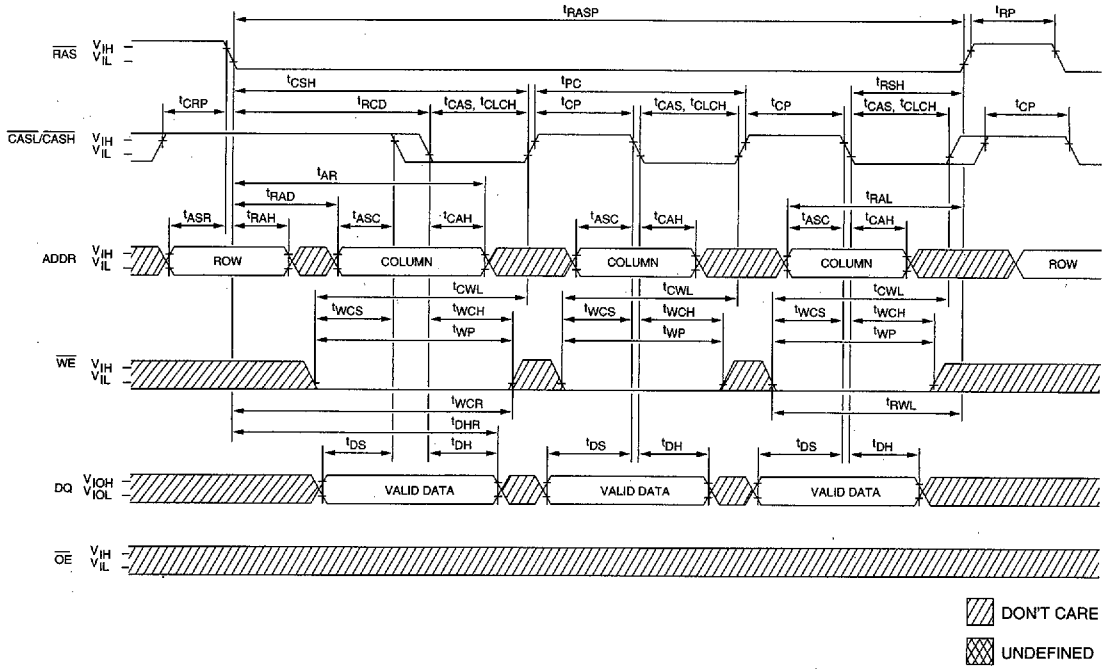


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLCH	10		10		ns
tCLZ	3		3		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	5		5		ns
tCSH	60		70		ns
tOD	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOE		15		20	ns
tOFF	3	15	3	20	ns
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

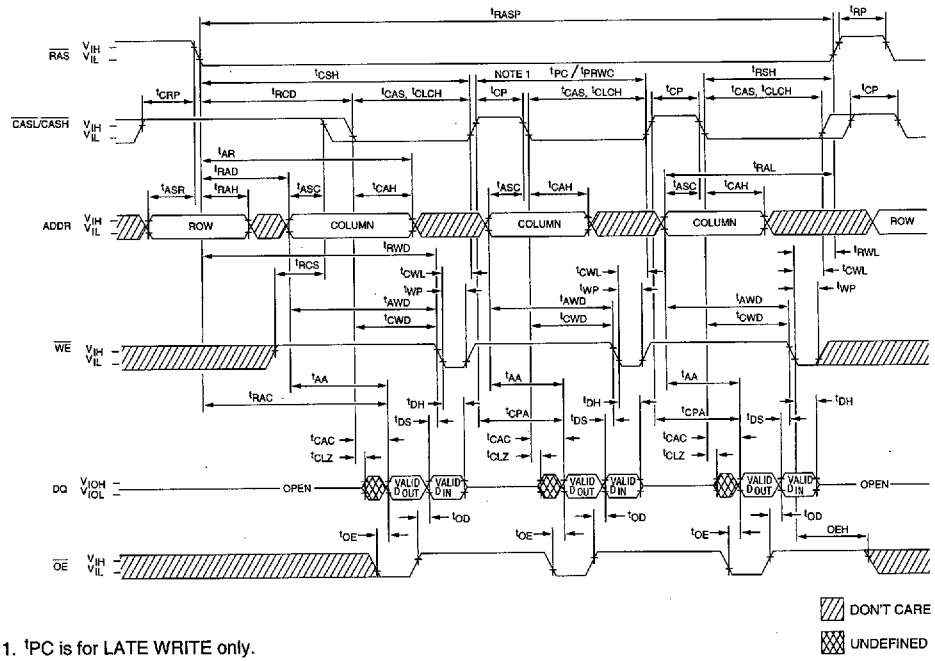


TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLCH	10		10		ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDHR	45		55		ns
tDS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tPC	35		40		ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		15		ns

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



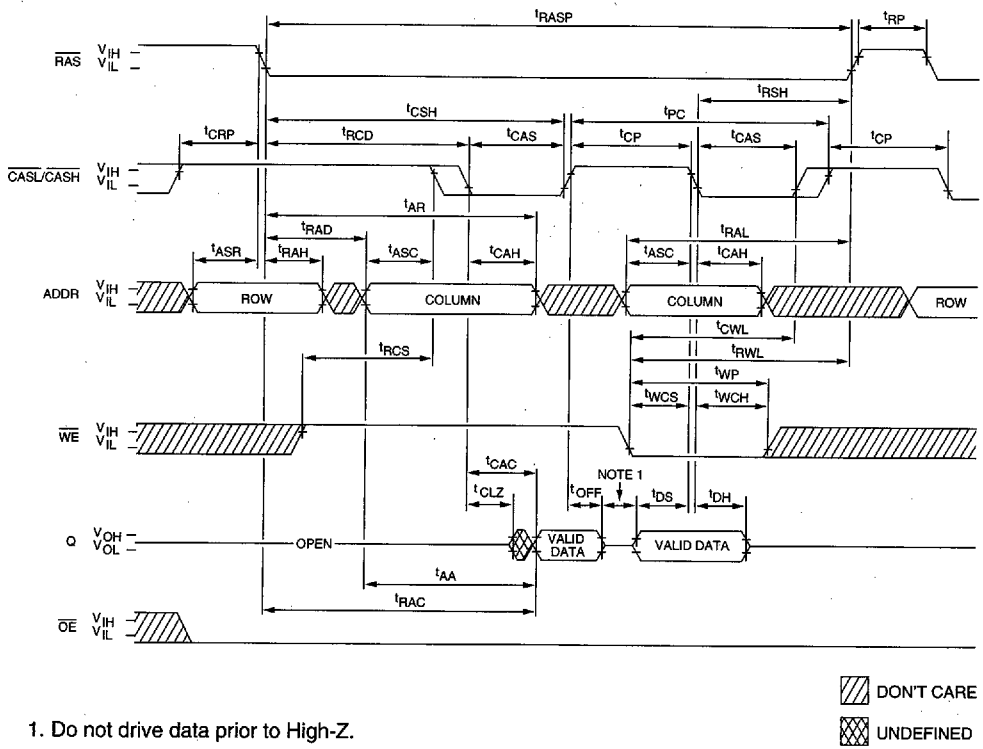
NOTE: 1. tPC is for LATE WRITE only.

TIMING PARAMETERS

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLCH	10		10		ns
tCLZ	3		3		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWD	40		45		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tOD	3	15	3	20	ns
tOE		15		20	ns
tOEH	15		20		ns
tPC	35		40		ns
tPRWC	85		95		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWD	85		95		ns
tRWL	15		20		ns
tWP	10		15		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



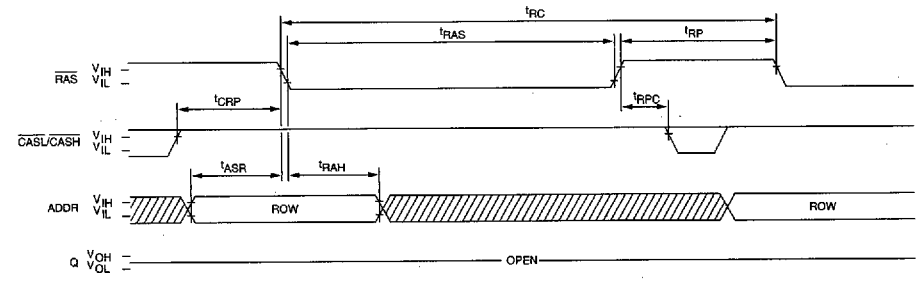
NOTE: 1. Do not drive data prior to High-Z.

TIMING PARAMETERS

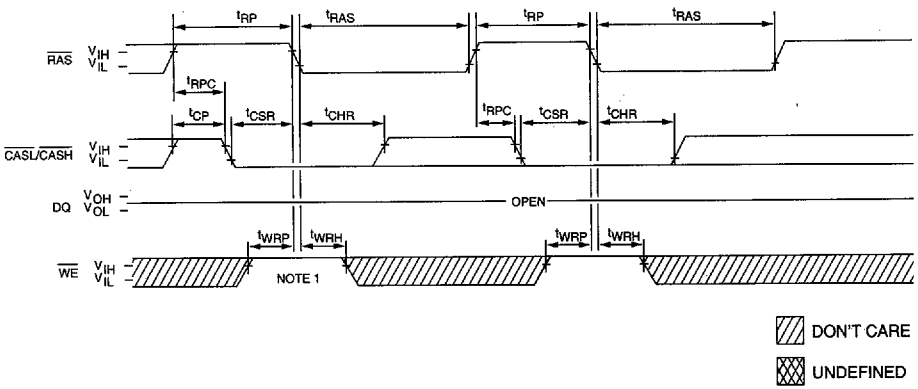
	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	3		3		ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCS	0		0		ns
tWP	10		15		ns

RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)



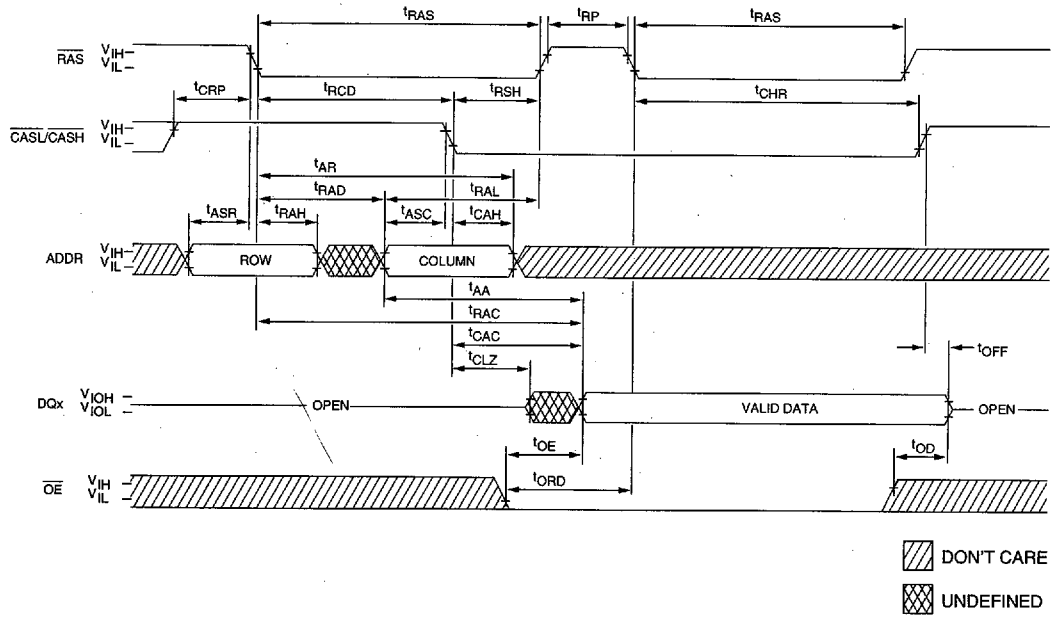
NOTE: 1. tWRP and tWRH are for system design reference only. The WE signal is actually a "don't care" at RAS time during a CBR REFRESH. However, WE should be held HIGH at RAS time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE HIGH at RAS time during a CBR REFRESH.

TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tASR	0		0		ns
tCHR	15		15		ns
tCP	10		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	10		10		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRP	40		50		ns
tRPC	0		0		ns
tWRH	10		10		ns
tWRP	10		10		ns

HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCHR	15		15		ns
tCLZ	3		3		ns
tCRP	5		5		ns
tOD	3	15	3	20	ns
tOE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOFF	3	15	3	20	ns
tORD	0		0		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns