

## 29F52•29F53 8-Bit Registered Transceiver

### General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The  $A_0$ - $A_7$  output pins are guaranteed to sink 24 mA while the  $B_0$ - $B_7$  output pins are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

### Features

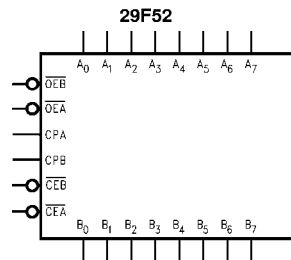
- 8-bit registered transceivers
- Separate clock, clock enable and 3-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

### Ordering Code:

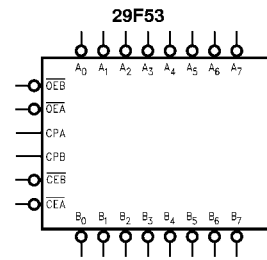
Order Number	Package Number	Package Description
29F52SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
29F52SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
29F53SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

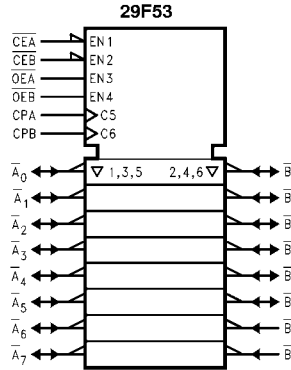
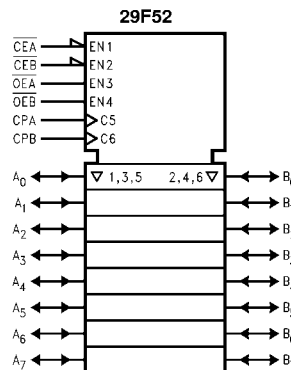
### Logic Symbols



IEEE/IEC

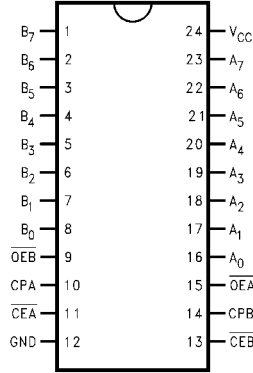


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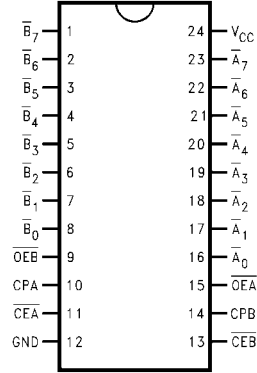


### Connection Diagrams

Pin Assignment for DIP and SOIC  
29F52



Pin Assignment for DIP  
29F53



### Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> -A <sub>7</sub>	A-Register Inputs/ B-Register 3-STATE Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A/0.65 mA -3 mA/24 mA (20 mA)
B <sub>0</sub> -B <sub>7</sub>	B Register Inputs/ A-Register 3-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A/0.65 mA -12 mA/64 mA (48 mA)
$\overline{OE}$ A	Output Enable A-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CPA	A-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CE}$ A	A-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{OE}$ B	Output Enable B-Register	1.0/1.0	20 $\mu$ A/-0.6 mA
CPB	B-Register Clock	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CE}$ B	B-Register Clock Enable	1.0/1.0	20 $\mu$ A/-0.6 mA

### Output Control

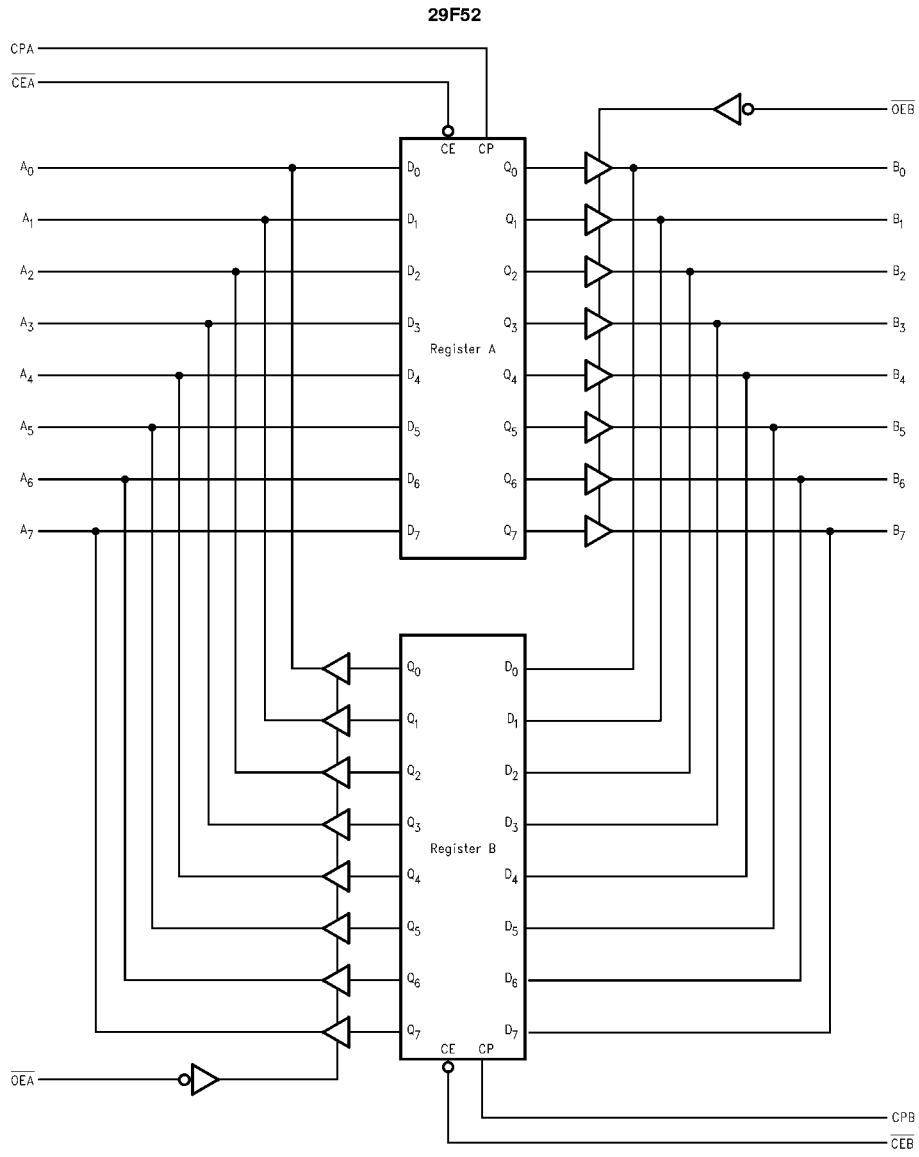
OE	Internal Q	Y-Output		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = HIGH Impedance  
 N = LOW-to-HIGH Transition  
 NC = No Change

### Register Function Table (Applies to A or B Register)

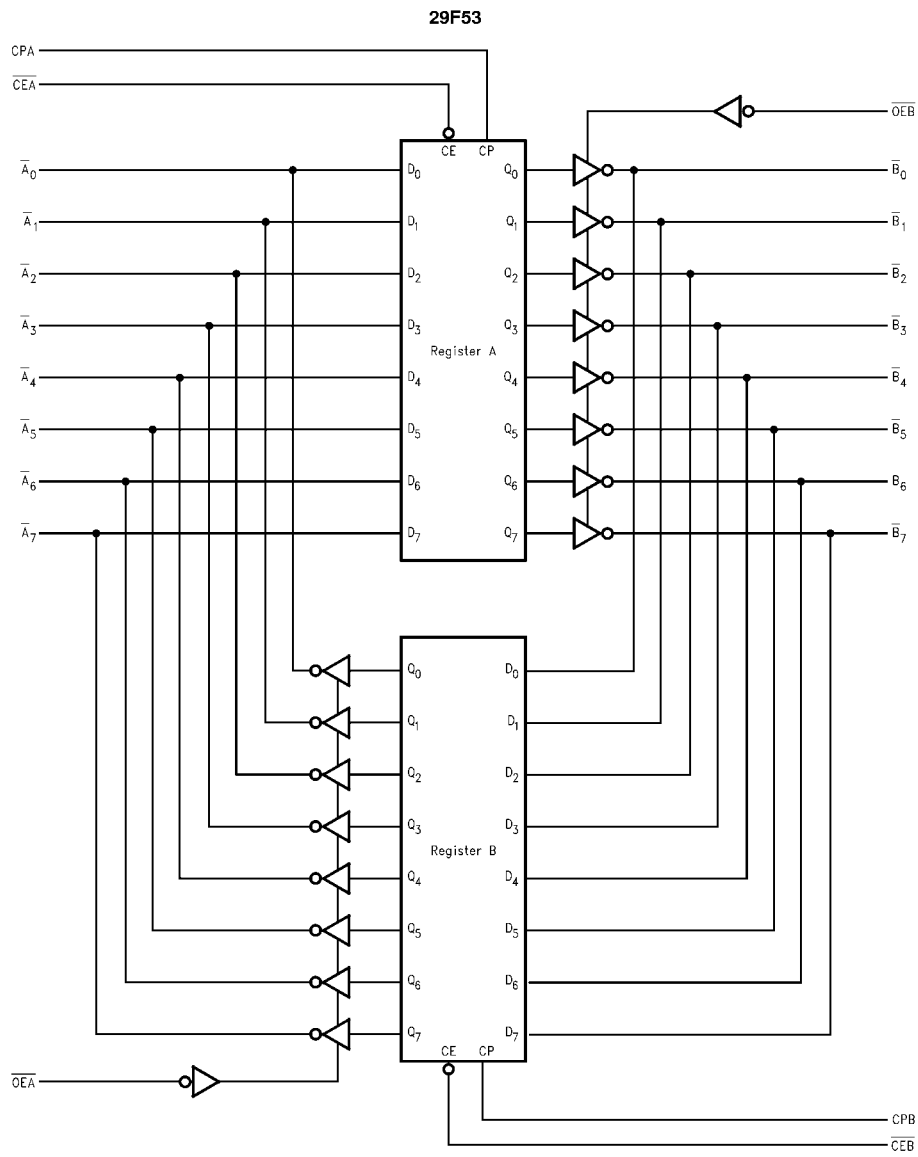
Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	N	L	L	Load Data
H	N	L	H	

# Block Diagrams



29F52, 29F53

Block Diagrams (continued)



**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
		10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -15 mA (B <sub>n</sub> )
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA (A <sub>n</sub> )
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 24 mA (A <sub>n</sub> )
		10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> )
				-100			-225
I <sub>CEx</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		130	190	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			190	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			190	mA	Max	V <sub>O</sub> = HIGH Z

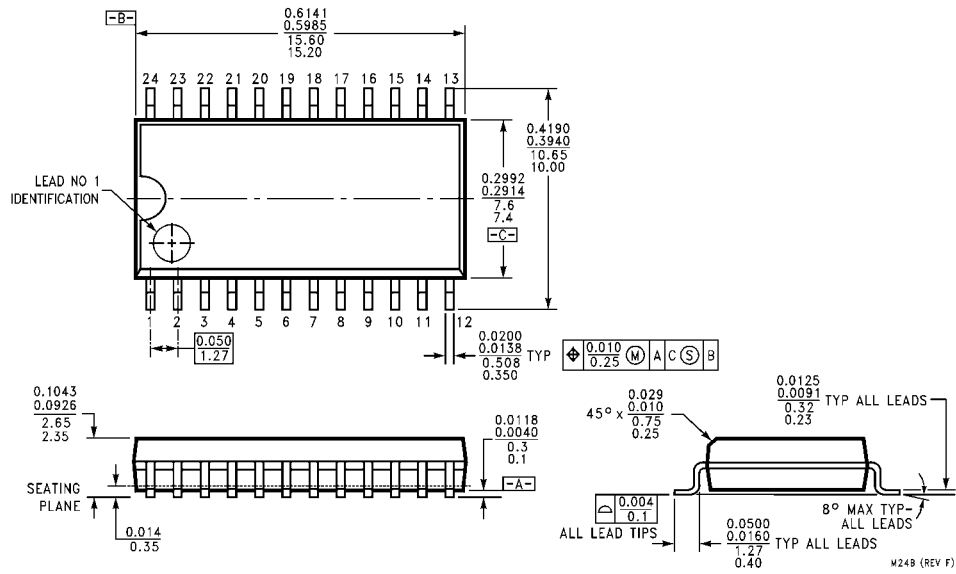
### AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay	3.0	5.5	7.5			2.5	8.5	ns
$t_{PHL}$	CPA or CPB to $A_n$ or $B_n$	4.0	7.0	9.0			3.5	10.0	
$t_{PZH}$	Output Enable Time	2.5	5.5	7.5			2.0	8.5	ns
$t_{PZL}$	$\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ to $A_n$ or $B_n$	3.5	7.0	9.5			3.0	10.5	
$t_{PHZ}$	Output Disable Time	2.5	6.5	9.0			2.0	10.0	ns
$t_{PLZ}$	$\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ to $A_n$ or $B_n$	2.5	5.5	7.5			2.0	8.5	

### AC Operating Requirements

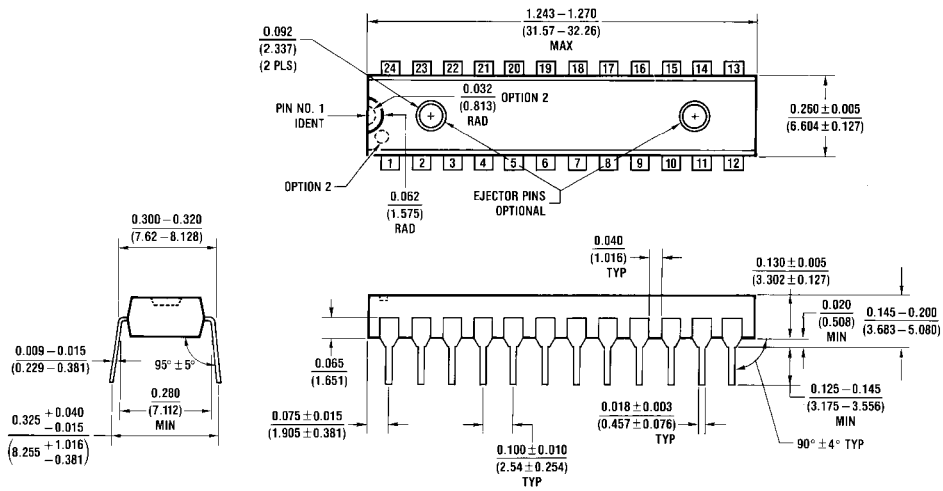
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0				4.5		ns
$t_S(L)$	$A_n$ or $B_n$ to CPA or CPB	4.0				4.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0				2.5		ns
$t_H(L)$	$A_n$ or $B_n$ to CPA or CPB	2.0				2.5		
$t_S(H)$	Setup Time, HIGH or LOW	1.0				1.5		ns
$t_S(L)$	$\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	4.0				4.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0				2.5		ns
$t_H(L)$	$\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	2.0				2.5		
$t_W(H)$	Pulse Width, HIGH or LOW	3.0				3.5		ns
$t_W(L)$	CPA or CPB	3.0				3.5		

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide  
Package Number N24C**

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