# High Speed CMOS Bus Interface 8, 9 & 10-bit Registers

**QS54/74FCT821T**
**QS54/74FCT823T**
**QS54/74FCT825T**

**QS54/74FCT2821T**
**QS54/74FCT2823T**
**QS54/74FCT2825T**

## FEATURES/BENEFITS

- Pin and function compatible to the 74F821/3/5 74FCT821/3/5 and 74FCT821T/3T/5T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

**FCT 821T/3T/5T**

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Iol = 48 mA Com., 32 mA Mil.

**FCT 2821T/3T/5T**

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Iol = 12 mA Com.

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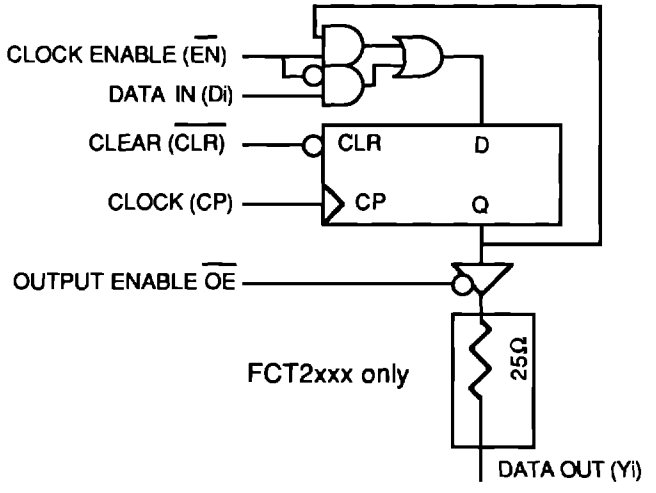
## DESCRIPTION

The QSFCT821T/823T/825T and QSFCT821T/823T/825T are 10, 9, and 8-bit high-speed CMOS TTL-compatible buffered registers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2821/3/5 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2821 series parts can replace the 821 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM

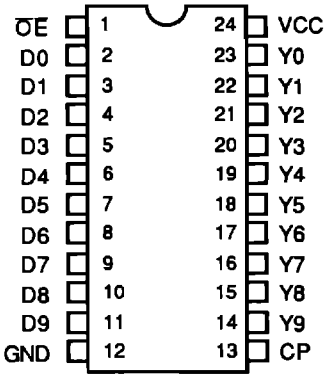


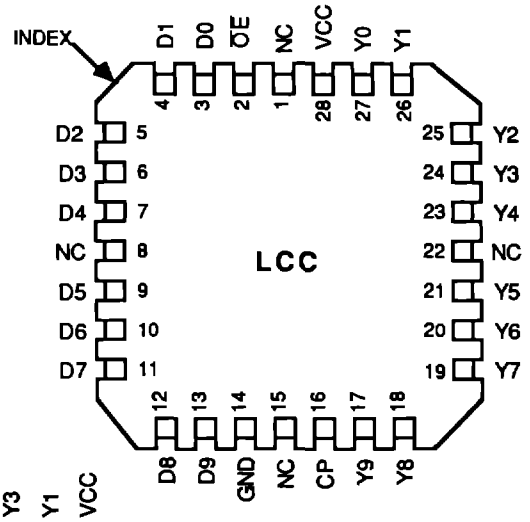
# PINOUTS

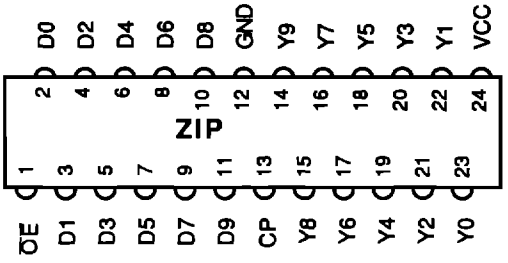
## FCT821 PIN CONFIGURATIONS

## FCT821 - 10-BIT REGISTER

### PDIP, SOIC, QSOP

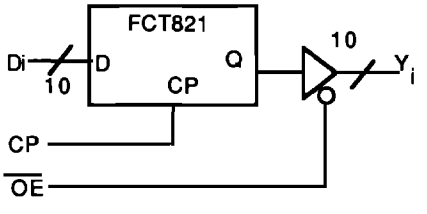



All packages are shown with the Top view

### FCT821 LOGIC SYMBOL

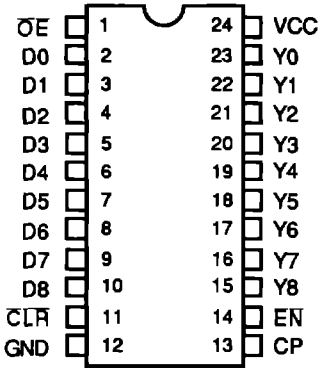


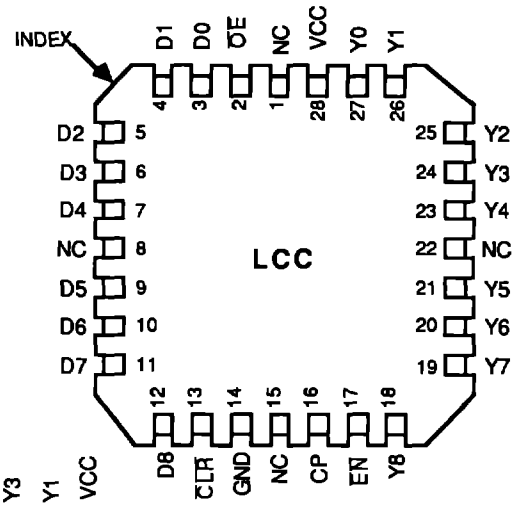

### PIN DESCRIPTIONS

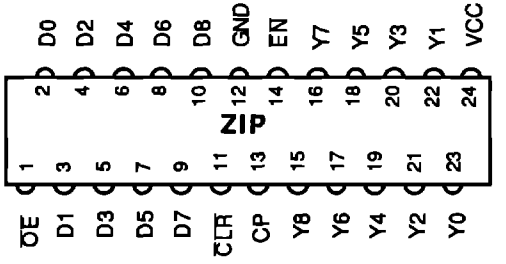
| Name | I/O | Function |
|---|---|---|
| Di | I | Data Inputs |
| Yi | O | Data Outputs - Three State |
| CP | I | Clock Pulse |
| OE | I | Output Enable |

## FCT823 - 9-BIT REGISTER

### PDIP, SOIC, QSOP

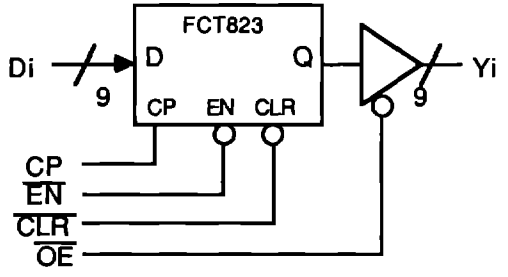



All packages are shown with the Top view

### FCT823 LOGIC SYMBOL

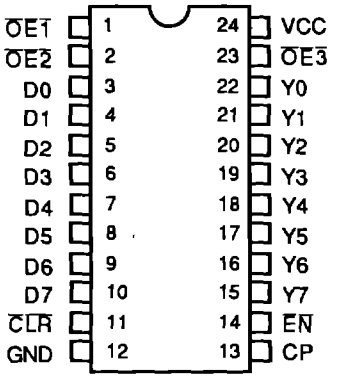


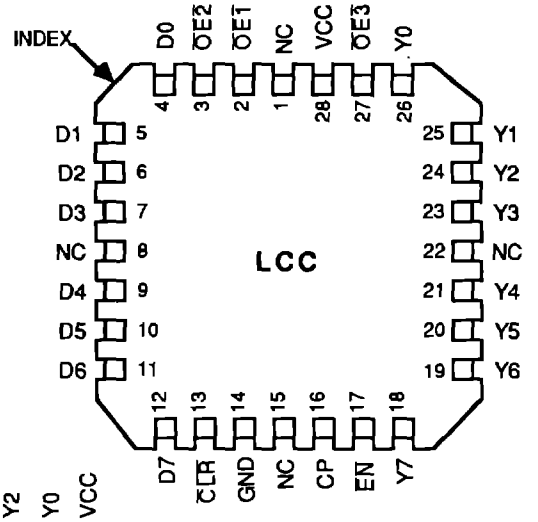

### PIN DESCRIPTIONS

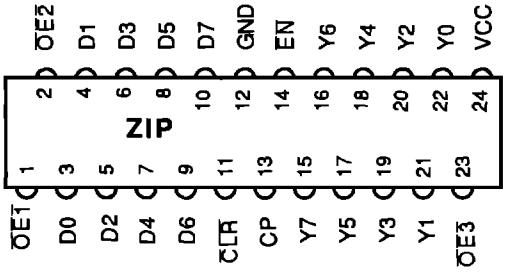
| Name | I/O | Function |
|---|---|---|
| Di | I | Data Inputs |
| Yi | O | Data Outputs - Three-State |
| OE | I | Output Enable |
| CP | I | Clock Pulse |
| EN | I | Clock Enable |
| CLR | I | Asynchronous Reset |

## FCT825 - 8-BIT REGISTER

**PDIP, SOIC, QSOP**

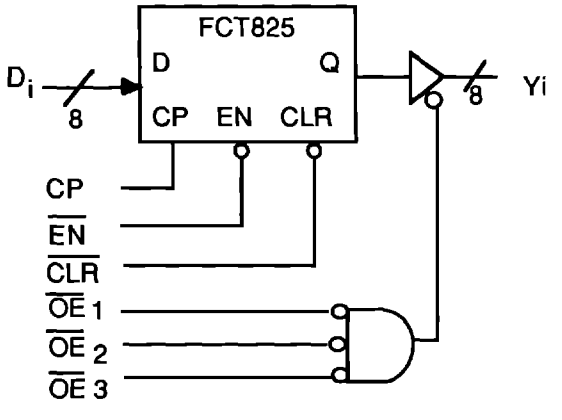



All packages are shown with the Top View

### FCT825 LOGIC SYMBOL




### PIN DESCRIPTIONS

| Name | I/O | Function |
|---|---|---|
| Di | I | Data Inputs |
| Yi | O | Data Outputs - Three State |
| $\overline{OE}$ | I | Output Enable |
| CP | I | Clock Pulse |
| $\overline{EN}$ | I | Clock Enable |
| $\overline{CLR}$ | I | Asynchronous Reset |

## FUNCTION TABLES - QSFCT821/823/825

| Inputs | | | | | Int. | O/P | Function |
|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{EN}$ | DI | CP | QI | YI | |
| H | X | L | L | ↑ | L | Z | High Z |
| H | X | L | H | ↑ | H | Z | |
| H | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | |
| H | H | L | L | ↑ | L | Z | Load |
| H | H | L | H | ↑ | H | Z | |
| L | H | L | L | ↑ | L | L | |
| L | H | L | H | ↑ | H | H | |

↑ = LOW-to-HIGH transition
NC = No Change from the previous state,
H = HIGH
L = LOW,
Z = High Impedance
Int. = Internal

For the 821, the Hi-Z and Load functions only apply as the $\overline{EN}$ and $\overline{CLR}$ are not present in these devices. For the 825, there are 3 output enables, and the composite output enable is asserted only when all the three are LOW. If any one of the three output enables are HIGH, the output is disabled.

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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage $V_O$ ..... -0.5V to 7.0V
DC Input Voltage $V_I$ ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with $V_I$<0.....-20 mA
DC Output Diode Current with $V_O$ <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
N=Number of Outputs, M=Number of inputs
Maximum Power Dissipation.....0.5 watts
$T_{STG}$Storage Temperature.....-65° to +165°C

## CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

| Pins | SOIC | QSOP | PDIP,LCC | ZIP | Unit |
|---|---|---|---|---|---|
| 1,3-11,13 | 4 | 4 | 5 | 7 | pF |
| 15-22 | 6 | 6 | 7 | 9 | pF |
| 2,14,23 | 8 | 8 | 9 | 10 | pF |

Note: Capacitance is characterized but not tested

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A$=0°C to 70°C, $V_{CC}$=5.0V±5% Military $T_A$=-55°C to 125°C, $V_{CC}$=5.0V±10%

| Symbol | Parameter | Test Conditions | | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|---|---|
| Vih | Input High Voltage | Logic HIGH for All Inputs | | 2.0 | - | - | Volts |
| Vil | Input LOW Voltage | Logic LOW for All Inputs | | - | - | 0.8 | |
| ΔVt | Input Hysterisis | Vtlh - Vthl for All Inputs | | - | 0.2 | - | |
| \|Iih\| \|Iil\| | Input Current Input HIGH or LOW | Vcc = MAX | 0 ≤ Vin < Vcc | - | - | 5 | µA |
| \|Ioz\| | Off State Output Current (Hi-Z) | Vcc = MAX, 0 ≤ Vin ≤ Vcc | | - | - | 5 | |
| Ios | Short Circuit Current FCTXXX | Vcc = MAX, Vo = GND (2,3) | | -60 | - | - | mA |
| Ior | Current Drive FCT2XXX | Vcc = Min, Vo =2.0V | | 50 | - | - | mA |
| Vic | Input Clamp Voltage | Vcc = MIN, Iin = 18 mA (3) | | - | -0.7 | -1.2 | Volts |
| Voh | Output HIGH Voltage FCTXXX & FCT2XXX | Vcc = MIN | Ioh = 15 mA (MIL) | 2.4 | - | - | Volts |
| | | | Ioh = 24 mA (COM) | 2.4 | - | - | |
| Vol | Output LOW Voltage FCTXXX | Vcc = MIN | Iol = 32 mA (MIL) | - | - | 0.50 | |
| | | | Iol = 48 mA (COM) | - | - | 0.50 | |
| | Output LOW Voltage FCT2XXX (25Ω) | Vcc = MIN | Iol = 12 mA (MIL) | - | - | 0.50 | |
| | | | Iol = 12 mA (COM) | - | | 0.50 | |
| Rout | Output Resistance FCT2XXX (25Ω) | Vcc = MIN | Iol = 12 mA (MIL) | 21 | 28 | 38 | Ω |
| | | | Iol = 12 mA (COM) | 24 | 28 | 35 | |

**Notes:**
1. Typical values indicate $V_{CC}$=5.0V and $T_A$=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

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## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions (1) | Min | Max | Unit |
|---|---|---|---|---|---|
| Icc | Quiescent Power Supply Current | Vcc = MAX, freq = 0<br>0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc | - | 1.5 | mA |
| ΔIcc | Supply Current per Input @ TTL HIGH | Vcc = MAX, Vin =3.4 V, freq = 0 (2) | - | 2.0 | |
| Qccd | Supply Current per input per mHz | Vcc = MAX, Outputs open and enabled<br>One bit toggling @ 50% duty cycle<br>Other inputs at GND or Vcc (3,4) | - | 0.25 | mA/ MHz |

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A$=0°C to 70°C, $V_{CC}$=5.0V±5% Military $T_A$=-55°C to 125°C, $V_{CC}$=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

| Symbol | Description | | Notes (1) | 821A 823A 825A 2821A 2823A 2825A | | 821B 823B 825B 2821B 2823B 2825B | | 821C 823C 825C | | 821D 823D | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t PHL t PLH | Clock to Y Delay $\overline{OE}$=low, FCT821/3/5 | Com | | | 10.0 | | 7.5 | | 6.0 | | 5.3 | ns |
| | | Mil | | | 11.5 | | 8.5 | | 7.0 | | | |
| | | Com | 2,3 | | 20.0 | | 15.0 | | 12.5 | | 12.5 | |
| | | Mil | 2,3 | | 20.0 | | 16.0 | | 13.5 | | | |
| | Clock to Y Delay $\overline{OE}$=low, FCT2821/3/5 | Com | | | 10.0 | | 7.5 | | | | | |
| | | Mil | | | 11.5 | | 8.5 | | | | | |
| | | Com | 2,3 | | 20.0 | | 15.0 | | | | | |
| | | Mil | 2,3 | | 20.0 | | 16.0 | | | | | |
| t S | Data to Cp Setup Time | Com | | 4.0 | | 3.0 | | 3.0 | | 3.0 | | |
| | | Mil | | 4.0 | | 3.0 | | 3.0 | | | | |
| t H | Data to Cp Hold Time | Com | | 2.0 | | 1.5 | | 1.5 | | 1.5 | | |
| | | Mil | | 2.0 | | 1.5 | | 1.5 | | | | |
| t ENS | $\overline{EN}$ to Cp Setup Time | Com | | 4.0 | | 3.0 | | 3.0 | | 3.0 | | |
| | | Mil | | 4.0 | | 3.0 | | 3.0 | | | | |
| t ENH | $\overline{EN}$ to Cp Hold Time | Com | | 2.0 | | 0.0 | | 0.0 | | 0.0 | | |
| | | Mil | | 2.0 | | 0.0 | | 0.0 | | | | |

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Cload = 300 pF
4) Cload = 5 pF

Commercial $T_A$=0°C to 70°C, $V_{CC}$=5.0V±5% Military $T_A$=-55°C to 125°C, $V_{CC}$=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

| Symbol | Description | | Notes (1) | 821A 823A 825A 2821A 2823A 2825A | | 821B 823B 825B 2821B 2823B 2825B | | 821C 823C 825C | | 821D 823D | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t CLR | $\overline{CLR}$ to Y Delay 823/5 | Com | | | 11.0 | | 9.0 | | 8.0 | | 7.0 | ns |
| | | Mil | | | 12.0 | | 9.5 | | 8.5 | | | |
| | $\overline{CLR}$ to Y Delay 2823/5 | Com | | | 11.0 | | 9 | | | | | |
| | | Mil | | | 12.0 | | 9.5 | | | | | |
| t REC | $\overline{CLR}$ to Cp Setup Time | Com | | 6.0 | | 6.0 | | 6.0 | | 6.0 | | |
| | | Mil | | 7.0 | | 6.0 | | 6.0 | | | | |
| t PWH t PWL | Clock Pulse Width High or Low | Com | 2 | 7.0 | | 6.0 | | 6.0 | | 6.0 | | |
| | | Mil | 2 | 7.0 | | 6.0 | | 6.0 | | | | |
| tPZH tPZL | Output Enable Time $\overline{OE}$ to Yi, FCT821-5 | Com | | | 12.0 | | 8.0 | | 7.0 | | 6.5 | |
| | | Mil | | | 13.0 | | 9.0 | | 8.0 | | | |
| | | Com | 2,3 | | 23 | | 15 | | 12.5 | | 12.5 | |
| | | Mil | 2,3 | | 25 | | 16 | | 13.5 | | | |
| | Output Enable Time $\overline{OE}$ to Yi, FCT2821-5 | Com | | | 12 | | 8.0 | | | | | |
| | | Mil | | | 13 | | 9.0 | | | | | |
| | | Com | 2,3 | | 23 | | | | | | | |
| | | Mil | 2,3 | | 25 | | | | | | | |
| tPHZ tPLZ | Output Disable Time $\overline{OE}$ to Yi | Com | 2,4 | | 7 | | 6.5 | | 6.2 | | 6.2 | |
| | | Mil | 2,4 | | 8 | | 7 | | 6.2 | | | |
| | | Com | 2 | | 9 | | 7.5 | | 6.5 | | 6.5 | |
| | | Mil | 2 | | 10 | | 8 | | 6.5 | | | |

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Cload = 300 pF
4) Cload = 5 pF