COMPLETE MONOLITHIC 12-BIT D/A CONVERTER

FEATURES

- Single Chip Construction
- On-Board Output Amplifier
- Low Power Dissipation: 300 mW
- Monotonicity Guaranteed Over Temperature
- Guaranteed for Operation With ±12V Supplies
- Buried Zener Reference
- ±1/2 LSB Max Nonlinearity

PRODUCT DESCRIPTION

The SP DAC87 is a 12-bit digital-to-analog converter with both a high stability voltage reference and output amplifier combined on a single monolithic chip.

Innovative circuit design reduces the total power consumption to 300 mW which not only improves reliability but also improves long term stability.

The SP DAC87 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The SP DAC87 is available in a hermetically sealed ceramic package and is specified for -55°C to +125°C temperature operation. MIL-STD-883 processing is available.

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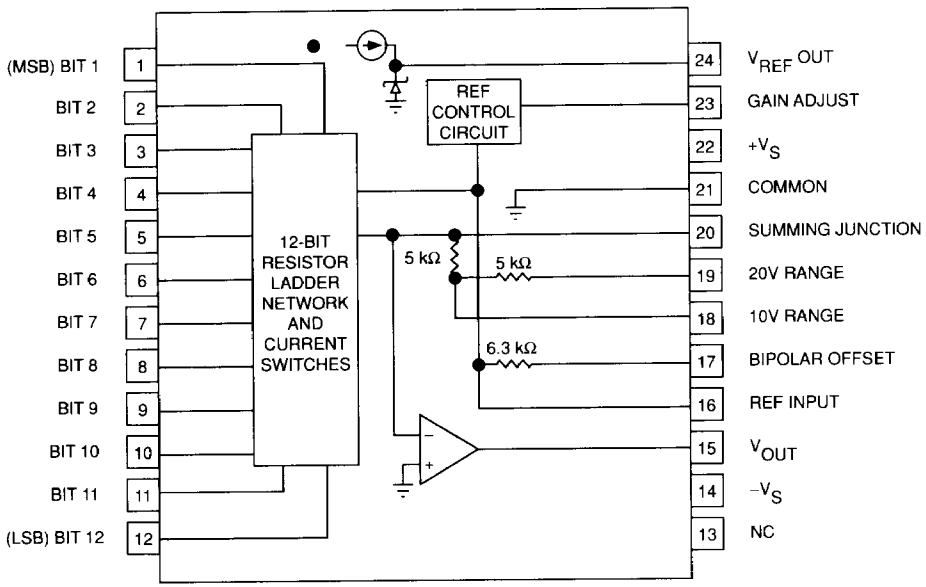
FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground ..... 0V to +18V
$-V_S$ to Power Ground ..... 0V to -18V
Digital Input (Pins 1 to 12) to Power Ground ..... -1.0V to +7V
Ref In to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span R to Reference Ground ..... ±12V
20V Span R to Reference Ground ..... ±24V
Ref Out ..... Indefinite Short to Power Ground or $+V_S$

(T_A = +25°C, rated power supplies unless otherwise noted.)

MODEL SP DAC87	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Binary - CBI			12	Bits
Logic Levels (TTL Compatible)				
V_{IH} (Logic "1")	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			250	µA
I_{IH} (V_{IL} = 0.8V)			100	µA
TRANSFER CHARACTERISTICS ACCURACY				
Linearity Error @ +25°			±1/2	LSB[1]
T_A @ T_{min} to T_{max}		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C			±3/4	LSB
T_A @ T_{min} to T_{max}			±1	LSB
Gain Error[2]		±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	-55		+125	°C
DRIFT (T_{min} to T_{max})				
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]				
Unipolar		±0.18	±0.3	% of FSR
Bipolar		±0.14	±0.24	% of FSR
Gain				
Including Internal Reference			±20	ppm of FSR/°C
Excluding Internal Reference			±10	ppm of FSR/°C
Unipolar Offset			±3	ppm of FSR/°C
Bipolar Offset			±10	ppm of FSR/°C
CONVERSION SPEED				
Settling Time to ±0.01% of FSR for FSR change (2 kΩ||500 pF load)				
with 10 kΩ Feedback		3	4	µs
with 5 kΩ Feedback		2	3	µs
For LSB Change		1		µs
Slew Rate	10			V/µs

(T_A = +25°C, rated power supplies unless otherwise noted.)

MODEL SP DAC87	MIN	TYP	MAX	UNITS
ANALOG OUTPUT				
Ranges - CBI		±2.5, ±5, ±10		V
		+5, +10		
Output Current	±5			mA
Output Impedance (dc)		0.05		Ω
Short Circuit Current			40	mA
Internal Reference Voltage (V_R)	+6.23	+6.3	+6.37	V
Output Impedance		1.5		Ω
Max External Current[6]			+2.5	mA
Tempco of Drift			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY				
±15V ±10%, 5V supply when applicable			±0.002	% of FSR/% V_S
±12V ±5%			±0.002	% of FSR/% V_S
POWER SUPPLY REQUIREMENTS				
Rated Voltages		±15		V
Range				
Analog Supplies	±11.4[7]		±16.5	V
Logic Supplies	+4.5		+5.5	V
Supply Drain				
+12, +15V		5	10	mA
-12, -15V		14	20	mA
TEMPERATURE RANGE				
Specification	-55		+125	°C
Operating	-55		+125	°C
Storage	-65		+150	°C

NOTES

1. Least Significant Bit.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V range.
4. Gain and offset errors adjusted to zero at +25°C.
5. C_F = 0, see Figure 1.
6. Maximum with no degradation of specifications, must be a constant load.
7. A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

DIGITAL INPUT CODES

The SP DAC87 accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	CSB COMPL. STRAIGHT BINARY	COB COMPL. OFFSET BINARY	CTC* COMPL. TWO'S COMPL.
000000000000	+Full Scale	+ Full Scale	-1 LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	Mid-Scale	-1 LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 1 1/2 LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each SP DAC87 model at the lowest operating temperature, +25°C and the highest operating temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0 1 1 1 . . . 11 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25 pF as shown in Figure 1.

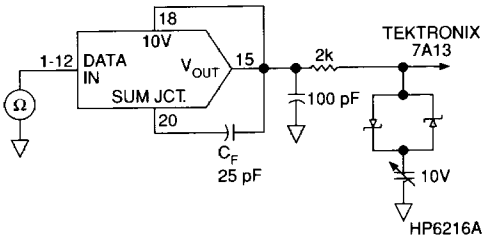


FIGURE 1
SETTLING TIME CIRCUIT

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. An external buffer amplifier is recommended if this reference will result in gain variations. All gain adjustments should be made under constant load conditions.

USING THE SP DAC87

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1 µF electrolytic recommended) should be located close to the SP DAC87. Electrolytic capacitors, if used, should be paralleled with 0.01 µF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100 ppm/°C or less. The 3.9 MΩ and 10 MΩ resistors (20% carbon or better) should be located close to the SP DAC87 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 2 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01 µF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

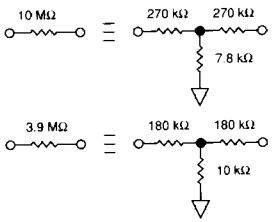


FIGURE 2
EQUIVALENT RESISTANCES

Offset Adjustment. For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

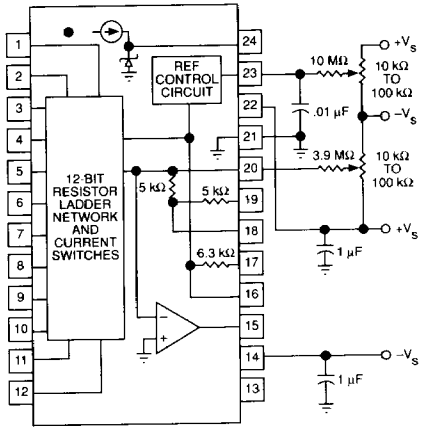


FIGURE 3
EXTERNAL ADJUSTMENT AND VOLTAGE SUPPLY CONNECTION DIAGRAM

DIGITAL INPUT		ANALOG OUTPUT	
12 BIT RESOLUTION		VOLTAGE*	
MSB	LSB	0 to +10V	±10V
000000000000		+9.9976V	+9.9951V
011111111111		+5.0000V	0.0000V
100000000000		+4.9976V	4.88 mV
111111111111		0.0000V	-10.0000V
1 LSB		2.44 mV	-0.0049V

* To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

Table II. Digital Input/Analog Output

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VOLTAGE RANGES

Internal scaling resistors provided in the SP DAC87 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 4).

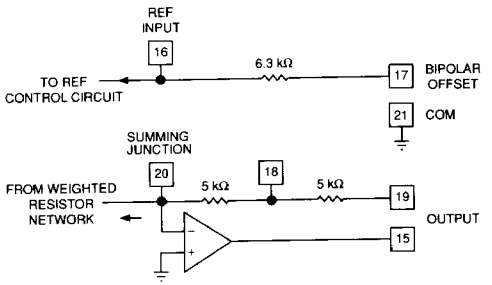


FIGURE 4
OUTPUT AMPLIFIER VOLTAGE RANGE
SCALING CIRCUIT

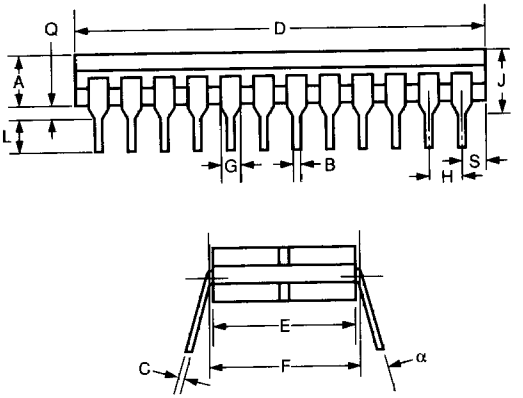
Gain and offset drift are minimized in the SP DAC87 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 4 microseconds for a 10 kΩ feedback resistor; 3 microseconds for a 5 kΩ feedback resistor when using the compensation capacitor shown in Figure 1.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 15 TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO	CONNECT PIN 16 TO
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections

ORDERING INFORMATION

MODEL	LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
SP DAC87-CBI-V/B	±1/2 LSB	-55°C to +125°C	MIL-STD-883C



SYMBOL	INCHES
A	.180
B	.018
C	.012
D	1.27
E	.535
F	.615
G	.070
H	.110
J	.225
L	.150
Q	.045
S	.090
α	15°