8 K × 8 / 3.3 Volts High Speed CMOS SRAM

Short description. Please refer to the full datasheet available on TEMIC web for detailed technical information.

Description

The L 65764 is a high speed CMOS static RAM organized as 8192 × 8 bits. It is manufactured using TEMIC high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 216 mW.

The L 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.

Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.

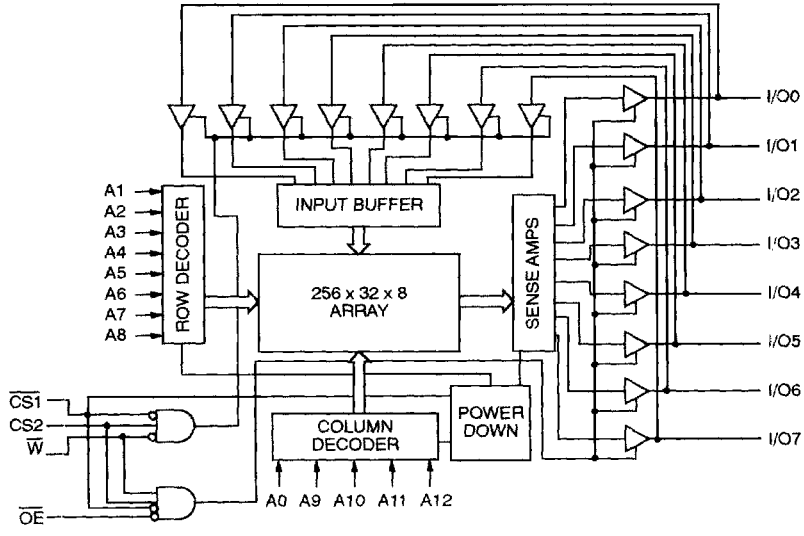
L 65764 provides fast access time with 3,3 volts power supply, perfectly designed for portable applications (PC cache memory... etc).

Features

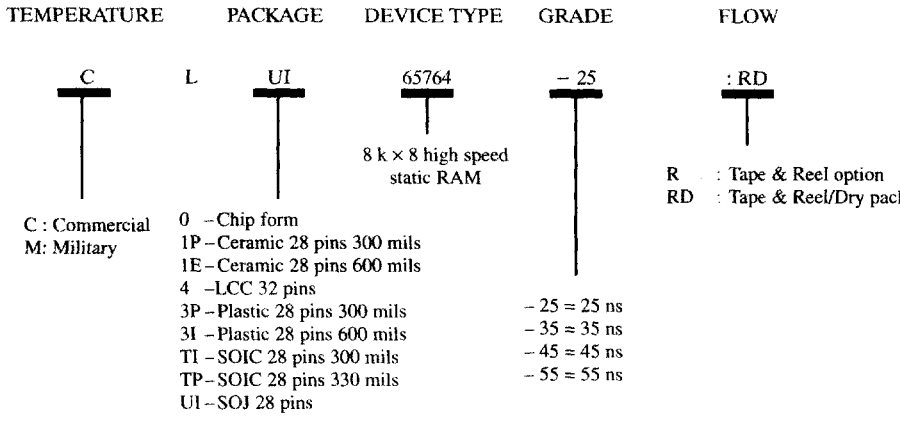
- Single supply 3.3 V ± 0.3 V
- Fast access time
  Commercial : 25/35/45/55 ns (max)
  Military : 35/45/55 ns (max)
- Low power consumption
  Active : 216 mW (typ)
  Standby : 36 mW (typ)
- 300 and 600 mils width package
- Asynchronous
- Capable of withstanding greater than 2000 V electrostatic discharge

Interface

Block Diagram



Ordering Information



Military Version

The following table gives package/access time/process flow available combinations

Temp. range	Packages	Access Time (ns)			Std process 65764
		35 (K)	45 (M)	55 (N)	Mil flows
M	1	X	X	X	X
	1E	X	X	X	X
	4	X	X	X	X
	0	X	X	X	X

X = call sales office for availibility