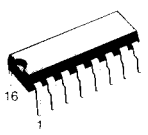
T54LS259
T74LS259

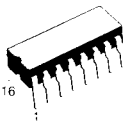
8-BIT ADDRESSABLE LATCH

DESCRIPTION

The T54LS259/T74LS259 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital sistems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enables.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

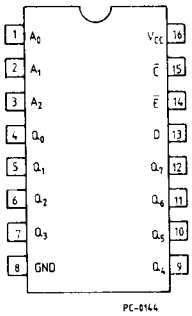
ORDERING NUMBERS:

T54LS259 D2
T74LS259 D1
T74LS259 B1
T74LS259 C1
T74LS259 M1

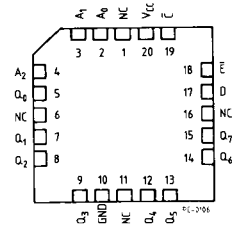
- SERIAL-TO-PARALLEL CONVERSION
- EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY
- EASILY EXPANDABLE
- COMMON CLEAR
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

PIN NAMES

A_0,A_1,A_2	Address Inputs
D	Data Input
$\overline{E}$	Enable (Active LOW) Input
$\overline{C}$	Clear (Active LOW) Input
Q_0 to Q_7	Parallel Latch Outputs

TRUTH TABLE - PRESENT OUTPUT STATES

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{n-1} →								Memory
H	L	L	L	L	L	L	Q_{n-1}	Q_{n-1}	Q_{n-1} →					Adressable
H	L	H	L	L	L	H	Q_{n-1}	Q_{n-1} →						Latch
H	L	L	H	L	L	Q_{n-1}	L	Q_{n-1} →						
H	L	H	H	L	L	Q_{n-1}	H	Q_{n-1} →						
H	L	L	H	H	H	Q_{n-1} →						Q_{n-1}	L	
H	L	H	H	H	H	Q_{n-1} →						Q_{n-1}	H	

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	30	mA

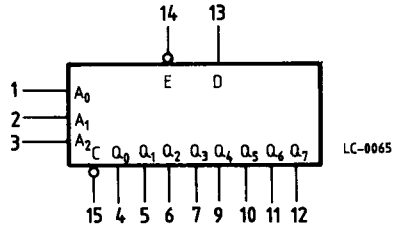
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

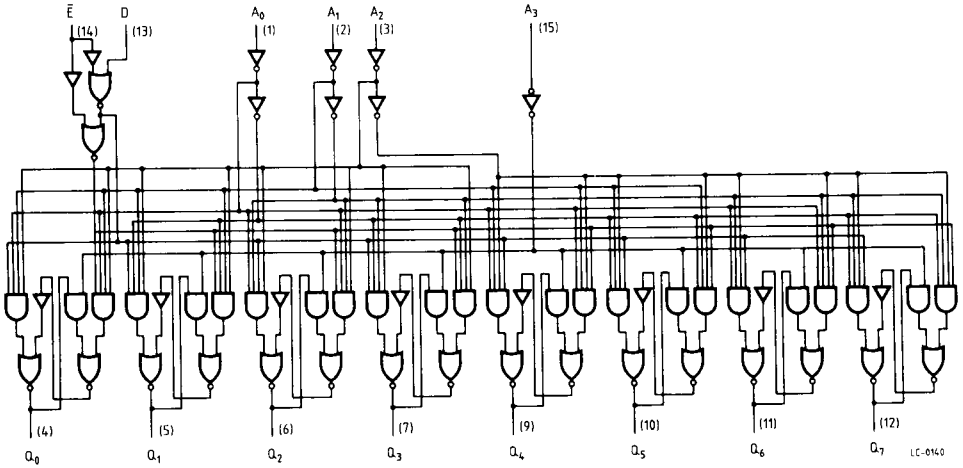
GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS259D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS259XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTIONAL DESCRIPTION

The LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The address latch will follow three data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address input. In one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The truth table below summarizes the operations of the LS259.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input Logical HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input Logical LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.4	3.1				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$				20 40	V_{CC} = MAX, V_{IN} = 2.7V		μA
	Input HIGH Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$				0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V		mA
I_{IL}	Input LOW Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$				−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current			20	36	V_{CC} = MAX		mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Turn-Off Delay, Enab. to Out. Turn-On Delay, Enab. to Out.		22 15	35 24	Fig. 1	V_{CC} = 5.0V C_L = 15pF	ns
t_{PLH} t_{PHL}	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	32 21	Fig. 2		ns
t_{PLH} t_{PHL}	Turn-Off Delay, Addr. to Out. Turn-On Delay, Addr. to Out.		24 18	38 29	Fig. 3		ns
t_{PHL}	Turn-On Delay, Clear to Output		17	27	Fig. 5		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_sH	Set-up Time HIGH, Data to Enable	20	13		Fig. 4	$V_{CC} = 5.0V$	ns
t_hH	Hold Time HIGH, Data to Enable	0	−7.0				
t_sL	Set-up Time LOW, Data to Enable	15	7.0				ns
t_hL	Hold Time LOW, Data to Enable	0	10				
$t_sA\text{-}\overline{E}$	Set-up Time, Address to Enable (Note 4)	0	−7.0		Fig. 6		ns
$t_{pW}\overline{E}$	Enable Pulse Width	17	12		Fig. 1		ns

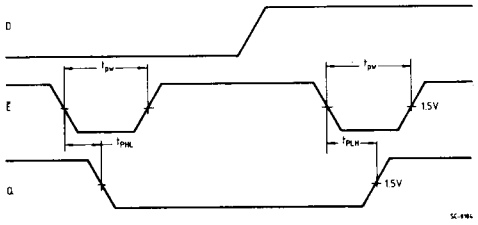
Notes:

4) The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

5) The shaded areas indicate when the inputs are permitted to change for predictable output performance.

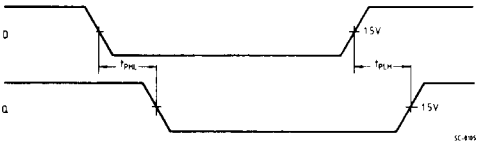
AC WAVEFORMS

Fig. 1 Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width



OTHER CONDITIONS: $\overline{C} = H$, A = STABLE

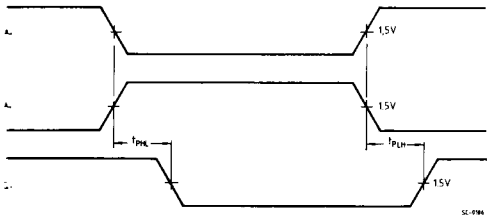
Fig. 2 Turn-On and Turn-Off Delays, Data to Output



OTHER CONDITIONS: $\overline{E} = L$, $\overline{C} = H$, A = STABLE

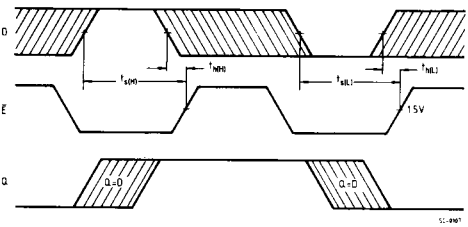
AC WAVEFORMS (continued)

Fig. 3 Turn-On and Turn-Off Delays, Address to Output



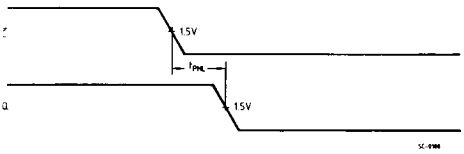
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 Set-up and Hold Time, Data to Enable



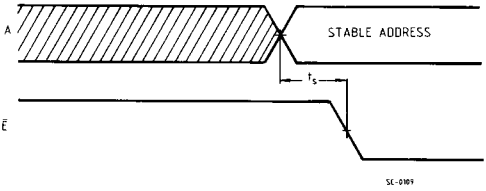
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 Turn-On Delay, Clear to Output



OTHER CONDITIONS: $\overline{E}$ = H

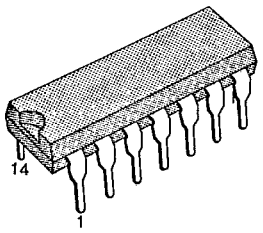
Fig. 6 Set-up Time, Address to Enable (see notes 4 and 5)

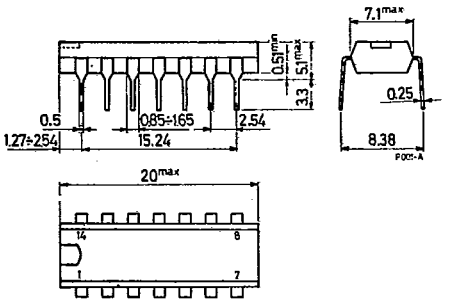


OTHER CONDITIONS: $\overline{C}$ = H

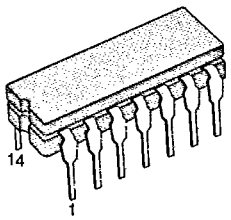
Packages

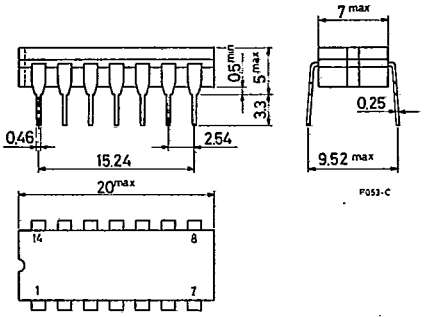
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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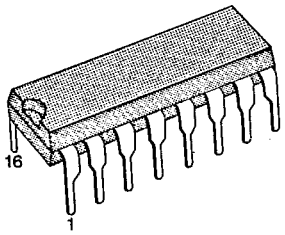
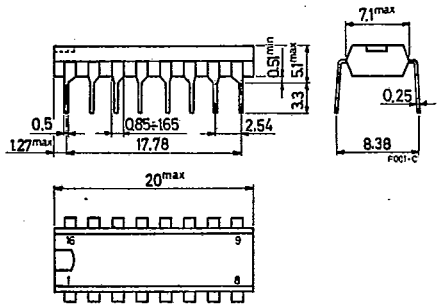
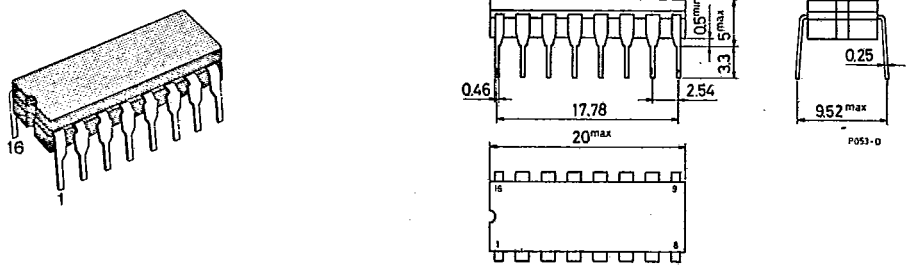




Packages

16-LEAD CERAMIC DIP



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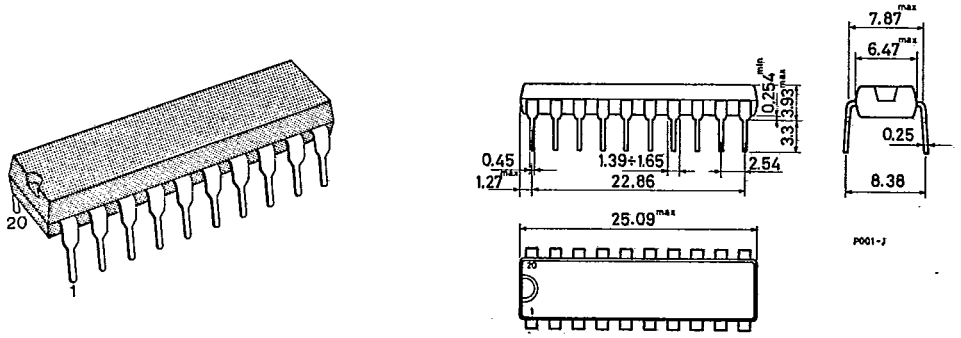
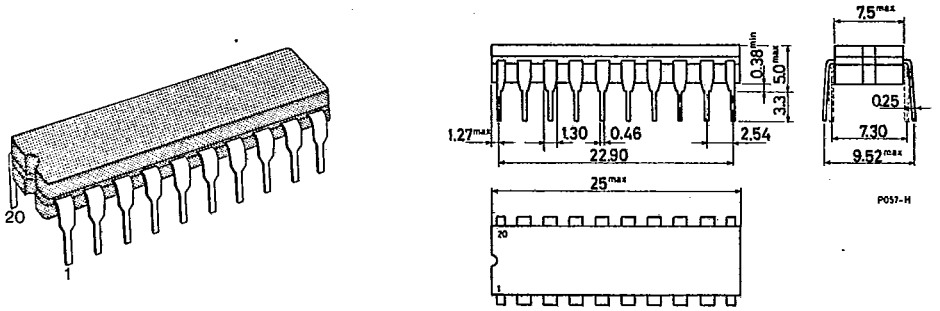
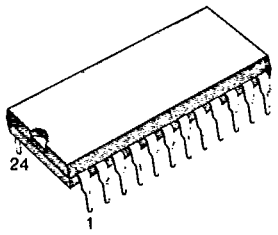


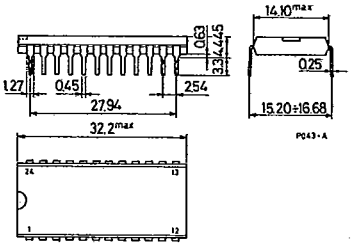
20-LEAD CERAMIC DIP



Packages

24-LEAD PLASTIC DIP





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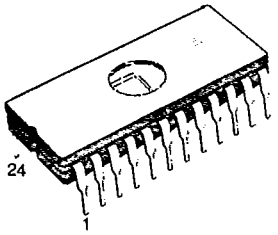
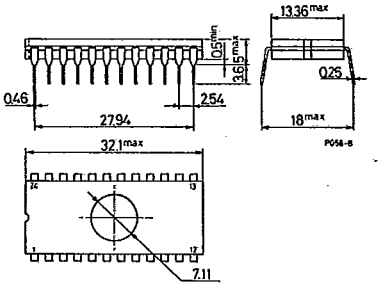
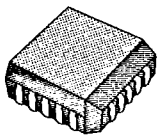
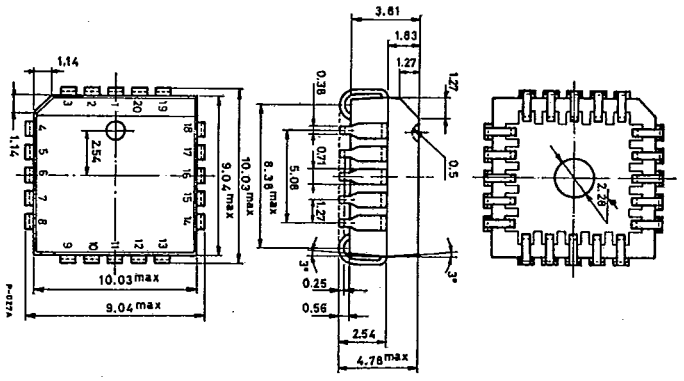




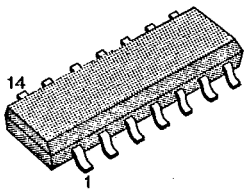
CHIP CARRIER 20 LEAD PLASTIC

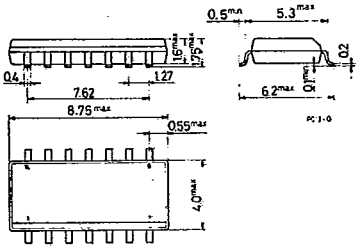




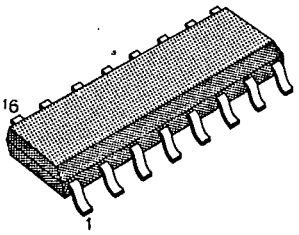
Packages

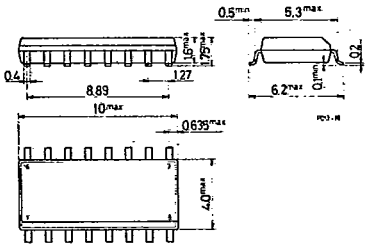
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.