

Recent Additions CD54AC161/3A CD54ACT161/3A

Synchronous Presettable Binary Counters Asynchronous Reset

The RCA CD54AC161 and CD54ACT161 are Synchronous presettable binary counters that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC/ACT161 are asynchronously reset. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

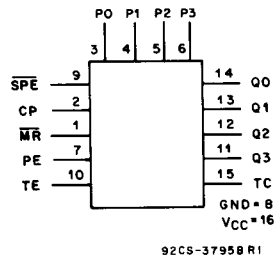
A LOW level on the Synchronous Parallel Enable input, \overline{SPE} , disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for \overline{SPE} are met).

The counters are reset with a LOW level on the Master Reset input, \overline{MR} .

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the \overline{SPE} , PE, TE, and CP inputs.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54AC161 and CD54ACT161 are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

Package Specifications (See Section 11, Fig. 11)

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
				+25		-55 to +125			
				MIN.	MAX.	MIN.	MAX.		
Quiescent Supply Current (MSI)	I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P_n	0.13
CP	1
\overline{MR} , TE	0.83
\overline{SPE}	0.67
PE	0.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections

Identical to CD54HC/HCT161/3A, page 5-66.

Recent Additions

CD54AC161/3A

CD54ACT161/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125° C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	t _{PLH}	1.5	—	207	ns
	t _{PHL}	3.3*	4.3	23.1	
CP to Qn (SPE LOW)	t _{PLH}	1.5	—	207	ns
	t _{PHL}	3.3	4.3	23.1	
CP to TC	t _{PLH}	1.5	—	209	ns
	t _{PHL}	3.3	4.4	23.4	
TE to TC	t _{PLH}	1.5	—	129	ns
	t _{PHL}	3.3	2.6	14.4	
$\overline{\text{MR}}$ to Qn	t _{PLH}	1.5	—	207	ns
	t _{PHL}	3.3	4.3	23.1	
$\overline{\text{MR}}$ to TC	t _{PLH}	1.5	—	207	ns
	t _{PHL}	3.3	4.3	23.1	
Power Dissipation Capacitance	C _{PD} §	—	—	—	pF
Input Capacitance	C _I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125° C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	t _{PLH} t _{PHL}	5†	2.8	16.5	ns
CP to Qn (SPE LOW)		5	2.8	16.5*	ns
CP to TC		5	2.9	16.7	ns
TE to TC		5	1.8	10.8*	ns
$\overline{\text{MR}}$ to Qn		5	2.8	16.5*	ns
$\overline{\text{MR}}$ to TC		5	2.8	16.5	ns
Power Dissipation Capacitance	C _{PD} §	—	—	—	pF
Input Capacitance	C _I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per device.

For AC, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$

For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

(Limits with black dots (*) are tested 100%.)