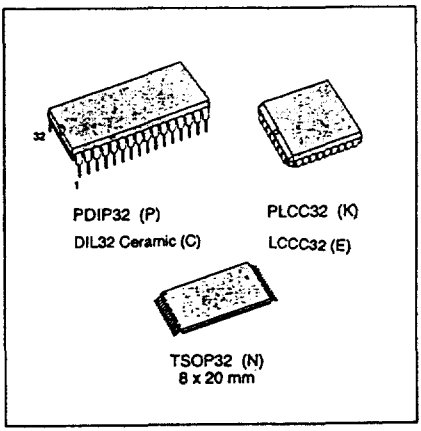
PRELIMINARY

M29F040

CMOS 4 Megabit (512K x 8, 8 sectors) SINGLE SUPPLY FLASH MEMORY

- VERY FAST ACCESS TIME : 70 ns
- 5 V ± 10 % SUPPLY VOLTAGE for PROGRAM and ERASE OPERATIONS
- 5 V ± 10 % SUPPLY VOLTAGE in READ OPERATIONS
- 10 µs TYPICAL PROGRAMMING TIME
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E.C. Status
- MEMORY ERASE in SECTORS
  - 8 Sectors of 64K Bytes each
  - Sector Protection
  - Multisector Erase
- ERASE SUSPEND and RESUME
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- LOW POWER CONSUMPTION
  - 25 µA Typical in Standby
- STANDARD EPROM/OTP MEMORY PACKAGES : TSOP32, PLCC32 and PDIP32, CERAMIC DIL32, LCCC32
- EXTENDED TEMPERATURE RANGES
  - 55 to + 125° C, MIL STD 883 quality level



DESCRIPTION

The M29F040 is a non-volatile memory that may be erased electrically at the sector level, and programmed Byte-by-Byte.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

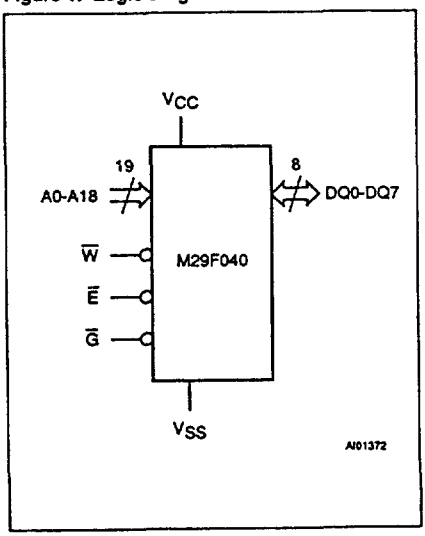


Figure 2A. DIP Pin Connections

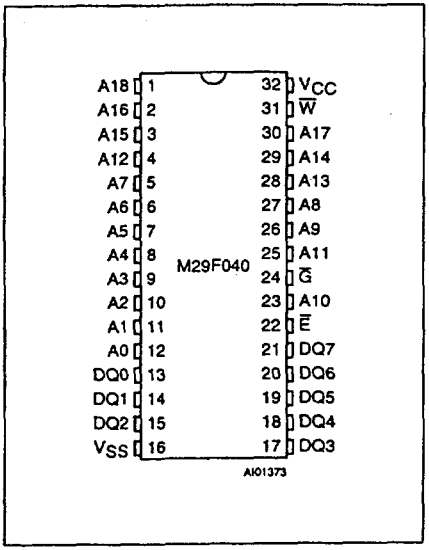


Figure 2B. LCC Pin Connections

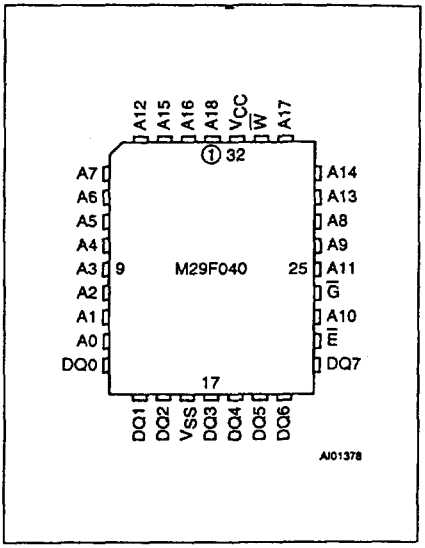
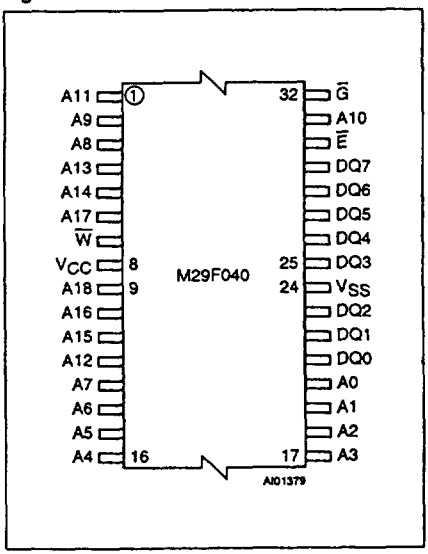


Figure 2C. TSOP Pin Connections



DESCRIPTION (cont'd)

The interface is directly compatible with most microprocessors. PDIP32, PLCC32 and TSOP32 (8 x 20mm) packages are used. Both normal and reverse pin outs are available for the TSOP32 package.

Organisation

The Organisation is 512K x 8 bits with Address lines A0-A18 and Data Inputs/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable Inputs.

Erase and Program are performed through the internal Program/Erase Controller (P/E.C.).

Data Outputs bits DQ7 and DQ6 provide polling or toggle signals during Automatic Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller.

Sectors

Erasure of the memory is in sectors. There are 8 sectors of 64K bytes each in the memory address space. Erasure of each sector takes typically 1.5 seconds and each sector can be programmed and erased over 100,000 cycles. Each sector may separately be protected and unprotected against program and erase. Sector erasure may be sus-

Table 2. Absolute Maximum Ratings(1)

Symbol	Parameter	Value	Unit
T_C	Case temperature	–55 to +125	°C
T_{STG}	Storage temperature	–65 to 150	°C
V_{IO}(2)	Input or Output voltages	–0.6 to 7	V
V_{CC}	Supply voltage	–0.6 to 7	V
V_{A9}(2)	A9 voltage	–0.6 to 13.5	V

Note : 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ragings" may cause permanent damage to the device. These are stess ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposutre to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. Minimum Voltage may undershoot to –2 V during transisiton and for less than 20 ns.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}

pended, while data is read from other blocks of the memory, and then resumed.

Bus Operations

Seven operations can be performed by the appropriate bus cycles, Read Array, Read Electronic Signature, Output Disable, Standby, Protect Sector, Unprotect Sector, and Write the Command of an Instruction.

Command Interface

Command Bytes can be written to a Command Interface (C.I.) latch to perform Reading (from the Array or Electronic Signature), Erasure or Programming. For added data protection, command execution starts after 4 or 6 command cycles. First, second, fourth and fifth cycles are used to input a code sequence to the Command Interface (C.I.). This sequence is equal for all P/E.C. instructions. Command itself and its confirmation - if it applies - are given on the third and fourth cycles.

Instructions

Seven instructions are defined to perform Read Memory Array, Read Electronic Signature, Auto Program, Sector Auto Erase, Auto Bulk Erase, Sector Erase Suspend and Sector Erase Resume. The internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides Data Polling, Toggle, and Status data to indicate completion of Program and Erase Operations.

Instructions are composed of up to six cycles. The first two input a code sequence to the Command Interface which is common to all P/E. C. instructions (see Table 7 for Command Descriptions). The third cycle inputs the instruction set up command instruction to the Command Interface. Subsequent cycles output the addressed data for Read operations. For added data protection, the instructions for program and sector or bulk erase require further command inputs. For a Program instruction, the

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	0E2h

Table 5. Sector Protection Status

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A16	A17	A18	Other Addresses	DQ0 - DQ7
Protected Sector	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	01h
Unprotected Sector	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	00h

Note: SA = Address of sector being checked

DESCRIPTION (cont'd)

fourth command cycle inputs the address and data to be programmed. For an Erase instruction (sector or bulk), the fourth and fifth cycles input a further code sequence before the Erase confirm command on the sixth cycle. Byte programming takes typically 10µs while erase is performed in typically 1.5 seconds.

Erasure of a memory sector may be suspended, in order to read data from another sector, and then resumed. Data Polling, Toggle and Error data may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

DEVICE OPERATION

Signal Descriptions

A0-A18 Address Inputs. The address inputs for the memory array are latched during a write operation. The A9 address input is used also for the Electronic Signature read and Sector Protect verification. When A9 is raised to V_{ID}, either a Read Manufacturer Code, Read Device Code or Verify Sector Proctection is enabled depending on the combination of levels on A0, A1 and A6. When A0, A1 and A6 are Low, the Electronic Signature Manufacturer code is read, when A0 is High and A1 and A6 are Low, the Device code is read, and when A1 is High and A0 and A6 are low, the Sector Protection Status is read.

DQ0-DQ7 Data Input/Outputs. The data input a byte to be programmed or a command written to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output is from the memory Array, the Electronic Signature, the Data Polling bit (DQ7), the Toggle Bit (DQ6), the Error bit (DQ5) or the Erase Timer bit (DQ3). Ouputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Addresses are then latched on the falling edge of $\overline{E}$ while datas on the rising edge of $\overline{E}$.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation. $\overline{G}$ is forced to V_{ID} level during Sector Protect and Sector Unprotect operations.

$\overline{W}$ Write Enable. This input controls writing to the Command Register and Address and Data latches. Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Table 6A. Instructions

Mne.	Instr.	Cyc.	1st Cycle			2nd Cycle			3rd Cycle			4th Cycle		
			Op.	Addr. [1,2]	Data	Op.	Addr. [1,2]	Data	Op.	Addr. [1,2]	Data	Op.	Addr. [1]	Data
RD	Read/ Reset Memory Array	1+	Write	X	0F0h	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RD	Read Memory Array	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	0F0h	Read	Read Address	Data
RSIG	Read Electronic Signature	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	90h	Read [2,3]	Signature Address	Signature
RSP	Read Sector Protection	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	90h	Read [2,4]	Protection Address	Protect Status [4]
PG	Program	4	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	0A0h	Write	Address	Data Input
SE	Sector Erase	6	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	80h	Write	x5555h [5]	0AAh
BE	Bulk Erase	6	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	80h	Write	x5555h [5]	0AAh
ES	Erase Suspend	1	Write	X	0B0h	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase.								
ER	Erase Resume	1	Write	X	30h	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time								

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
3. Signature Address bits A0, A1, A6 at V_L will output Manufacturer code (20h). Address bits A0 at V_H and A1, A6 at V_L will output Device code (0E2h).
4. Protection Address: A0, A6 at V_L and A1 at V_H, other addresses within the sector to be checked A16, A17, A18 define this Sector Address.
5. Address bits A16, A17, A18 are don't care for coded address inputs
6. Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed.

Table 6B. Instructions

Mne.	Instr.	Cyc.	5th Cycle			6th Cycle			7th Cycle		
			Op.	Addr. [1]	Data	Op.	Addr.	Data Out	Op.	Addr.	Data Out
RD	Read/ Reset Memory Array	1+	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RD	Read Memory Array	3+	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RSIG	Read Electronic Signature	3+	Read [2,3]	Signature Address	Signature	Read [2,3]	Signature Adress	Signature	Read [2,3]	Signature Adress	Signature
RSP	Read Sector Protection	3+	Read [2,4]	Protection Address	Protect Status [4]	Read [2,4]	Protection Address	Protect Status [4]	Read [2,4]	Protection Address	Protect Status [4]
PG	Program	4	Read Data Polling or Toggle Bit until Program completes								
SE	Sector Erase	6	Write	x2AAAh [5]	55h	Write	Sector Address	30h	Write [5]	Additional Sector	30h
BE	Bulk Erase	6	Write	x2AAAh [5]	55h	Write	x5555h [5]	10h	Read Data Polling or Toggle bit until Erase completes or Erase is suspended another time		
ES	Erase Suspend	1	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase.								
ER	Erase Resume	1	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time								

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
3. Signature Address bits A0, A1, A6 at V_L will output Manufacturer code (20h). Address bits A0 at V_H and A1, A6 at V_L will output Device code (0E2h).
4. Protection Address: A0, A6 at V_L and A1 at V_H, other addresses within the sector to be checked A16, A17, A18 define this Sector Address.
5. Address bits A16, A17, A18 are don't care for coded address inputs
6. Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed.

Memory Sectors

The memory sectors of the M29F040 are shown in Figure 5. The memory array is divided in 8 sectors of 64K bytes. Each sector can be erased separately or any combination of sectors can be erased simultaneously. The Sector Erase operation is managed automatically by the P/E.C. The operation can be suspended in order to read from any another sector, and then resumed.

Sector Protection provides additional data security. Each sector can be separately protected or unprotected against Program or Erase. Bringing A9 and $\overline{G}$ to V_{ID} initiates protection, while bringing A9, $\overline{G}$ and $\overline{E}$ to V_{ID} cancels the protection. The sector affected is addressed by the inputs on A16, A17, and A18.

Table 7. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Bulk Erase Confirm
30h	Sector Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Sector protection Status
0A0h	Program
0B0h	Erase Suspend
0F0h	Read Array/Reset

Table 8. Status Register

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase on Going	
		DQ	Program Complete	
		$\overline{DQ}$	Program on Going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program on Going	Sucessive read output complementary datas on DQ6 while Programming or Erase operations are going on. DQ6 remain at constant level when P/E.C. operations are completed.
		'-0-0-0-0-0-0-0-'	Program ('0' on DQ6) Complete	
		'-1-1-1-1-1-1-1-'	Erase or Program ('1' on DQ6) Complete	
5	Error Bit	'1'	Program or Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
		'0'	Program or Erase Success	
4		'1'		
		'0'		
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES). Additional sector to be erased in parallel can be entered to the P/E.C.
		'0'	Erase Timeout Period on Going	
2				
1				
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

Table 9. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

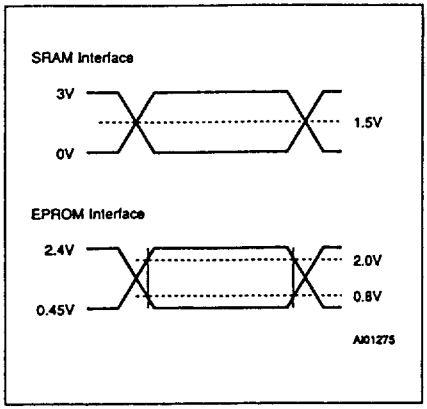


Figure 4. AC Testing Load Circuit

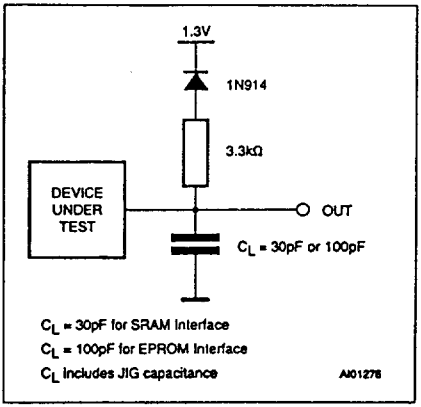


Table 10. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

7

Operations

Operations are defined as specific bus cycles and signals which allow Memory Read, Command Write, Output Disable, Standby, Read Status Bits, Sector Protect/Unprotect, Sector Protection Check and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD and RSIG, and Status Bits).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs last.

Figure 5. Memory Map and Sector Address Table

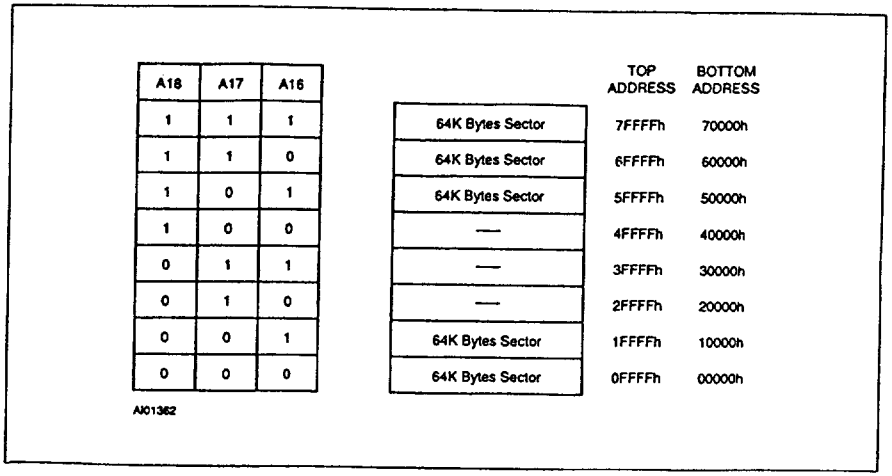


Table 11. DC Charecteristics
(T_C = –55 to +125° C ; VCC = 5 V ± 10 %)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 6MHz		40	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC4}	Supply Current (Program or Erase)	Byte program, Sector or Bulk Erase in progress		60	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V		V
		I_{OH} = –2.5mA	0.85 x V_{CC}		V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	12.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		50	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		3.2	4.2	V

Table 12A. Read AC Characteristics
(T_C = −55 to +125°C)

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from dhe memory, the manufacturer's code for TCS is 20h, and the device codes is E2h for the M29F040. These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 and A6 are at low. The manufacturer code is output when the Address Input A0 is Low and the device code when this Input is High. Other Address Inputs are ignored. The codes are output on DQ0 DQ7. This is shown in Table 4.

The Electronic Signature can also be read, without raising A9 to V_{ID} by giving the memory the instruction RSIG (see below).

Sector Protection. Each sector can be separately protected against Program or Erase. Sector Protection provides additional data security, as it disables all program or erase operations. This

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-70		-90		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	70		90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 12B. Read AC Characteristics
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-120		-150		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

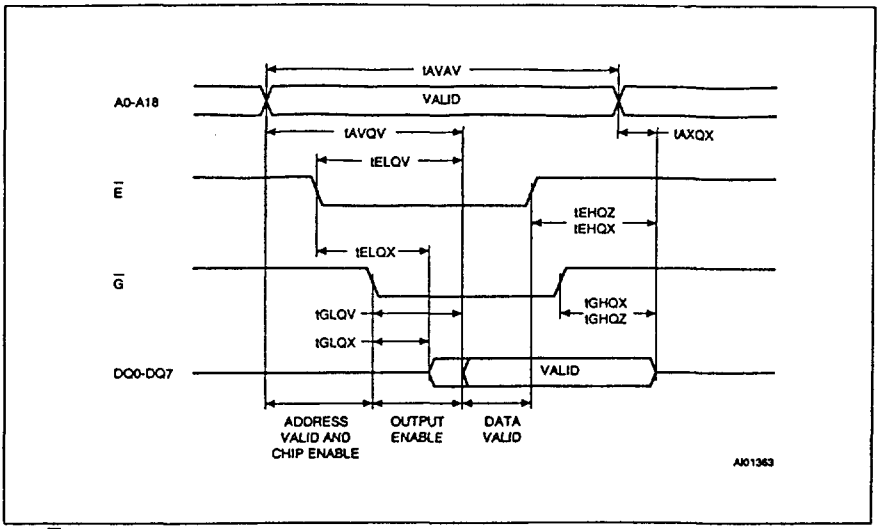
Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

DEVICE OPERATION (cont'd)

mode is activated when both A9 and $\overline{G}$ are set to V_{ID} and the sector address is applied on A16, A17 and A18. Sector protection is programmed using a Presto F program like algorithm. Protection is initiated by edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100us, the edge of $\overline{W}$ rising to V_{IH} will end the protection operation. Protection verify is achieved by bringing $\overline{G}$, $\overline{E}$ and A6 to V_{IL} while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the sector defined by the inputs on A16, A17 and A18 is protected. Any attempt to program or erase a protected sector will be ignored by the device.

Any protected sector can be unprotected to allow content updating. All sectors must be protected before an unprotect operation. Sector unprotect is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID}. The addresses inputs A6, A16, A12 must be maintained at V_{IH}. Sector unprotect is performed through a Presto F Erase like algorithm. Unprotect is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the edge of $\overline{W}$ rising to V_{IH} will end the unprotection operation. Unprotect verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A6 and $\overline{W}$ are at V_{IH} and A9 at V_{ID}. In these conditions, reading the output data will yield 00h if the sector defined by the inputs on A16, A17 and A18 is protected. All combinations of A16, A17 and A18 must be addressed in order to ensure that all of the 8 sectors have been unprotected. Sector Protection Status is shown in Table 5.

Figure 6. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Instructions and Commands

The Command Interface (C.I.) latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Electronic Signature, Sector Erase, Bulk Erase, Program, Sector Erase Suspend and Erase Resume. Commands are made of address and data sequences. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ and data is latched on the rising of $\overline{W}$ or $\overline{E}$. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the command. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Commands are initialised by two preceding coded cycles which unlock the Command Interface. In addition, for Erase, command confirmation is again preceeded by the two coded cycles.

P/E.C. status is indicated during command execution by Data Polling on DQ7, detection of Toggle on DQ6, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output those four bits. The P/E.C. automatically sets bits DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1, DQ2 and DQ4) are reserved for future use and should be masked.

Data Polling Bit DQ7. When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it will outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. It must be performed at the address being programmed or at an address within the sector being erased. If the sector to be erased is protected, if the byte to be programmed belongs to a protected sector or if all of the sectors are protected, DQ7 will set to data complement for about 100µs for erase, and then return to previous addressed memory data. The programming of a protection sector is ignored. See Figure 9 for the Data Polling flowchart and Figure 10 for the Data Polling waveforms.

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Table 13A. Write AC Characteristics, Write Enable Controlled
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		45		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	30		45		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		45		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQV} + t_{QVQV}$

Toggle Bit DQ6. When Programming operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$ or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit is valid only effective during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the sector to be erased is protected, if the byte to be programmed belongs to a protected sector or if all of the sectors are protected, DQ6 will toggle for about 2µs for programming and 100us for erase and then stop toggling and return back to Read. See Figure 11 for Toggle Bit flowchart and Figure 12 for Toggle Bit waveforms.

Error bit DQ5. This bit is set to '1' by the P/E.C when there is a failure of byte programming, sector erase, or bulk erase that results in invalid data being programmed in the memory sector. In case of error in sector erase or byte program, the sector in which the error occured or to which the programmed byte belongs, must be discarded. Other sectors may still be used. Error bit resets to '0' after Read/Reset (RD) instruction.

Erase Timer bit DQ3. This bit is set to '0' by the P/E.C. when the last Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the waiting period is finished, DQ3 returns back to '1'.

Coded Cycles. The two coded cycles unlock the Command Interface. They are followed by a com-

Table 13B. Write AC Characteristics, Write Enable Controlled
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQV1} + t_{QVQV}$

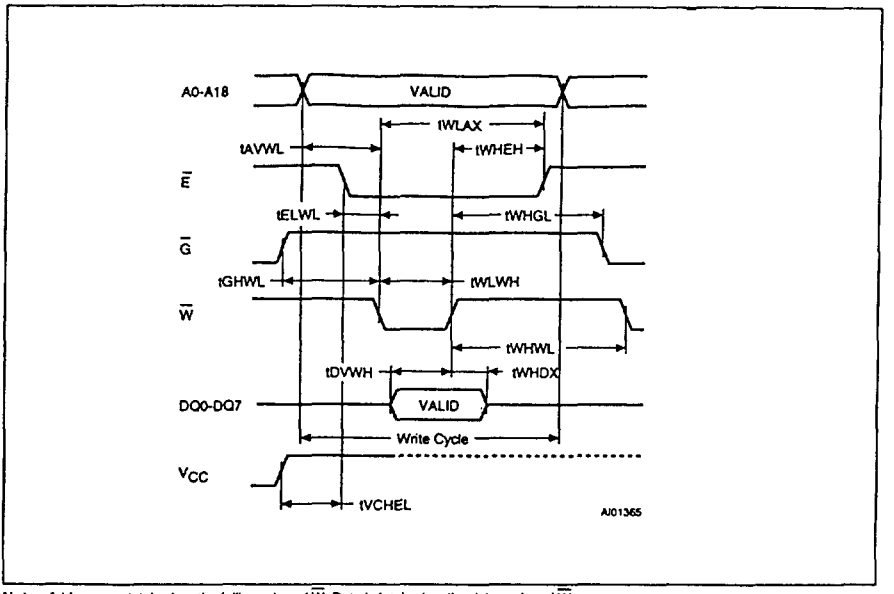
mand input or a comand confirmation. They consist in writing the data 0AAh at address 5555h during first cycle and data 55h at address 2AAAh during second cycle. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ while data is latched on the rising edge of $\overline{W}$ or $\overline{E}$. They happen on first and second cycles of the command write or on the fourth and fifth cycle.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0F0h at address 2555h. It can be optionally preceded by the two coded cycles. Subsequent read operations will read the memory array addressed and output the read byte.

Read Electronic Signature (RSIG) instruction. This instruction uses the two coded cycles followed by one write cycle giving the command 90h to address 5555h for command setup. Subsequent read will output the manufacturer code, the device code or the sector protection status depending on the levels of A0, A1, A6, A16, A17 and A18. The manufacturer code, 20h, is output when the addresses lines A0, A1 and A6 are Low, the device code, 0E2h is output when A0 is High with A1 and A6 Low.

Read Sector Protection. The use of Read Electronic Signature (RSIG) command also allows access to the sector protection status verify. After

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

DEVICE OPERATION (cont'd)

giving the RSIG command, A0 and A6 are set to V_{IL} with A1 at V_{IH}, while A16, A17 and A18 define the sector of the sector to be verified. A read in these conditions will output a 01h if sector is protected and a 00h if sector is not protected.

Bulk Erase (BE) Instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written on third cycle to address 5555h after the two coded cycles. The Bulk Erase Confirm command 10h is written at address 5555h on sixth cycle after another two coded cycles. If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle Bit DQ6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because the erasure has not been verified even after the maximum number of erase cycles have been executed.

Sector Erase (SE) instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written on third cycle to address 5555h after the two coded cycles. The Sector Erase Confirm command 30h is written on sixth cycle after another two coded cycles. During

Table 14A. Write AC Characteristics, Chip Enable Controlled
(T_C = −55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		45		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	30		45		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		45		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQV1} + t_{QVQV}$

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the input of the second command an address within the sector to be erased is given and latched into the memory. Additional Sector Erase confirm commands and sector addresses can be written subsequently to erase other sectors in parallel without further coded cycles. The erase will start after an Erase timeout period of about 100us. Thus, additional Sector Erase commands must be given within this delay. The input of a new Sector Erase command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Sector Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C is erasing the sector(s). If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the sector with 00h as the P/E.C. will do this automatically before to erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register status bits.

During the execution of the erase by the P/E.C., the memory accepts only the ES (Erase Suspend) instruction. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle Bit DQ6 toggles during erase operation. It stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed.

Table 14B. Write AC Characteristics, Chip Enable Controlled
(T_C= –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, t_{WHQV} = t_{WHQV} + t_{QVQV}

Program (PG) instruction. This instruction uses four write cycles. The Program command A0h is written on third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on its rising edge and starts the P/E.C. Read operations output the status bits after the programming has started. Memory programming is made only by writing '0' in place of '1' in a Byte.

Erase Suspend (ES) instruction. The Sector Erase operation may be suspended by this instruction which consists of writing the command 0B0h without any specific address code. No coded cycles are required. It allows reading of data from another sector while erase is in progress. Erase suspend is accepted only during the Sector Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle Bit DQ6 stops toggling when the P/E.C. is suspended. Toggle Bit status must be monitored at an address out of the sector being erased. During the suspension the memory will respond only to Read (RD), or Erase Resume (ER) instructions. Read operations initially output the status bits while erase is suspended but, following a Read instruction, data from other sectors of the memory can be read.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any coded cycle.

Table 15A. Data Polling and Toggle Bit AC Characteristics(1)
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program W Control		10		10	µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Erase $\overline{W}$ Controller	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program E Controller		10		10	µs
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Erase $\overline{E}$ Controlled	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		30		35	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2}		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2}		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQV} is the Program or Erase time.

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Programing. The memory can be programmed byte-by-byte. The program sequence is started by two coded cycles, followed by writing the Program command (0A0h) to the Command Interface, this is followed by writing the address and data byte to the memory. The Program/Erase Controller automatically starts and performs the programming after the fourth write operation. During programming the memory status is checked by reading the status bits DQ3, DQ5, DQ6 and DQ7 which shows the status of the P/E.C. DQ6 and DQ7 determine if programming is on going or has completed and DQ5 allows a check to be made for any possible error.

Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ should be tied to V_{IH} to allow maximum security. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

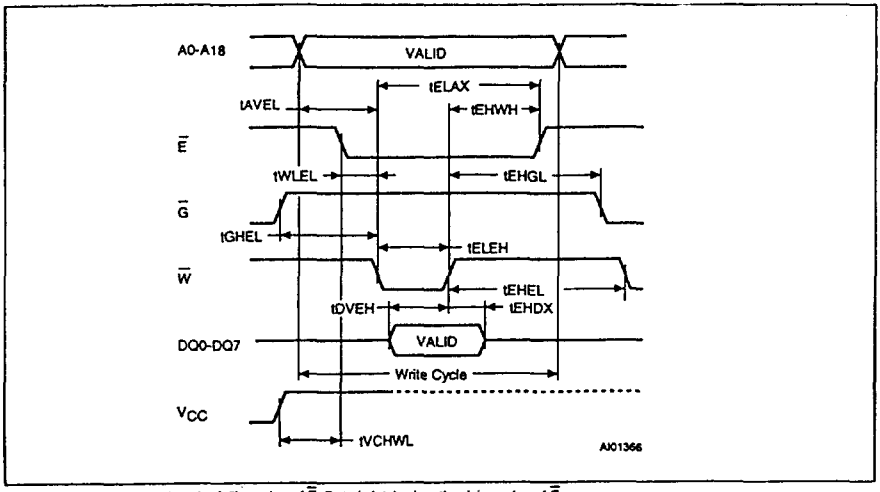
Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Table 15B. Data Polling and Toggle Bit AC Characteristics[1]
(T_C= –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} [2]		Write Enable High to DQ7 Valid (Program W Control		10		10	µs
t_{WHQ7V2} [2]		Write Enable High to DQ7 Valid (Erase $\overline{W}$ Controller	1.5	30	1.5	30	sec
t_{EHQ7V1} [2]		Chip Enable High to DQ7 Valid (Program E Controller		10		10	µs
t_{EHQ7V2} [2]		Chip Enable High to DQ7 Valid (Erase $\overline{E}$ Controlled	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		50		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2}		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2}		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

Figure 9. Data Polling Flow-chart

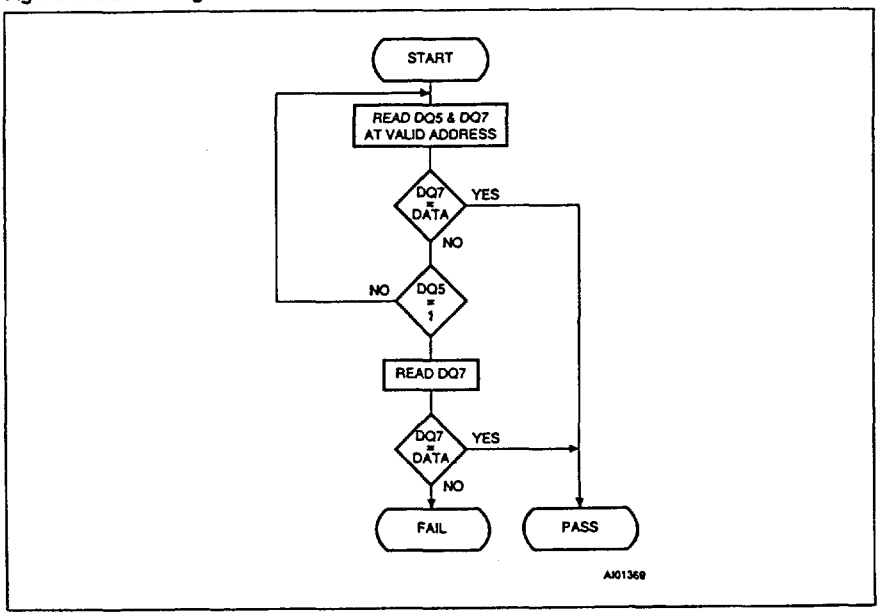
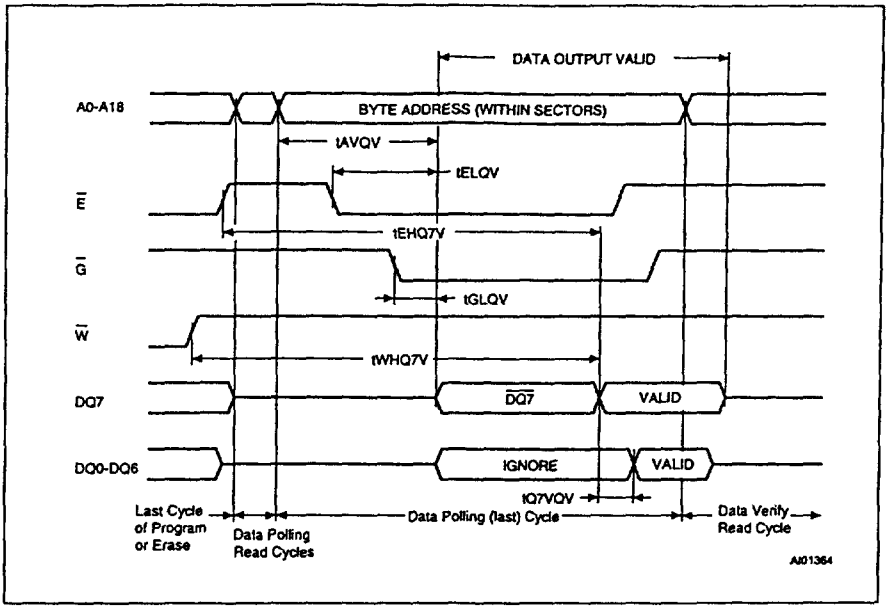


Figure 10. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Sector being erased.

Figure 11. Data Toggle Flow-chart

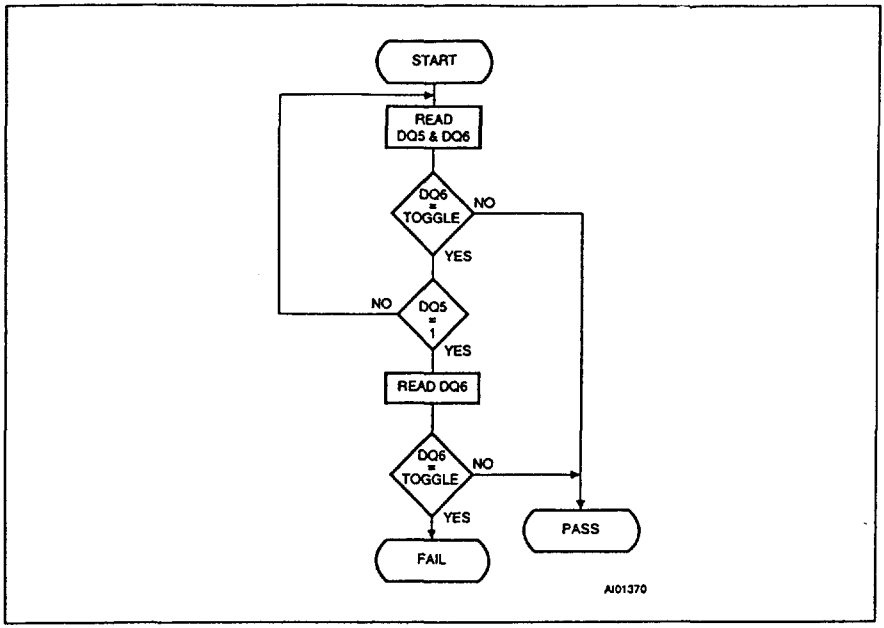
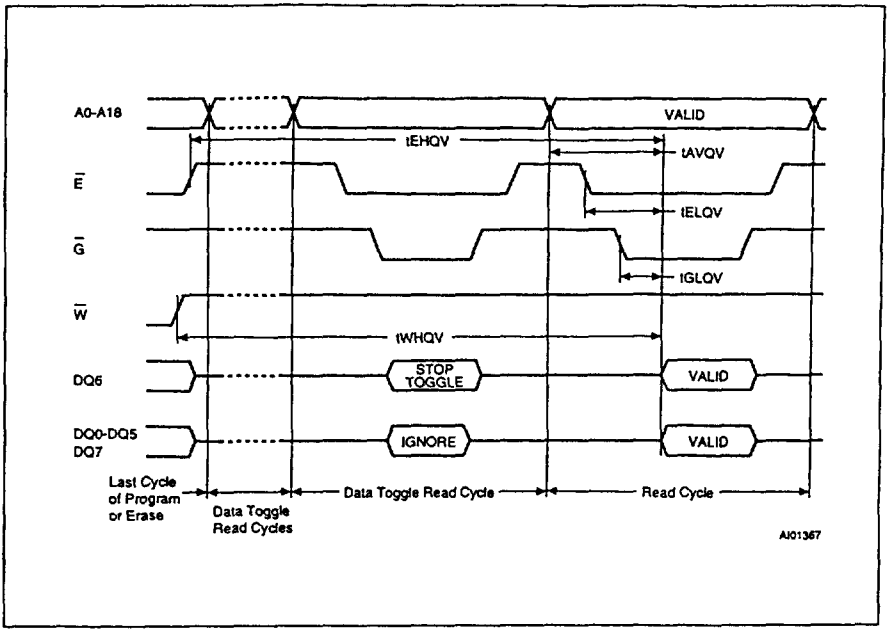


Figure 12. Data Toggle DQ6 AC Waveforms



Note: All other timings are as a normal Read cycle.

Table 16. Program, Erase Times and Program, Erase Endurance Cycles
(T_C= –55 to +125°C)

Parameter	M29F040			Unit
	Min	Typ	Max	
Chip Program (Byte)		8.5		sec
Bulk or Sector Erase		1.5	30	sec
Byte Program		10		µs
Program/Erase Cycles	100,000			cycles

Figure 13. Sector Protection Flow-chart

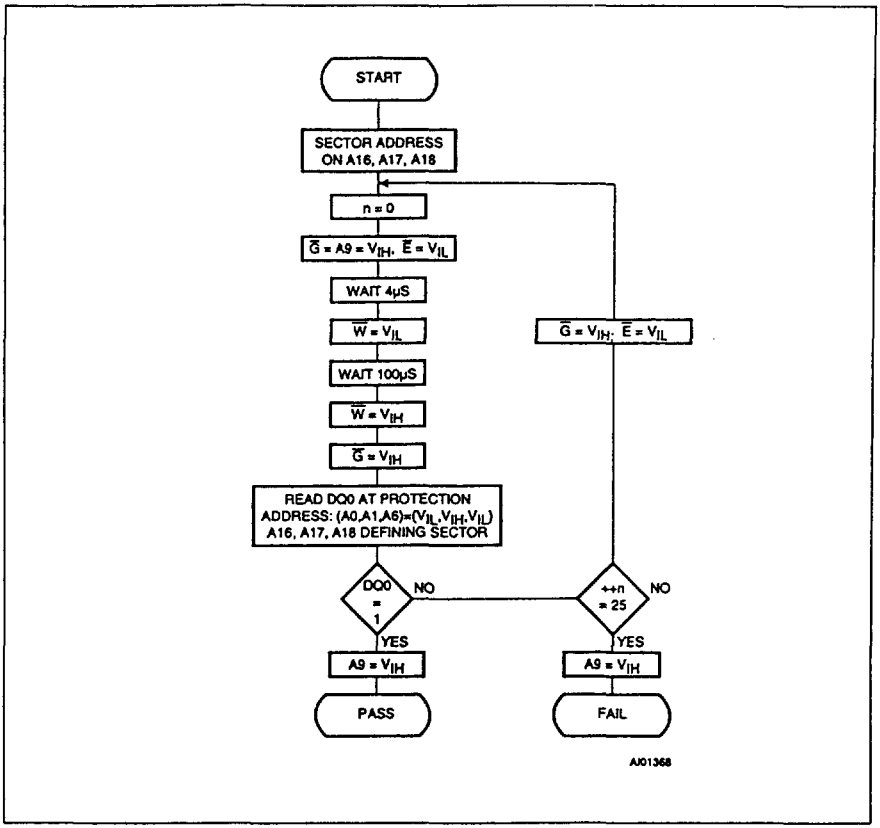


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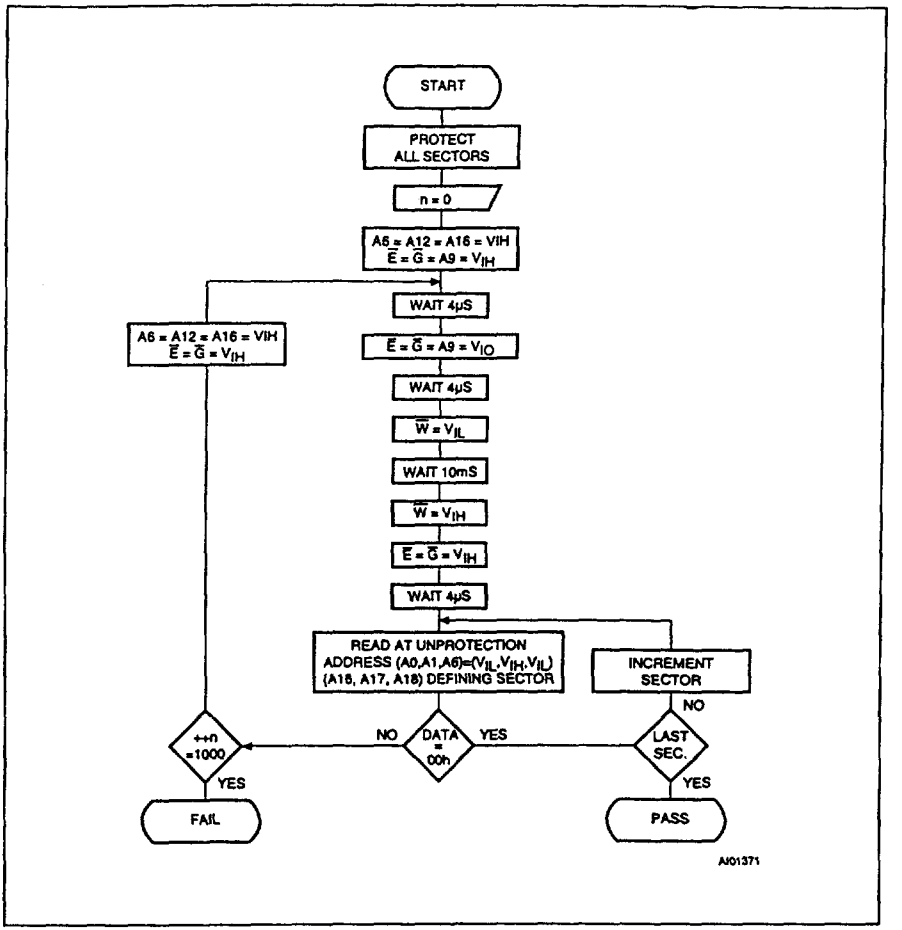
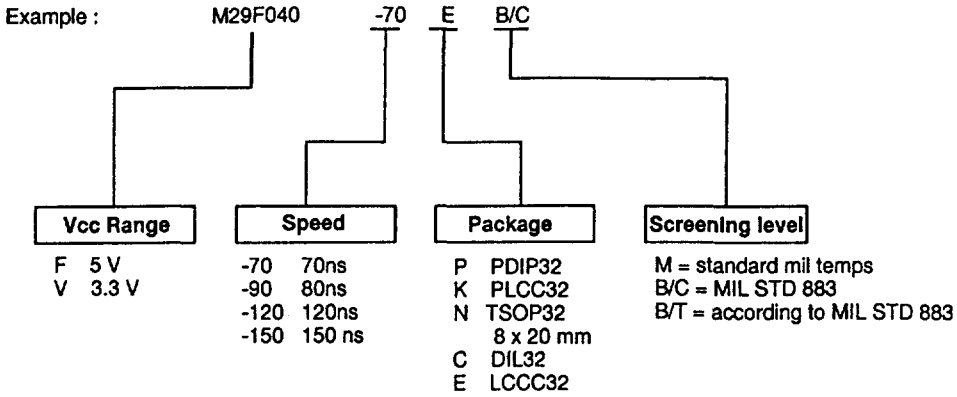
Figure 14. Sector Unprotecting Flow-chart



ORDERING INFORMATION SCHEME



Full data on the 3V product, M29V040, will be added to this document in the near future.

For further information on any aspect of this device, please contact THOMSON-CSF SEMICONDUCTORS SPECIFIQUES Sales Office nearest to you.

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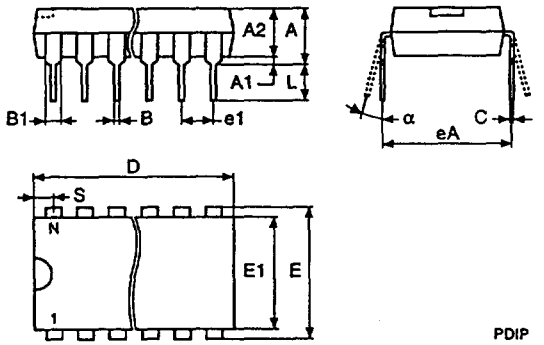
PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



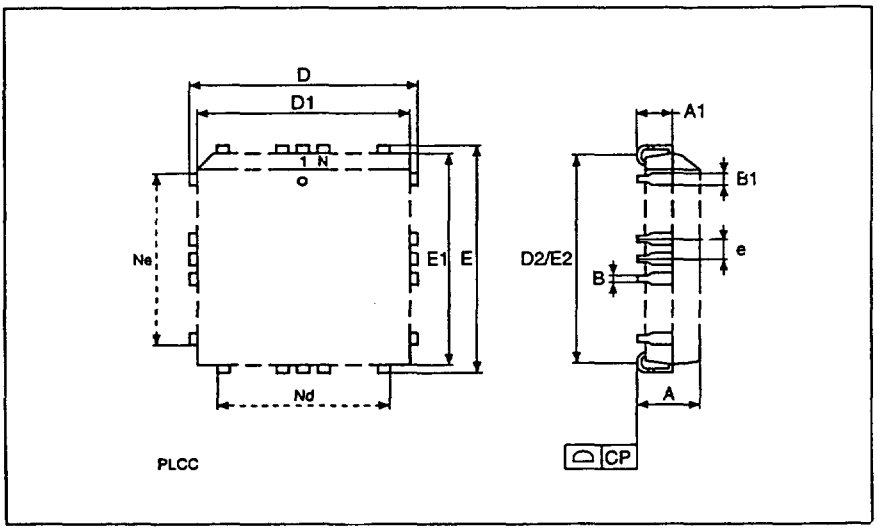
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32

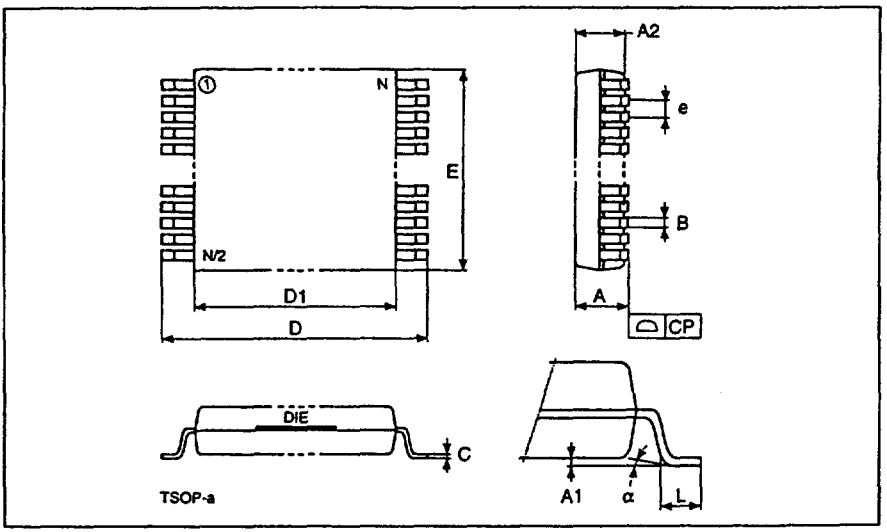


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20 mm

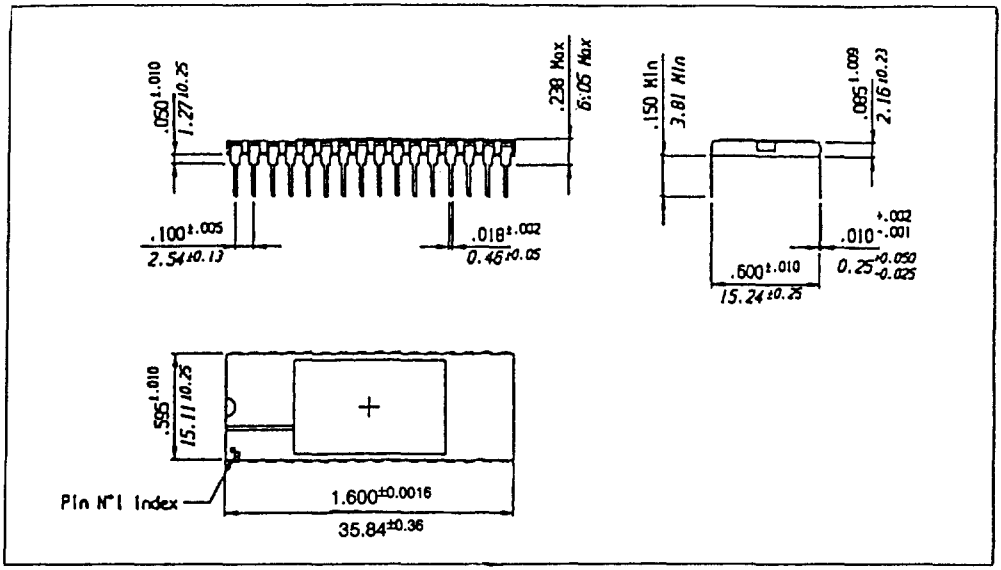
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0 °C	5 °C		0 °C	5 °C
N		32			32	
CP			0.10			0.004

TSOP32



Drawing is out of scale

DIL 32 - 32 pin Ceramic DIL, 600 mils width



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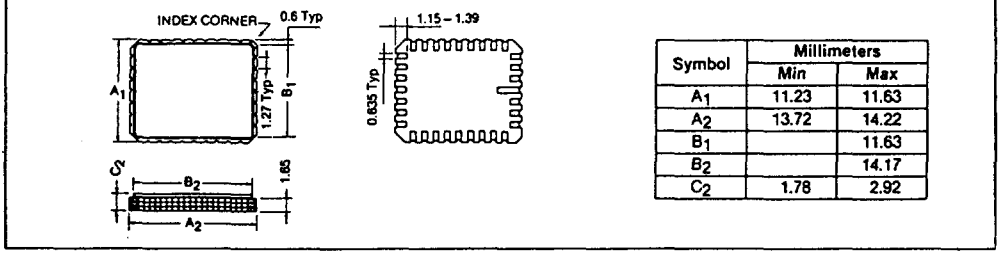
LCCC 32 - lead Leaded Ceramic Chip Carrier, rectangular



Symbol	Millimeters	
	Min	Max
A_1	11.23	11.63
A_2	13.72	14.22
B_1		11.63
B_2		14.17
C_2	1.78	2.92