2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Single 5 volt supply**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- **User selectable memory organization**
  - **— 256 x 16 or 512 x 8 for KM93C67**
  - **— 128 x 16 or 256 x 8 for KM93C57**
- **System Clock Frequency: 1 MHz (max.)**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle**
  - **— Data retention: 10 years**

GENERAL DESCRIPTION

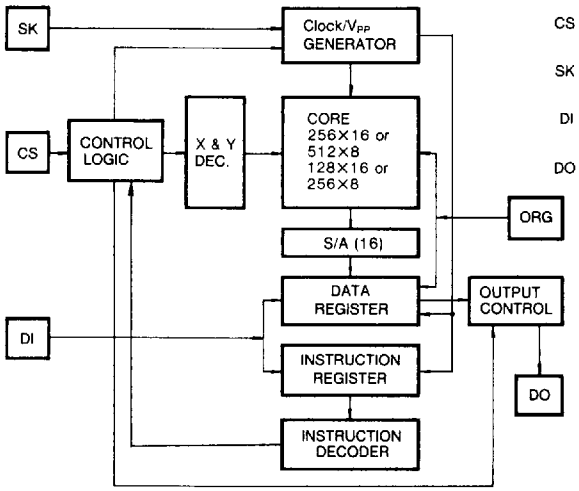
The KM93C57/67 is a 5V only 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

The KM93C57/67 can be organized as 128/256 registers of 16 bits each or as 256/512 registers by 8 bits each, which can be read/written serially by a microprocessor.

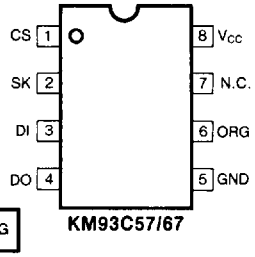
The KM93C57/67 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

2

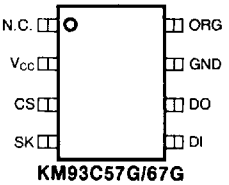
FUNCTIONAL BLOCK DIAGRAM



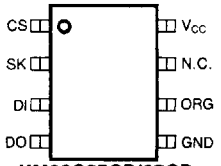
PIN CONFIGURATION



KM93C57/67



KM93C57G/67G
(SC57/67)



KM93C57GD/67GD
(C57D/67D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
ORG*	Memory Organization
V_{CC}	Power Supply

*Note: When the ORG pin is connected to V_{CC}, X16 organization is selected. And when it is connected to ground, X8 organization is selected. If it is unconnected, then an internal pull-up device will select the X16 organization.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		4.5	5.5	V
Operating Current	DC	I_{CC1}	CS = V_{IH}, SK = V_{IH}	—	1	mA
	AC	I_{CC2}	CS = V_{IH}, SK = 1.0MHz	—	3	mA
Standby Current	TTL	I_{SB1}	V_{CC} = 5.5V, CS = V_{IL}	—	250	μA
	CMOS	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}	—	100	μA
Input Low Voltage Levels		V_{IL}		-0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	Vcc+0.3	V
Output Voltage Levels		V_{OL}	I_{OL} = 2.1mA	—	0.4	V
		V_{OH}	I_{OH} = −400μA	2.4	—	V
Input Leakage Current		I_{IL}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{OL}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

A.C. TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.45V to 2.4V
Input Rise and Fail Time	20ns
Output Load	1 TTL Gate and C_L=100pF

AC OPERATING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{0H}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.

Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

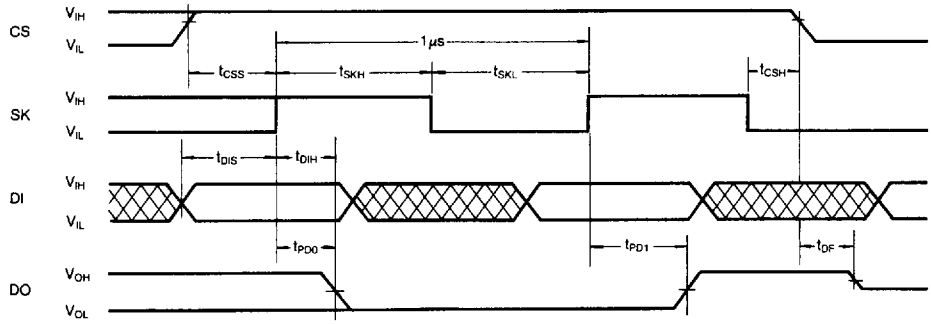
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address		Data		Comment
			256 x 16 *(128 x 16)	512 x 8 (256 x 8)	256 x 16	512 x 8	
READ	1	10	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{OUT} (16 bit)	D_{OUT} (8 bit)	Read register at specified address
WRITE	1	01	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{15}~D_0	D_8~D_0	Write the data at specified address
ERASE	1	11	A7~A0 (A6~A0)	A8~A0 (A7~A0)	—	—	Erase the data at specified address
EWEN	1	00	11XXXXXX (11XXXXX)	11XXXXXXX (11XXXXXX)	—	—	Erase/Write enable
EWDS	1	00	00XXXXXX (00XXXXX)	00XXXXXXX (00XXXXXX)	—	—	Erase/Write disable
WRAL	1	00	01XXXXXX (01XXXXX)	10XXXXXXX (01XXXXXX)	D_{15}-D_0	D_8~D_0	Write all registers
ERAL	1	00	10XXXXXX (10XXXXX)	01XXXXXXX (10XXXXXX)	—	—	Erase all registers

Note: '( )' is appliable to KM93C57

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

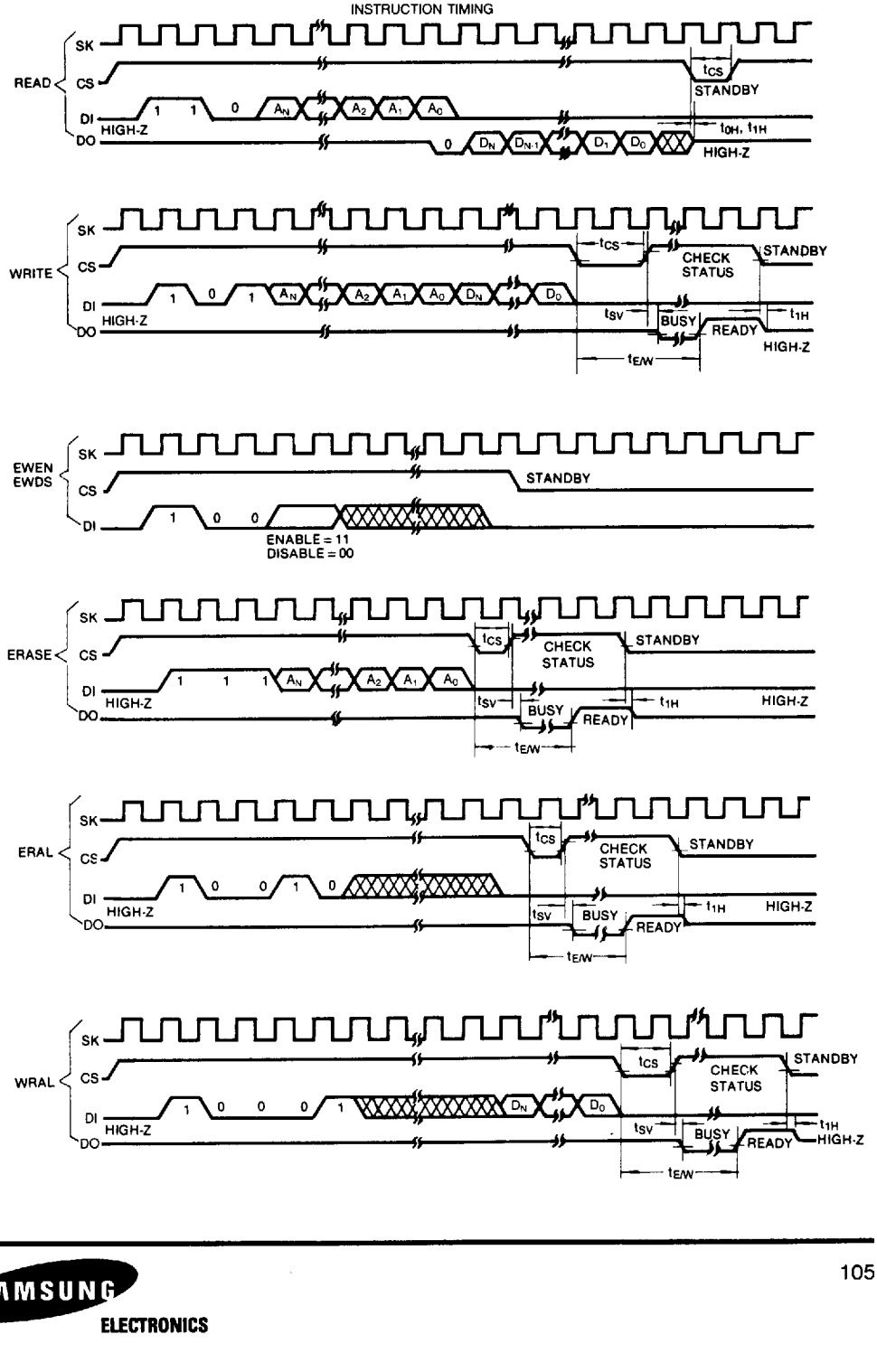


ORGANIZATION

P/N	Organization	AN	DN
KM93C67	512× 8	A_8	D_7
	256×16	A_7	D_{15}
KM93C57	256× 8	A_7	D_7
	128×16	A_6	D_{15}

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



SAMSUNG ELECTRONICS

INTRODUCTION

The KM93C57/67 is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a single 5.0V power supply. The write cycle of the KM93C57/67 is self timed with the ready/$\overline{busy}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C57/67 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto-chip-erase. All cells are written simultaneously with given data.

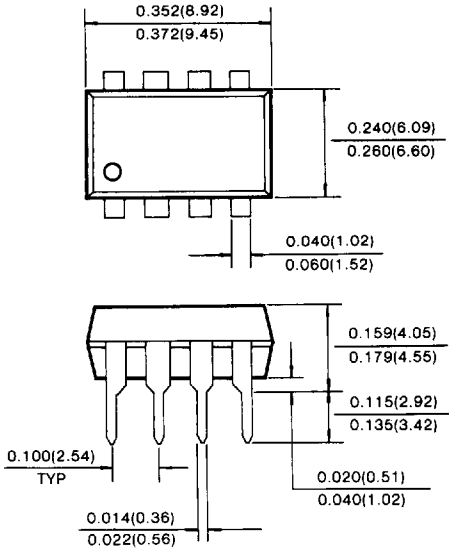
ERAL

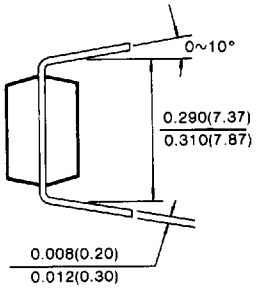
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

PACKAGE DIMENSIONS

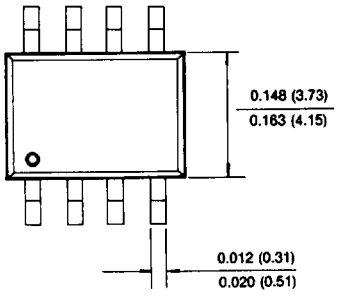
8 PIN PLASTIC DUAL IN LINE PACKAGE

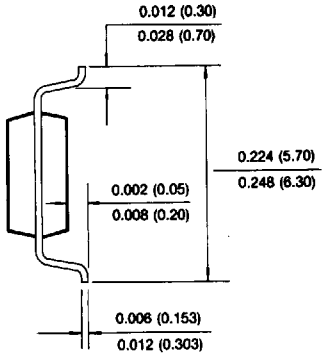
unit; inches (millimeters)

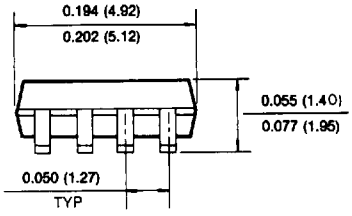




8 PIN PLASTIC SMALL OUT LINE PACKAGE







PRELIMINARY

KM93C57V/KM93C67V

CMOS EEPROM

2K/4K Bit Serial Electrically Erasable PROM

FEATURES

- **Enhanced extended operating voltage: 3.0V~5.5V**
- **Low power consumption**
  - **— Active: 3 mA (TTL)**
  - **— Standby: 250μA (TTL)**
- **User selectable memory organization**
  - **— 256 x 16 or 512 x 8 for KM93C67 V**
  - **— 128 x 16 or 256 x 8 for KM93C57 V**
- **System Clock Frequency: 1 MHz (max.)**
  - **— Automatic erase before write**
  - **— R/$\overline{B}$ status signal during programming**
- **Reliable CMOS floating-gate technology**
  - **— Endurance : 100,000 cycle**
  - **— Data retention: 10 years**

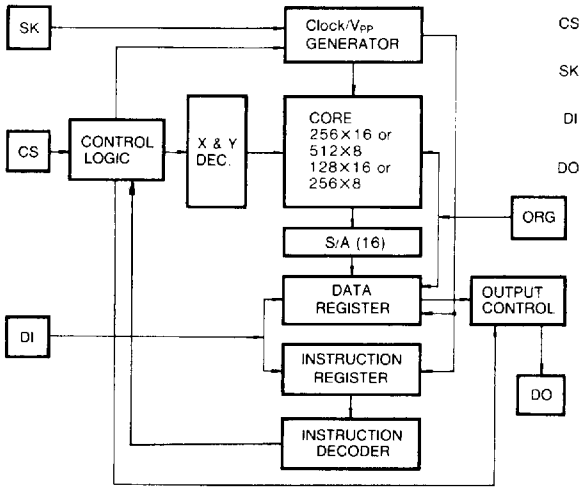
GENERAL DESCRIPTION

The KM93C57V/67V is a extended voltage 2K/4K bits serial I/O EEPROM and is fabricated with the well defined floating gate CMOS technology using Flower Nordheim tunneling for erasing and programming.

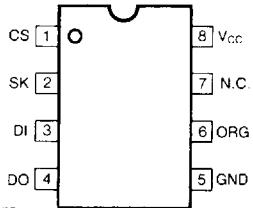
The KM93C57V/67V can be organized as 128/256 registers of 16 bits each or as 256/512 registers by 8 bits each, which can be read/written serially by a microprocessor.

The KM93C57V/67V is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

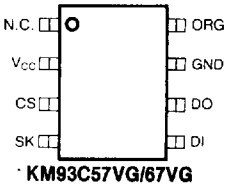
FUNCTIONAL BLOCK DIAGRAM



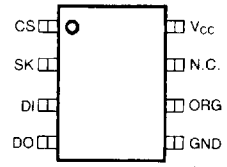
PIN CONFIGURATION



KM93C57V/67V



KM93C57VG/67VG
(C57V/67V)



KM93C57VGD/67VGD
(57VD/67VD)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
N.C.	No Connection
ORG*	Memory Organization
V_{CC}	Power Supply

*Note: When the ORG pin is connected to V_{CC}, X16 organization is selected. And when it is connected to ground, X8 organization is selected. If it is unconnected, then an internal pull-up device will select the X16 organization.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0°C to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	—	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC OPERATING CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Parameter		Symbol	Test Condition	Min	Max	Unit
Operating Voltage		V_{CC}		3.0	5.5	V
Operating Current	(DC)	I_{CC1}	CS = SK = V_{IH}		1	mA
	(AC)	I_{CC2}	CS = V_{IH}, SK = 1MHz		3	mA
Standby Current	(TTL)	I_{SB1}	V_{CC} = 5.5, CS = V_{IL}		250	μA
	(CMOS)	I_{SB2}	V_{CC} = 5.5V, CS = V_{SS}		100	μA
Input Low Voltage Levels		V_{IL}		−0.3	0.8	V
Input High Voltage Levels		V_{IH}		2.0	V_{CC} + 0.3	V
Output Voltage Levels ($4.5 < V_{CC} < 5.5$)		V_{OL1}	I_{OL} = 2.1mA		0.4	V
		V_{OH1}	I_{OH} = −400μA	2.4		V
Output Voltage Levels ($3.0 < V_{CC} < 4.5$)		V_{OL2}	I_{OL} = 10μA		0.2	V
		V_{OH2}	I_{OH} = −10μA	2.0		V
Input Leakage Current		I_{LI}	V_{IN} = 5.5V	-2.5	2.5	μA
Output Leakage Current		I_{LO}	V_{OUT} = 5.5V, CS = 0V	-2.5	2.5	μA

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.2V to 2.6V
Input Rise and Fall Times	20ns
Timing Measurement Reference Level	0.8V and 2.0V
Output Load	1 TTL GATE and CL = 100pF

AC OPERATING CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions	Limits		Unit
			Min.	Max.	
Maximum clock frequency	f_{CLK}	—	—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500	—	ns
SK Low Time	t_{SKL}	(Note 1)	250	—	ns
Minimum CS Low Time	t_{CS}	(Note 2)	250	—	ns
CS Setup Time	t_{CSS}	Relative to SK	50	—	ns
DI Setup Time	t_{DIS}	Relative to SK	50	—	ns
CS Hold Time	t_{CSH}	Relative to SK	0	—	ns
DI Hold Time	t_{DIH}	Relative to SK	100	—	ns
Output Delay to Data "1"	t_{PD1}	—	—	500	ns
Output Delay to Data "0"	t_{PD0}	—	—	500	ns
CS to Status Valid	t_{SV}	—	—	500	ns
CS to DO in High-Z	t_{DF}	—	—	100	ns
Write Cycle Time	$t_{E/W}$	—	—	10	ms
Falling Edge of CS to Dout High-Z	t_{OH}, t_{1H}	—	—	100	ns

Note 1: The SK spec. specifies a minimum SK clock period of 1 us, therefore in a SK clock cycle $t_{SKL}+t_{SKH}$ must be equal or greater than to 1 μs.
e.g., if t_{SKL}=250 ns then the minimum t_{SKH}=750 ns in order to meet the SK frequency specification.
Note 2: The CS must be brought low for a minimum 250 ns (t_{CS}) between consecutive instruction cycles.

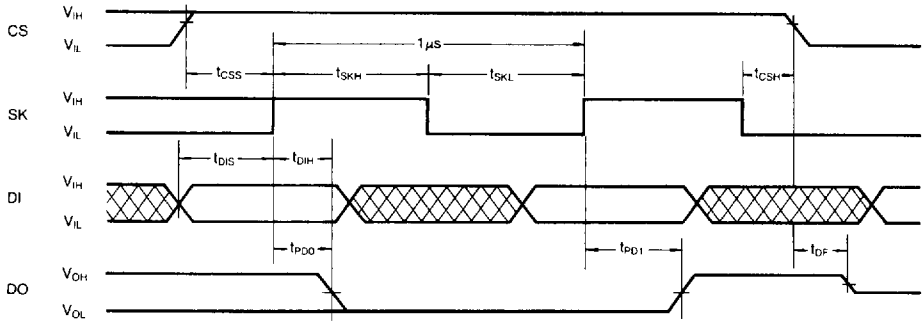
INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address		Data		Comment
			256 x 16 *(128 x 16)	512 x 8 (256 x 8)	256 x 16	512 x 8	
READ	1	10	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{OUT} (16 bit)	D_{OUT} (8 bit)	Read register at specified address
WRITE	1	01	A7~A0 (A6~A0)	A8~A0 (A7~A0)	D_{15}~D_0	D_8~D_0	Write the data at specified address
ERASE	1	11	A7~A0 (A6~A0)	A8~A0 (A7~A0)	—	—	Erase the data at specified address
EWEN	1	00	11XXXXXX (11XXXXX)	11XXXXXXX (11XXXXXX)	—	—	Erase/Write enable
EWDS	1	00	00XXXXXX (00XXXXX)	00XXXXXXX (00XXXXXX)	—	—	Erase/Write disable
WRAL	1	00	01XXXXXX (01XXXXX)	10XXXXXXX (01XXXXXX)	D_{15}-D_0	D_8~D_0	Write all registers
ERAL	1	00	10XXXXXX (10XXXXX)	01XXXXXXX (10XXXXXX)	—	—	Erase all registers

Note: '( )' is appliable to KM93C57V

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

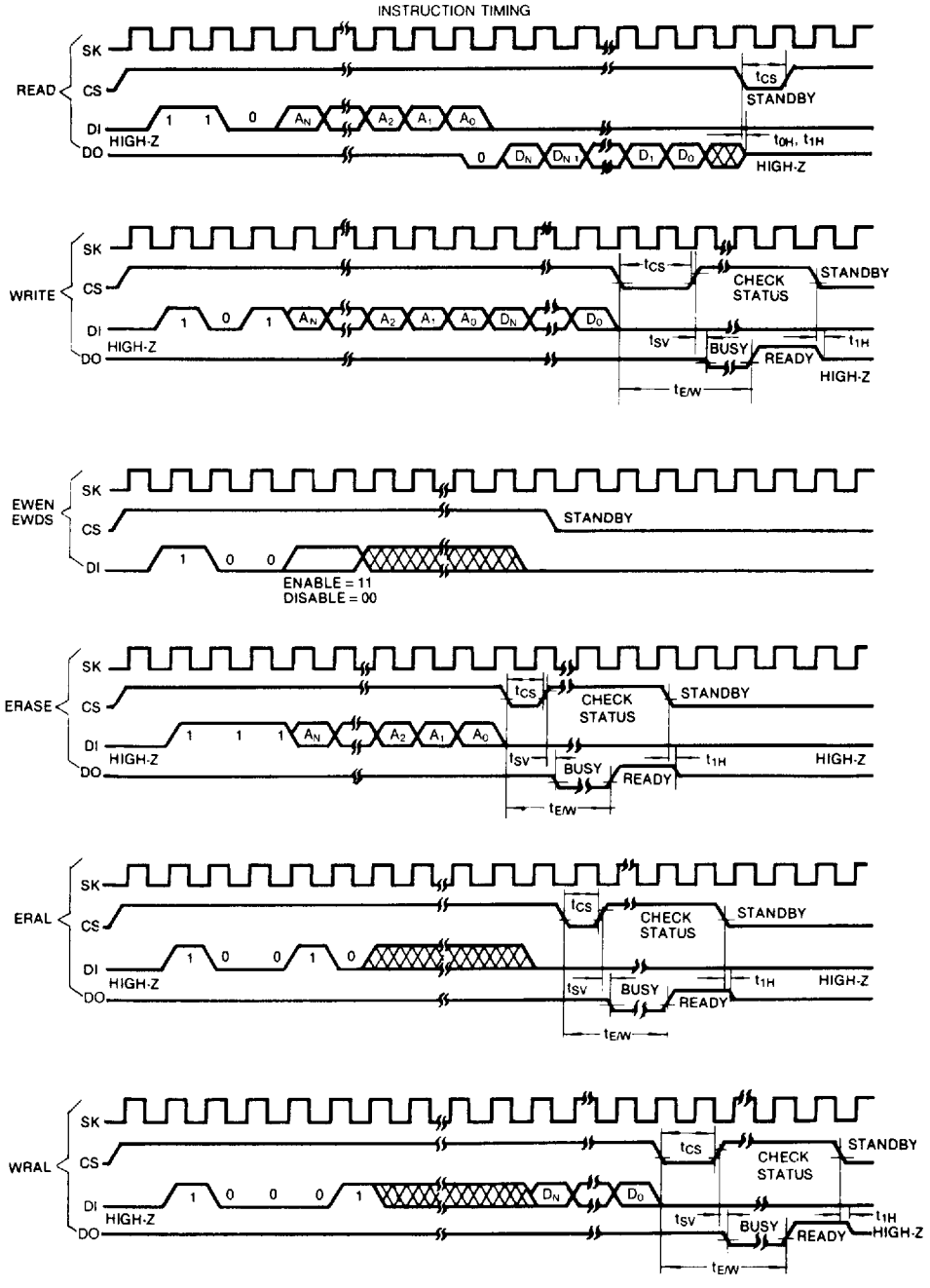


ORGANIZATION

P/N	Organization	AN	DN
KM93C67V	512× 8	A_8	D_7
	256×16	A_7	D_{15}
KM93C57V	256× 8	A_7	D_7
	128×16	A_6	D_{15}

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



INTRODUCTION

The KM93C57V/67V is a 2K/4K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on chip programming voltage generator allows user to use a3.0V to 5.5V single power supply. The write cycle of the KM93C57V/67V is self timed with the ready/$\overline{\text{busy}}$ status of chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is a high-Z except for the read period and the ready/$\overline{\text{busy}}$ indication period to eliminate bus contention.

It is possible to connect the DI and DO pins together as a common I/O to futher simplify the interface. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

DEVICE OPERATION

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN/EWDS

The KM93C57/67 is at the write disable (EWDS) state during the power-up period to protect against accidental disturbance. After the power-up period, the write operation must be preceded by an write enable (EWEN) operation. The write enable (EWEN) mode is maintained until a EWDS operation is executed or V_{CC} is removed from the part. Execution of the read operation is independent of both EWEN and EWDS instructions.

WRITE

The write operation is started by sequentially loading its instruction, address and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto erase. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during write cycle.

ERASE

The erase operation is started by sequentially loading its instruction, address. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed erase cycle. The chip's ready/$\overline{\text{busy}}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRAL

The WRAL instruction is started by sequentially loading its instruction and data set. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle with auto-chip-erase. All cells are written simultaneously with given data.

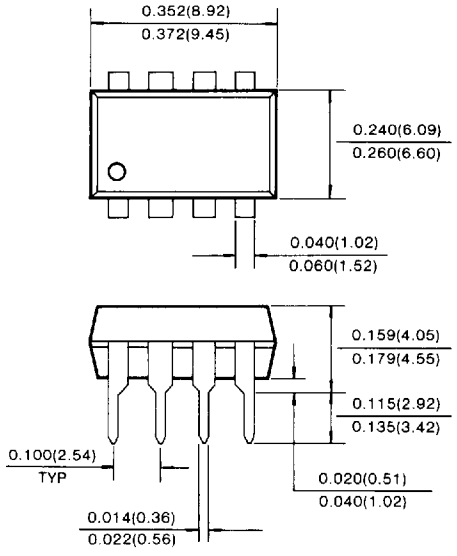
ERAL

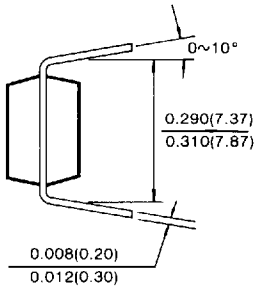
The ERAL instruction is started by sequentially loading its instruction. After the last bit of data is input on the DO pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. All cells are erased simultaneously.

PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)





8 PIN PLASTIC SMALL OUT LINE PACKAGE