



SANYO Semiconductors DATA SHEET

LA6220AM — Monolithic Linear IC Rail-to-Rail Dual Operational Amplifier for Automotive Applications

Overview

The LA6220AM dual operational amplifier is optimal for both consumer and industrial applications, including all types of transducer amplifier and DC amplifier circuit. It supports from ground to V_{CC} (rail to rail) as the voltage range for both inputs and outputs and is a high-performance dual operational amplifier that features the wide operating temperature range of -40 to $+125^{\circ}\text{C}$. It is optimal for the amplification of signals from all types of sensors.

Features

- Does not require phase compensation
- Supports from ground to V_{CC} (rail to rail) as the voltage range for both inputs and outputs
- Low current dissipation : $I_{CC} = 1.2\text{mA typ}/V_{CC} = +5\text{V}$, $R_L = \infty$

Specifications

Maximum Ratings at $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	$V_{CC \text{ max}}$		18	V
Differential Input Voltage	V_{ID}		± 1	V
Maximum Input Voltage	$V_{IN \text{ max}}$		-0.3 to +18	V
Operating Temperature	T_{opr}		-40 to +125	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

Recommended Operating Conditions at $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply Voltage	V_{CC}		2		17	V

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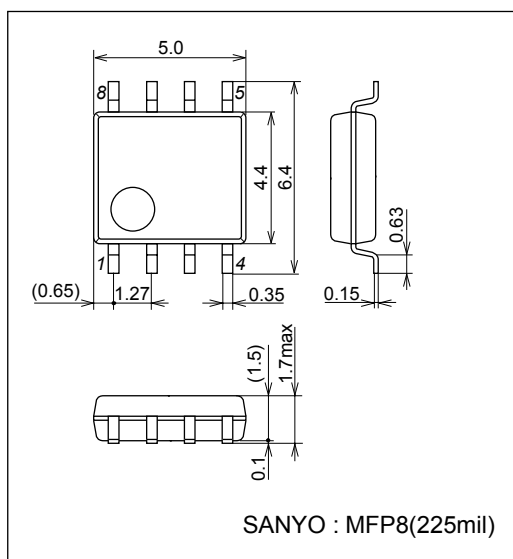
Electrical Characteristics at $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, (Otherwise unless specified.)

Parameter	Symbol	Conditions	Test Circuit	Ratings			unit
				min	typ	max	
Input Offset Voltage	V_{IO}		1		± 2	± 7	mV
Input Offset Current	I_{IO}	$I_{IN(+)} / I_{IN(-)}$	2		± 5	± 50	nA
Input Bias Current	I_B	$I_{IN(+)} / I_{IN(-)}$	3,4		45	250	nA
Common-Mode Input Voltage Range	V_{ICM}		5	0		V_{CC}	V
Common-Mode Rejection Ration	CMR		5		80		dB
Large Amplitude Voltage Gain	VG		6		100		V/mV
Output Voltage Range	V_{OH1A}	$R_L = 20\text{k}\Omega$; $T_a = 25^{\circ}\text{C}$	12	4.9			V
	V_{OH1B}	$R_L = 20\text{k}\Omega$; $T_a = -40$ to 125°C	12	4.85			V
	V_{OL1}	$R_L = 20\text{k}\Omega$	12			0.1	V
Output Voltage Range	V_{OH2}	$R_L = 2\text{k}\Omega$	12	4.75			V
	V_{OL2}	$R_L = 2\text{k}\Omega$	12			0.25	V
Supply Voltage Rejection Ratio	SVR		11		80		dB
Channel Separation		$f = 1\text{kHz}$ to 20kHz	7		80		dB
Current Drain	I_{CC}		8		1.2	2.5	mA
Output Current (Source)	$I_{O\text{ source}}$	$V_{IN+} = 1\text{V}$, $V_{IN-} = 0\text{V}$	9	6	10		mA
Output Current (Sink)	$I_{O\text{ sink}}$	$V_{IN+} = 0\text{V}$, $V_{IN-} = 1\text{V}$	10	3	5		mA
Slew Rate	SR	$R_L = 2\text{k}\Omega$			0.35		V/ μs
Gain-Bandwidth Product	F_t	$R_L = 2\text{k}\Omega$			1		MHz
Phase Margin	Φ_M	$R_L = 2\text{k}\Omega$			80		Deg

Package Dimensions

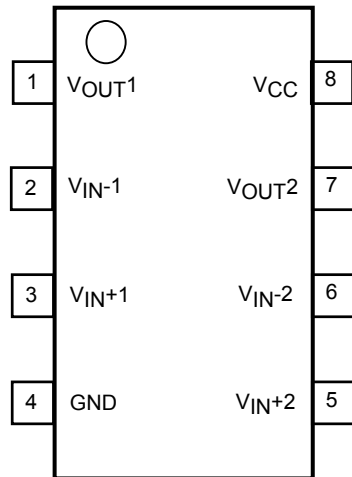
unit : mm

3032D



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Pin Assignment

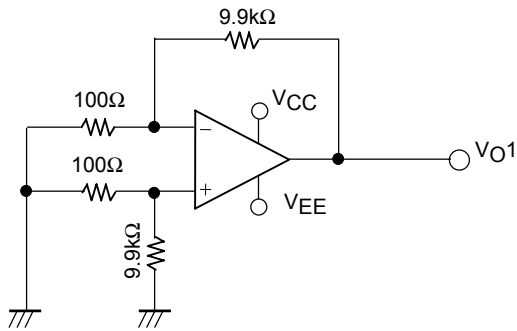


Pin Description

Pin Name	Pin Symbol	Pin No.	Equivalent Circuit Diagram	Pin Description
V_{IN}	V_{IN+1} V_{IN-1} V_{IN+2} V_{IN-2}	3 2 5 7		Inverting inputs Noninverting inputs
V_{OUT}	V_{OUT1} V_{OUT2}	1 7		Outputs

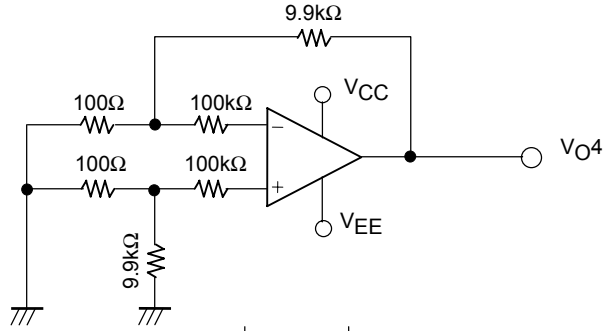
Test Circuits

1. Input offset voltage V_{IO}



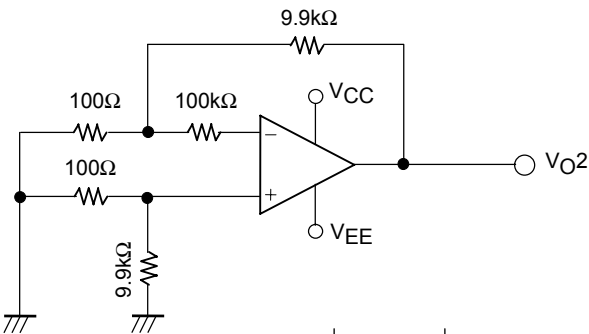
$V_{CC}/V_{EE} = \pm 2.5V$
 $V_{IO} = V_{O1}/100$

2. Input offset current I_{IO}



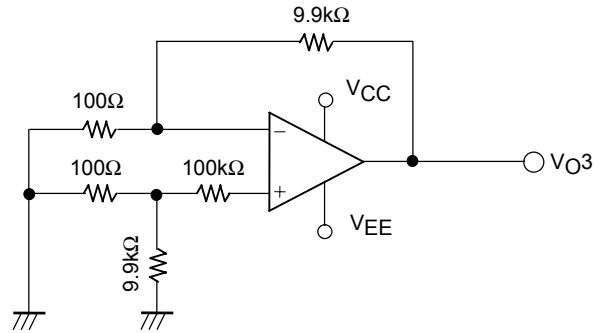
$$I_{IO} = \frac{|V_{O4} - V_{O1}|}{100k\Omega \times 100}$$

3. Input bias current $I_B (-)$



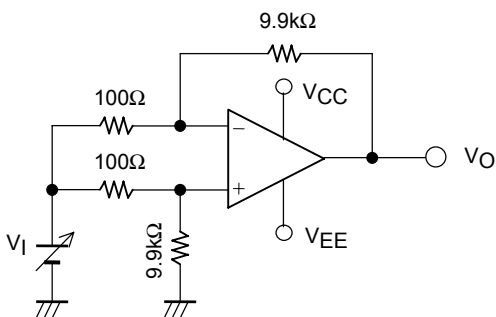
$$I_B(-) = \frac{|V_{O2} - V_{O1}|}{100k\Omega \times 100}$$

4. Input bias current $I_B (+)$



$$I_B(+) = \frac{|V_{O3} - V_{O1}|}{100k\Omega \times 100}$$

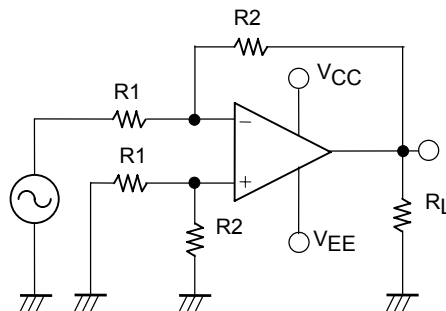
5. Common-mode rejection ratio (CMR)
 Common-mode input voltage range (VICM)



CMR $V_I = \pm 2.5V$

$$CMR = 20\log(5 \times 100 / |\Delta V_O|)$$

6. Voltage gain (VG)

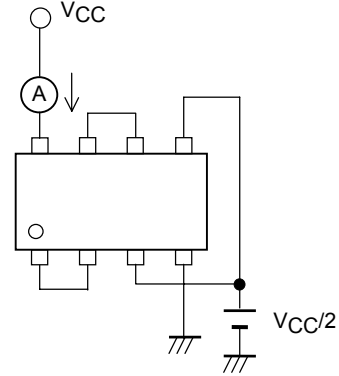
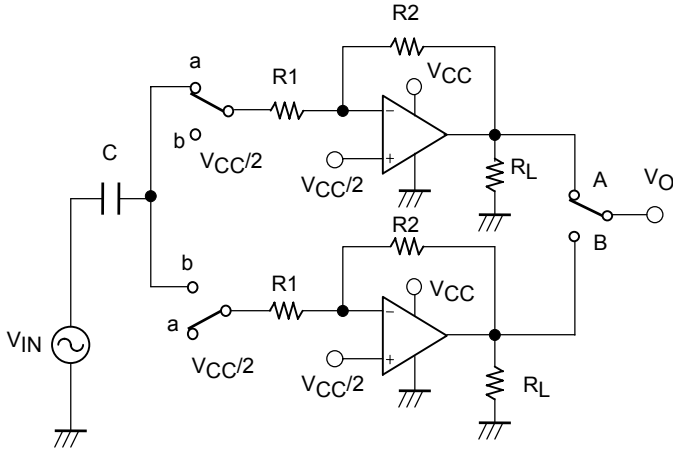


$$VG = \frac{R2}{R1}$$

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7. Channel separation (CS)

8. Current drain (ICC)



When the switch is in the "a" position.

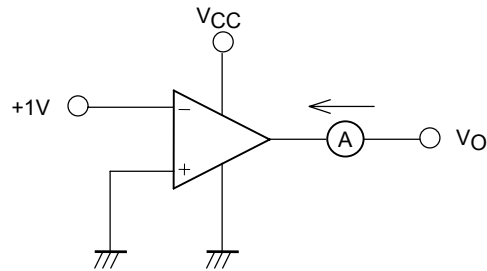
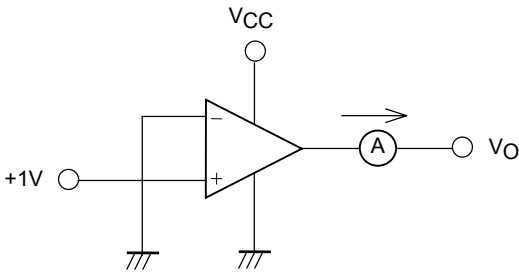
$$CS(A \rightarrow B) = 20 \log \frac{R2V_{oA}}{R1V_{oB}}$$

When the switch is in the "b" position.

$$CS(B \rightarrow A) = 20 \log \frac{R2V_{oB}}{R1V_{oA}}$$

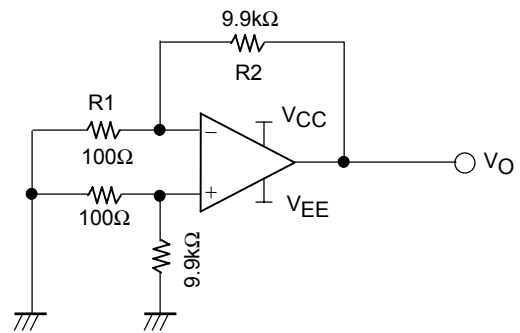
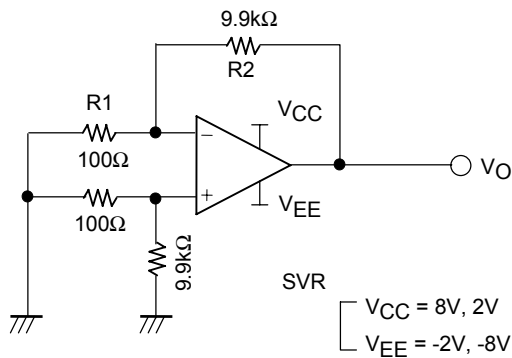
9. Output current (I_{Osource})

10. Output current (I_Osink)



11. Supply voltage rejection ratio SVR (+)

12. Supply voltage rejection ratio SVR (-)

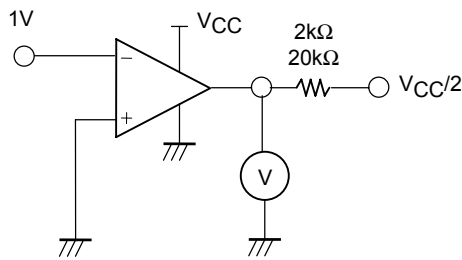


$$SVR(+) = 20 \log \left| \frac{\Delta V_{CC} \times 100}{\Delta V_O} \right|$$

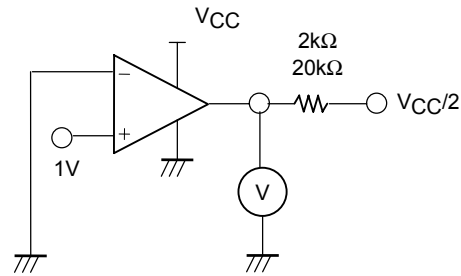
$$SVR(-) = 20 \log \left| \frac{\Delta V_{EE} \times 100}{\Delta V_O} \right|$$

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13. Output voltage range (Isink)



14. Output voltage range (Isource)



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