



3.3V CMOS 18-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

IDT74LVCR16501A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCR16501A:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

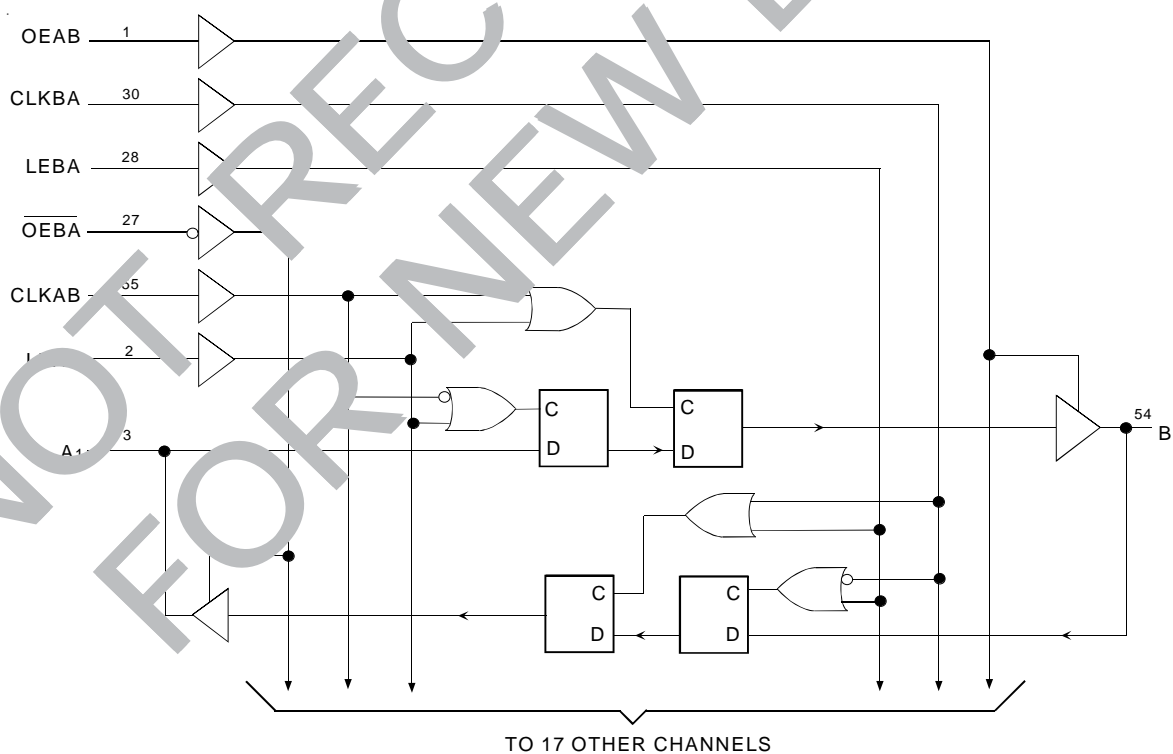
DESCRIPTION:

The LVCR16501A 18-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power, 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable ($OEAB$ and \overline{OEBA}), latch enable ($LEAB$ and $LEBA$) and clock ($CLKAB$ and $CLKBA$) inputs. For A-to-B data flow, the device operates in transparent mode when $LEAB$ is high. When $LEAB$ is low, the A data is latched if $CLKAB$ is held at a high or low logic level. If $LEAB$ is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of $CLKAB$. $OEAB$ performs the output enable function on the B port. Data flow from B port to A port is similar but requires using \overline{OEBA} , $LEBA$ and $CLKBA$. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

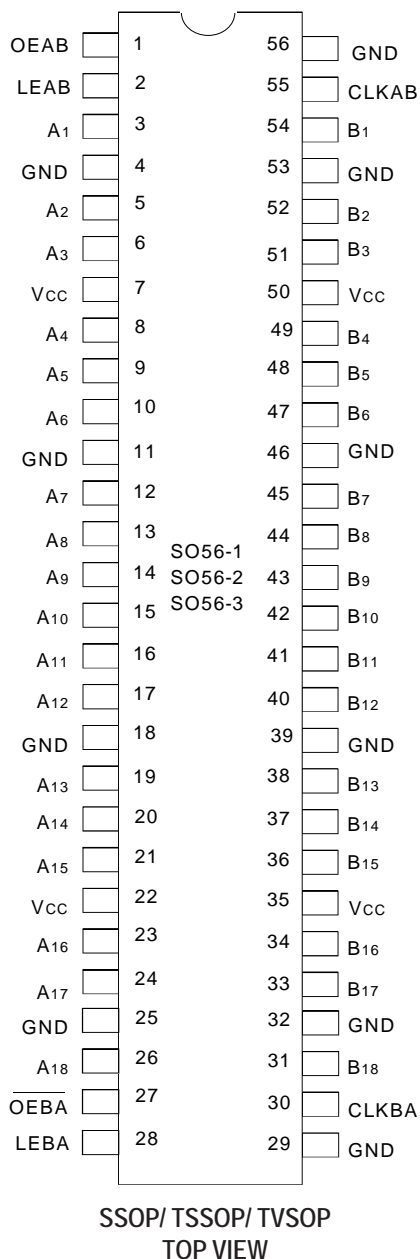
The LVCR16501A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive $\pm 12mA$ at the designated thresholds.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current	- 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (1, 2)

Inputs				Outputs	
OEAB	LEAB	CLKAB	Ax	Bx	
L	X	X	X	Z	
H	H	X	L	L	
H	H	X	H	H	
H	L	↑	L	L	
H	L	↑	H	H	
H	L	L	X	B ⁽³⁾	
H	L	H	X	B ⁽⁴⁾	

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition
- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	VCC = 3.6V	VI = 0 to 5.5V	—	—	±5	µA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = 0 to 5.5V	—	—	±10	µA
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5V		—	—	±50	µA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V	VIN = GND or VCC	—	—	10	µA
			3.6 ≤ VIN ≤ 5.5V ⁽²⁾	—	—	10	
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V other inputs at VCC or GND		—	—	500	µA

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NOTES:

1. Typical values are at VCC = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
			IOH = -4mA	1.9	—	
		VCC = 2.7V	IOH = -6mA	1.7	—	
			IOH = -4mA	2.2	—	
		VCC = 3.0V	IOH = -8mA	2	—	
			IOH = -6mA	2.4	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
			VCC = 2.3V	IOL = 4mA	—	
		VCC = 2.7V		IOL = 6mA	—	
			VCC = 3.0V	IOL = 4mA	—	
		VCC = 3.0V		IOL = 8mA	—	
			IOL = 6mA	—	0.55	
IOL = 12mA	—	0.8				

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	$C_L = 0pF, f = 10MHz$		pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled			pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit	
		Min.	Max.	Min.	Max.		
t _{PHL} t _{PLH}	Propagation Delay Ax to Bx or Bx to Ax	1.5	7	1.5	6	ns	
t _{PHL} t _{PLH}	Propagation Delay LEBA to Ax, LEAB to Bx	1.5	8	1.5	7	ns	
t _{PHL} t _{PLH}	Propagation Delay CLKBA to Ax, CLKAB to Bx	1.5	8	1.5	6.7	ns	
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx	1.5	8.2	1.5	7.2	ns	
t _{PHZ} t _{PLZ}	Output Disable Time OEBA to Ax, OEAB to Bx	1.5	8	1.5	7	ns	
t _{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	2.5	—	2.5	—	ns	
t _H	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	0	—	0	—	ns	
t _{SU}	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	2.5	—	2.5	—	ns
		Clock HIGH	2.5	—	2.5	—	ns
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—	ns	
t _w	LEAB or LEBA Pulse Width HIGH	3	—	3	—	ns	
t _w	CLKAB or CLKBA Pulse Width HIGH or LOW	3	—	3	—	ns	
t _{sk(0)}	Output Skew ⁽²⁾	—	—	—	500	ps	

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

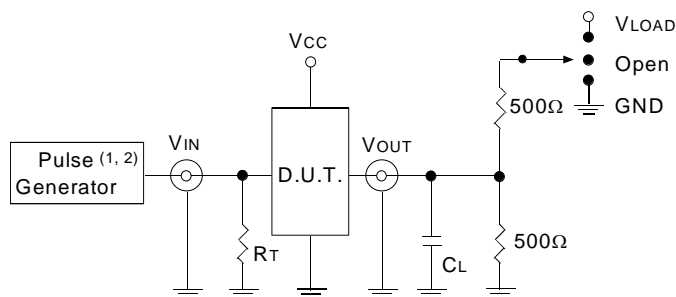
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ±0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

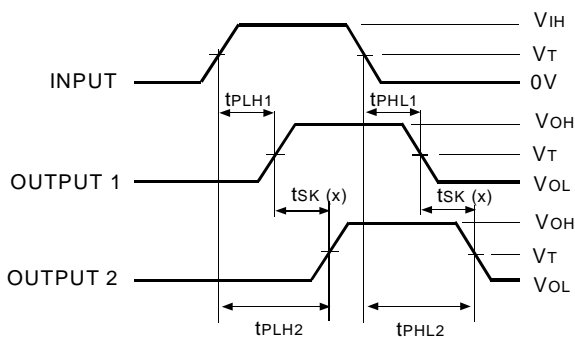
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK}(x)



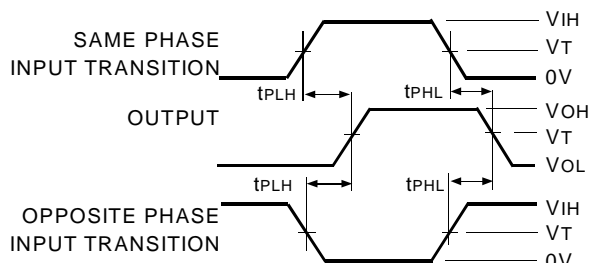
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

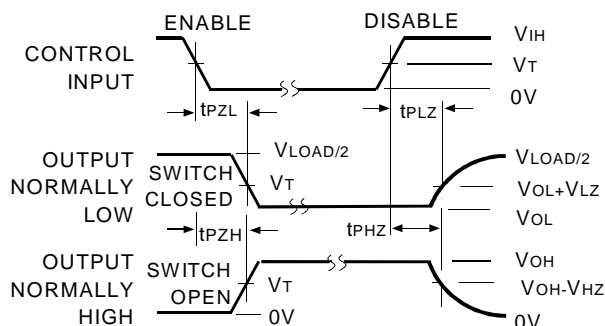
1. For t_{SK}(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

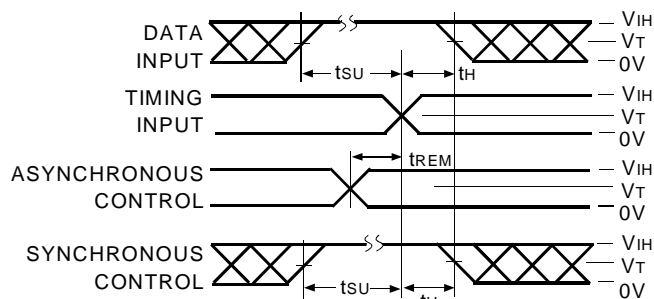


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NOTE:

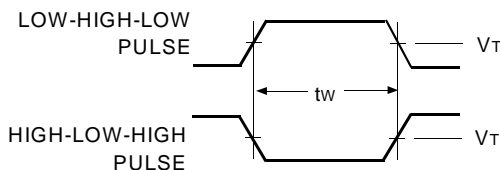
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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