

Document Title

256Kx36-Bit Pipelined NtRAM™

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	June. 09. 1998	Preliminary
0.1	1. Changed DC parameters Icc; from 450mA to 420mA at 150MHZ. ISB1; from 10mA to 20mA, ISB2 ; from 10mA to 20mA.	Aug. 19. 1998	Preliminary
0.2	1. Changed tCD from 4.0ns to 4.2ns at -75 2. Changed DC condition at Icc and parameters ISB1 ; from 20mA to 30mA, ISB2 ; from 20mA to 30mA.	Sep. 09. 1998	Preliminary
0.3	1. ADD 119BGA(7x17 Ball Grid Array Package) . 2. ADD x32 organization.	Oct. 15. 1998	Preliminary
0.4	Changed VOL Max value from 0.2V to 0.4V at 2.5V I/O.	Dec. 23 .1998	Preliminary
1.0	1. Final Spec Release. 2. Remove x32 organization.	Jan. 29. 1999	Final
2.0	1. Remove VDDQ Supply voltage(2.5V I/O)	Feb. 25. 1999	Final
3.0	1. Add VDDQ Supply voltage(2.5V I/O)	April. 23. 1999	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



256Kx36-Bit Pipelined NtRAM™

FEATURES

- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention only for TQFP.
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package).

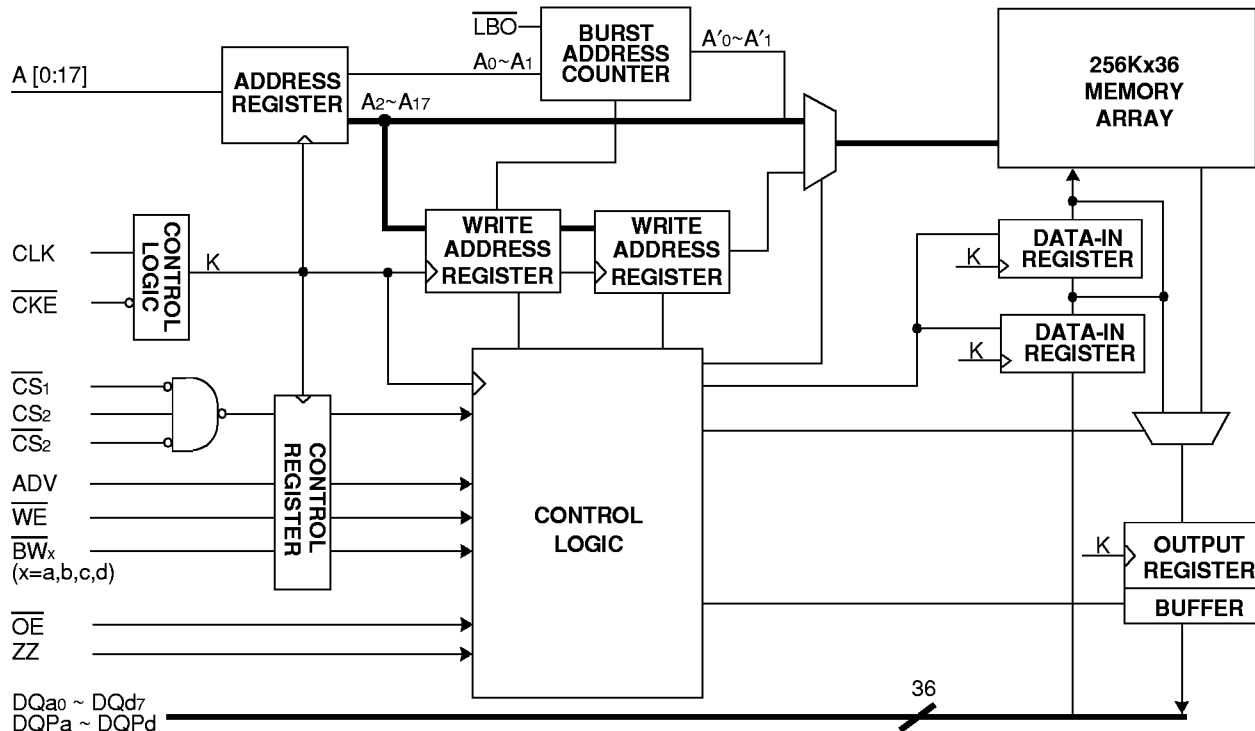
GENERAL DESCRIPTION

The KM736V849 is 9,437,184 bits Synchronous Static SRAMs. The NtRAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock. The KM736V849 is implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP and 119BGA packages. Multiple power and ground pins minimize ground bounce.

FAST ACCESS TIMES

PARAMETER	Symbol	-67	-75	-10	Unit
Cycle Time	t _{CYC}	6.7	7.5	10	ns
Clock Access Time	t _{CD}	3.8	4.2	5.0	ns
Output Enable Access Time	t _{OE}	3.8	4.2	5.0	ns

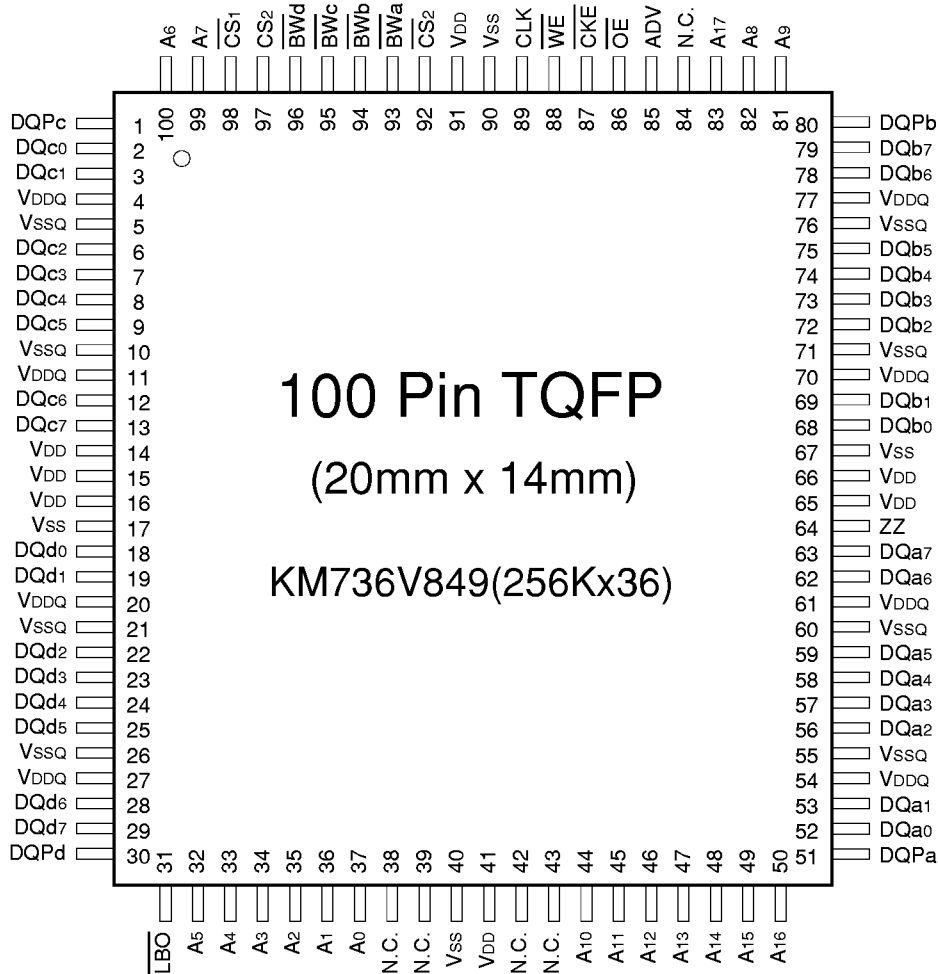
LOGIC BLOCK DIAGRAM



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PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,81 82,83,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
ADV	Address Advance/Load	85	Vss	Ground	17,40,67,90
WE	Read/Write Control Input	88	N.C.	No Connect	38,39,42,43,84
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63 68,69,72,73,74,75,78,79
CKE	Clock Enable	87	DQb0~b7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQc0~c7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQd0~d7		51,80,1,30
CS2	Chip Select	92	DQPa~Pd		
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VssQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

Notes : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM736V849(256Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	NC	A	A	VDDQ
B	NC	CS ₂	A	$\overline{\text{CKE}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	Vss	NC	Vss	DQPb	DQb
E	DQc	DQc	Vss	$\overline{\text{CS}}_1$	Vss	DQb	DQb
F	VDDQ	DQc	Vss	$\overline{\text{OE}}$	Vss	DQb	VDDQ
G	DQc	DQc	$\overline{\text{BW}}_c$	ADV	$\overline{\text{BW}}_b$	DQb	DQb
H	DQc	DQc	Vss	NC	Vss	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{\text{BW}}_d$	NC	$\overline{\text{BW}}_a$	DQa	DQa
M	VDDQ	DQd	Vss	$\overline{\text{WE}}$	Vss	DQa	VDDQ
N	DQd	DQd	Vss	A ₁ *	Vss	DQa	DQa
P	DQd	DQPd	Vss	A ₀ *	Vss	DQP _a	DQ _a
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A ₀ ,A ₁	Burst Address Inputs	Vss	Ground
ADV	Address Advance/Load	N.C.	No Connect
WE	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{\text{CKE}}$	Clock Enable	DQb	Data Inputs/Outputs
CS ₁	Chip Select	DQc	Data Inputs/Outputs
CS ₂	Chip Select	DQd	Data Inputs/Outputs
$\overline{\text{BW}}_x$ (x=a,b,c,d)	Byte Write Inputs	DQP _{a~Pd}	Data Inputs/Outputs
$\overline{\text{OE}}$	Output Enable	VDDQ	Power Supply
ZZ	Power Sleep Mode		
LBO	Burst Mode Control		

FUNCTION DESCRIPTION

The KM736V849 are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of OE, LBO and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(CKE) pin allows the operation of the chip to be suspended as long as necessary. All synchronous inputs are ignored when CKE is high and the internal device registers will hold their previous values.

When CKE is active asserted, ADV is low and all three chip enables(CS1, CS2, CS2) are asserted, NtRAM™ latches external address and initiates a cycle.

Output Enable(OE) can be used to disable the output at any given time.

Read operation is initiated when the following conditions are satisfied at the rising edge of clock, CKE is asserted Low, all three chip enables(CS1, CS2, CS2) are active, the write enable input signals WE is deasserted high, and ADV is asserted Low. The address presented to the address inputs are latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data a propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within provided OE is active Low.

Write operation occurs when WE is sampled Low at the rising edge of clock. BW[d:a] can be used for byte write operation. The Pipelined NtRAM™ uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of clock, WE and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected.

And this pin is High, Interleaved burst sequence is selected.

During normal operation, ZZ must be pulled LOW. When ZZ is pulled HIGH, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, LBO=High)

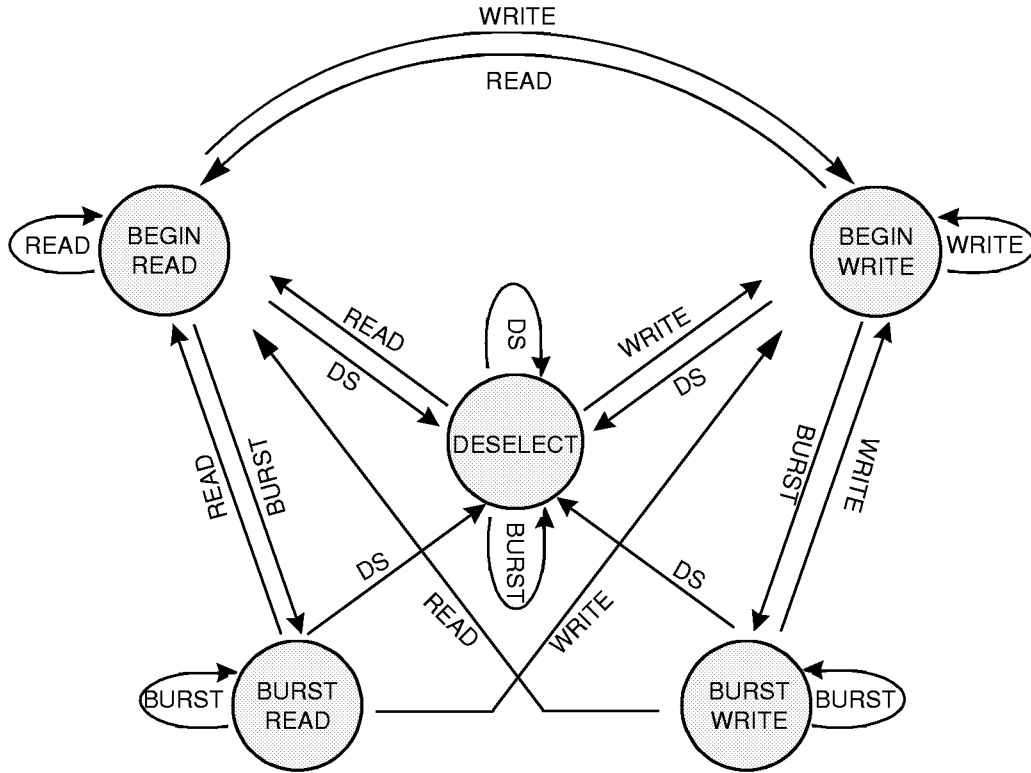
LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst, LBO=Low)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
 2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS ₁	CS ₂	CS ₂	ADV	WE	BW _x	OE	CKE	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :**
1. X means "Don't Care".
 2. The rising edge of clock is symbolized by (↑).
 3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
 4. WRITE = L means Write operation in WRITE TRUTH TABLE.
WRITE = H means Read operation in WRITE TRUTH TABLE.
 5. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE_(x36)

WE	BW _a	BW _b	BW _c	BW _d	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

- Notes :**
1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	\overline{OE}	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to VSS	VIN	-0.3 to 4.6	V
Power Dissipation	PD	1.6	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE* (TA=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	6	pF
Output Capacitance	COU	VOU=0V	-	8	pF

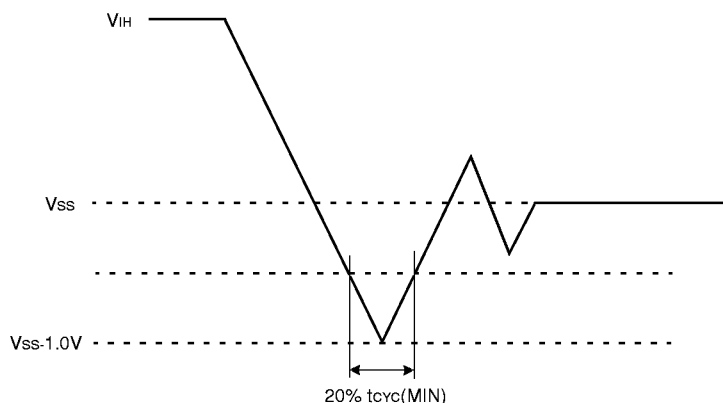
*Note : Sampled not 100% tested.



DC ELECTRICAL CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES	
Input Leakage Current(except ZZ)	I _{IL}	V _{DD} =Max ; V _{IN} =V _{SS} to V _{DD}	-2	+2	μA		
Output Leakage Current	I _{OL}	Output Disabled, V _{out} =V _{SS} to V _{DDQ}	-2	+2	μA		
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ≤V _{IL} , Cycle Time ≥ t _{CYC} Min	-67	-	420	mA	1,2
			-75	-	370		
			-10	-	300		
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ≤V _{IL} , f=Max, All Inputs≤0.2V or ≥ V _{DD} -0.2V	-67	-	80	mA	
			-75	-	70		
			-10	-	60		
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	-	30	mA	
I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ≥V _{DD} -0.2V, f=Max, All Inputs≤V _{IL} or ≥V _{IH}	-	-	30	mA		
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V		
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	V _{IH}		2.0	V _{DD} +0.5**	V	3	
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	V _{IH}		1.7	V _{DD} +0.5**	V	3	

- Notes :** 1. Reference AC Operating Conditions and Characteristics for input and timing.
 2. Data states are all zero.
 3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

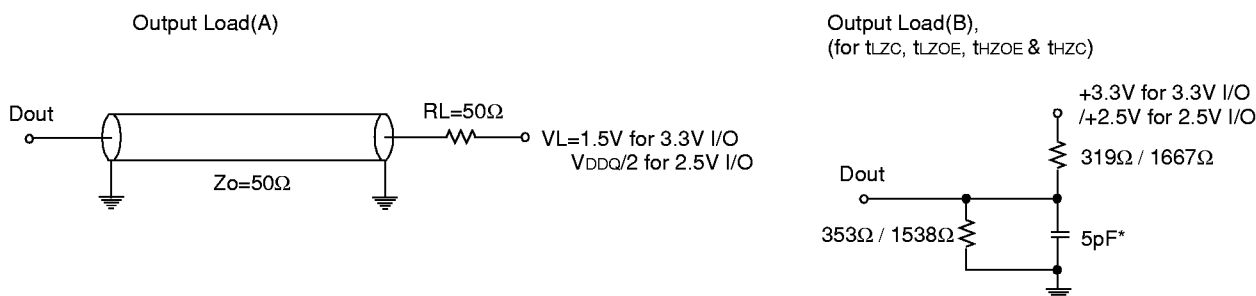


TEST CONDITIONS

(V_{DD}=3.3V+0.165V/-0.165V, V_{DDQ}=3.3V+0.165V/-0.165V or V_{DD}=3.3V+0.165V/-0.165V, V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0to70°C)

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V _{DDQ} /2
Output Load	See Fig. 1





* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0 to 70°C)

PARAMETER	SYMBOL	-67		-75		-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t _{CYC}	6.7	-	7.5	-	10.0	-	ns
Clock Access Time	t _{CD}	-	3.8	-	4.2	-	5.0	ns
Output Enable to Data Valid	t _{OE}	-	3.8	-	4.2	-	5.0	ns
Clock High to Output Low-Z	t _{LZC}	1.5	-	1.5	-	1.5	-	ns
Output Hold from Clock High	t _{OH}	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	3.0	-	3.5	-	3.5	ns
Clock High to Output High-Z	t _{HZC}	-	3.0	-	3.5	-	3.5	ns
Clock High Pulse Width	t _{CH}	2.5	-	3.0	-	3.0	-	ns
Clock Low Pulse Width	t _{CL}	2.5	-	3.0	-	3.0	-	ns
Address Setup to Clock High	t _{AS}	1.5	-	1.5	-	1.5	-	ns
CKE Setup to Clock High	t _{CES}	1.5	-	1.5	-	1.5	-	ns
Data Setup to Clock High	t _{DS}	1.5	-	1.5	-	1.5	-	ns
Write Setup to Clock High (WE, BWx)	t _{WS}	1.5	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.5	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.5	-	1.5	-	1.5	-	ns
Address Hold from Clock High	t _{AH}	0.5	-	0.5	-	0.5	-	ns
CKE Hold from Clock High	t _{CEH}	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (WE, BWEx)	t _{WH}	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t _{PD5}	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	2	-	cycle

- Notes :**
1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
 3. A write cycle is defined by WE low having been registered into the device at ADV Low, A Read cycle is defined by WE High with ADV Low, Both cases must meet setup and hold times.
 4. To avoid bus contention, At a given voltage and temperature t_{clz} is more than t_{chz}.
The specs as shown do not imply bus contention because t_{clz} is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than t_{chz}, which is a Max. parameter(worst case at 70°C,3.135V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
 5. ADV must not be asserted for at least 2 Clocks after leaving ZZ state.

SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

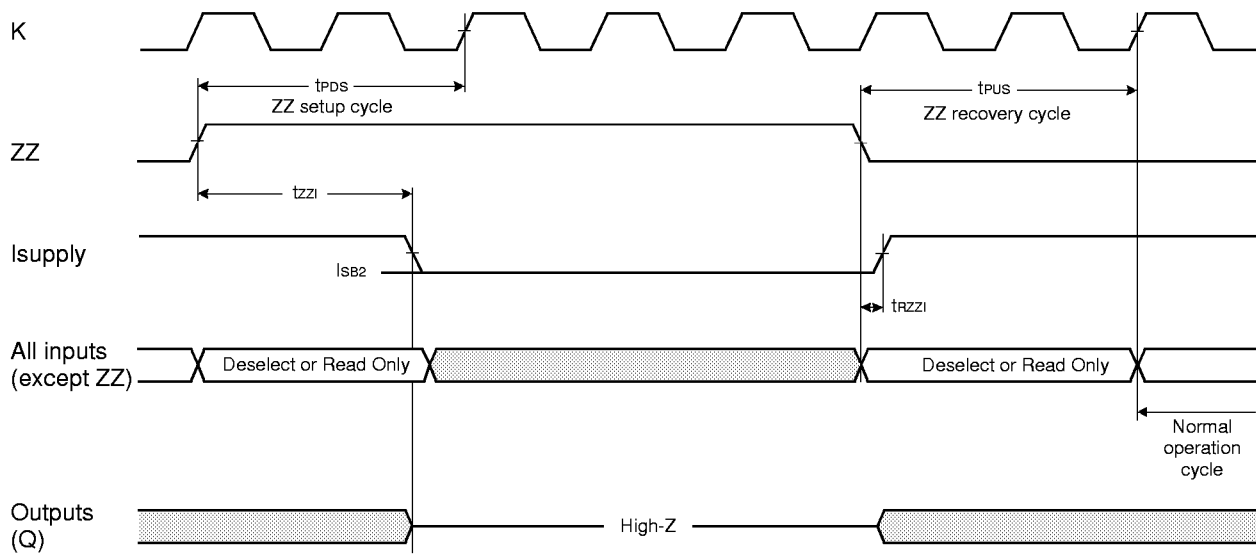
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZ1} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

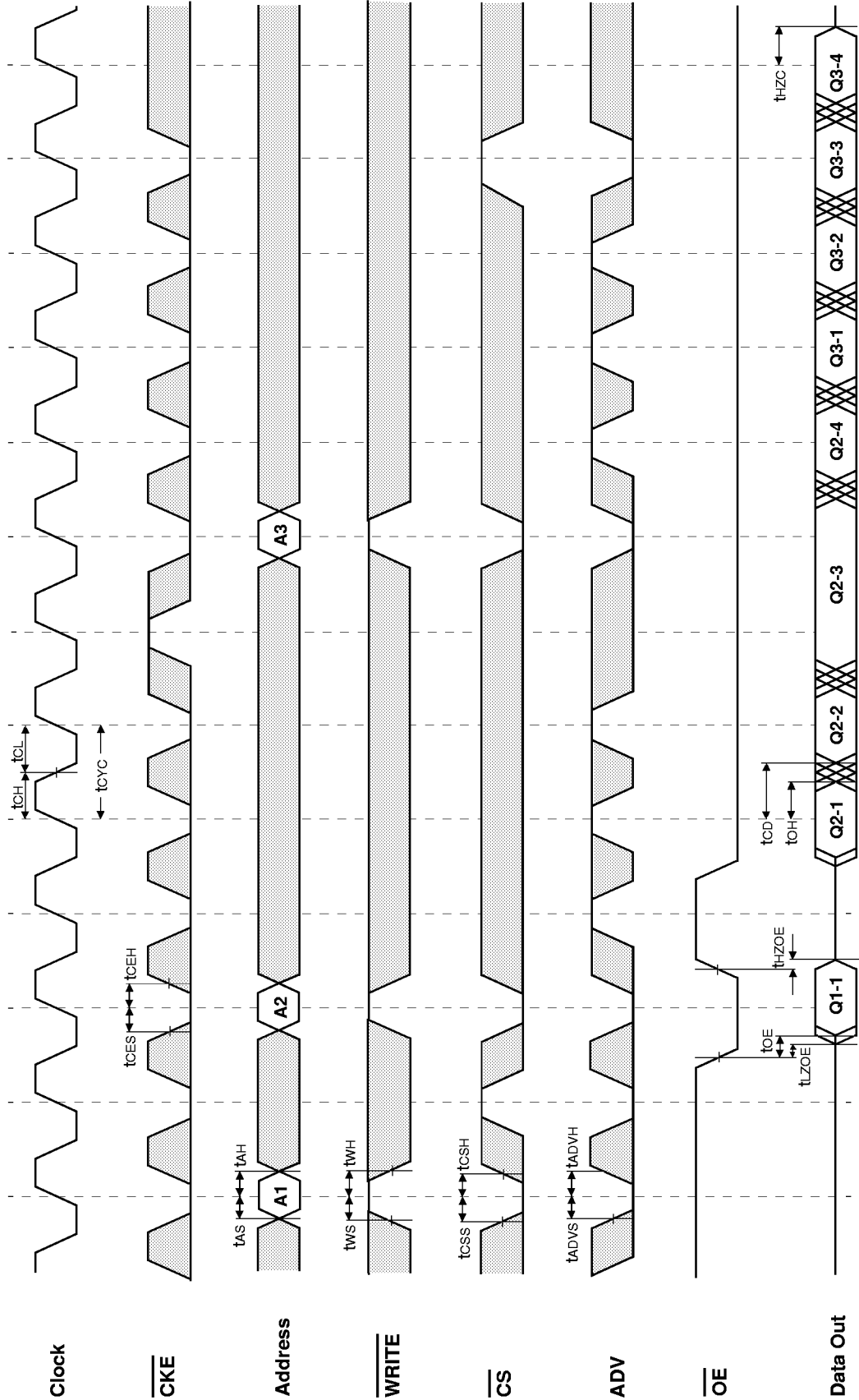
SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		10	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZ1}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZ1}	0		

SLEEP MODE WAVEFORM



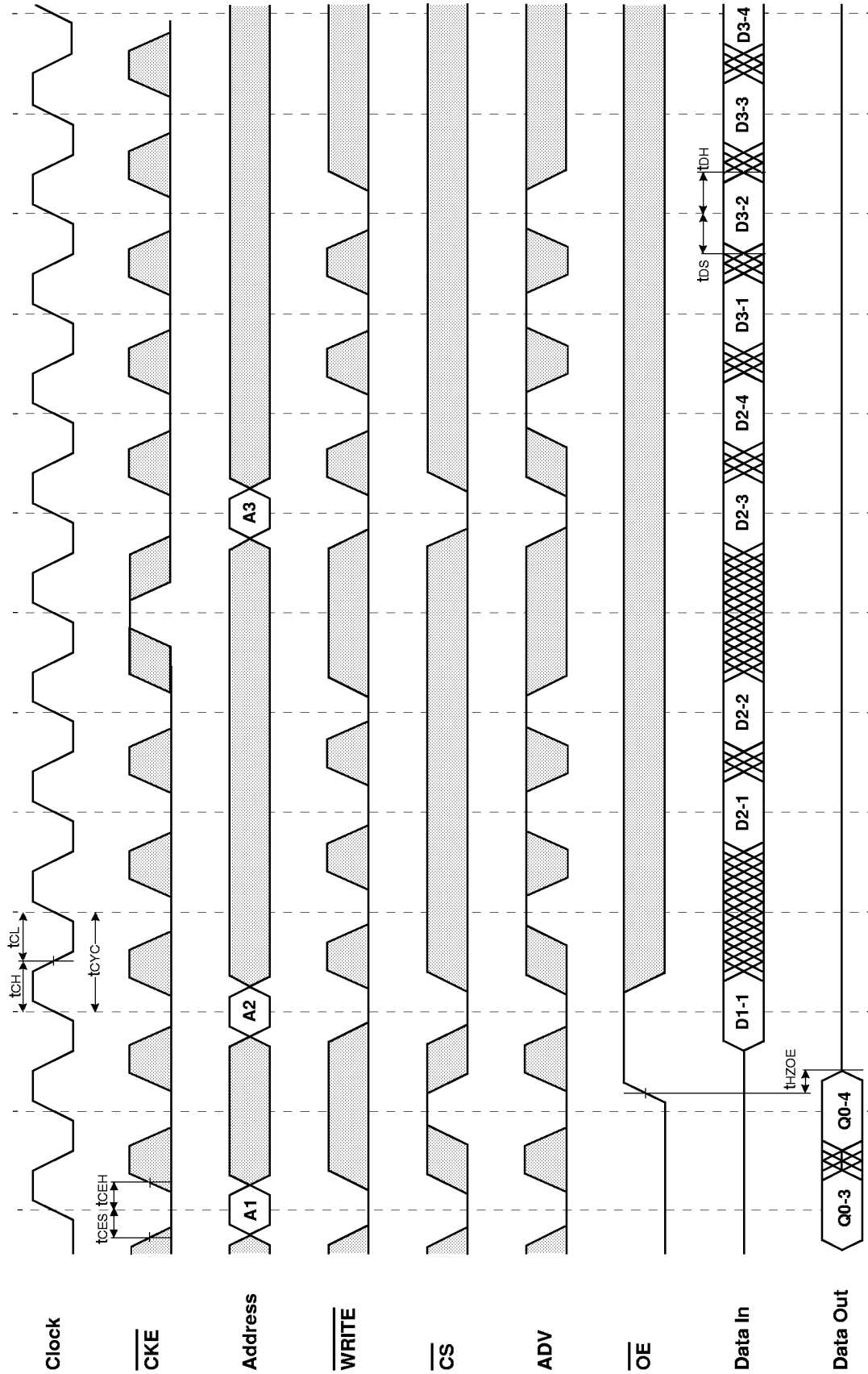
TIMING WAVEFORM OF READ CYCLE



Don't Care
 Undefined

NOTES : $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS1}} = \text{L}$, $\overline{\text{CS2}} = \text{H}$ and $\overline{\text{CS2}} = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS1}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$ and $\overline{\text{CS2}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$, and $\overline{\text{CS2}} = \text{L}$

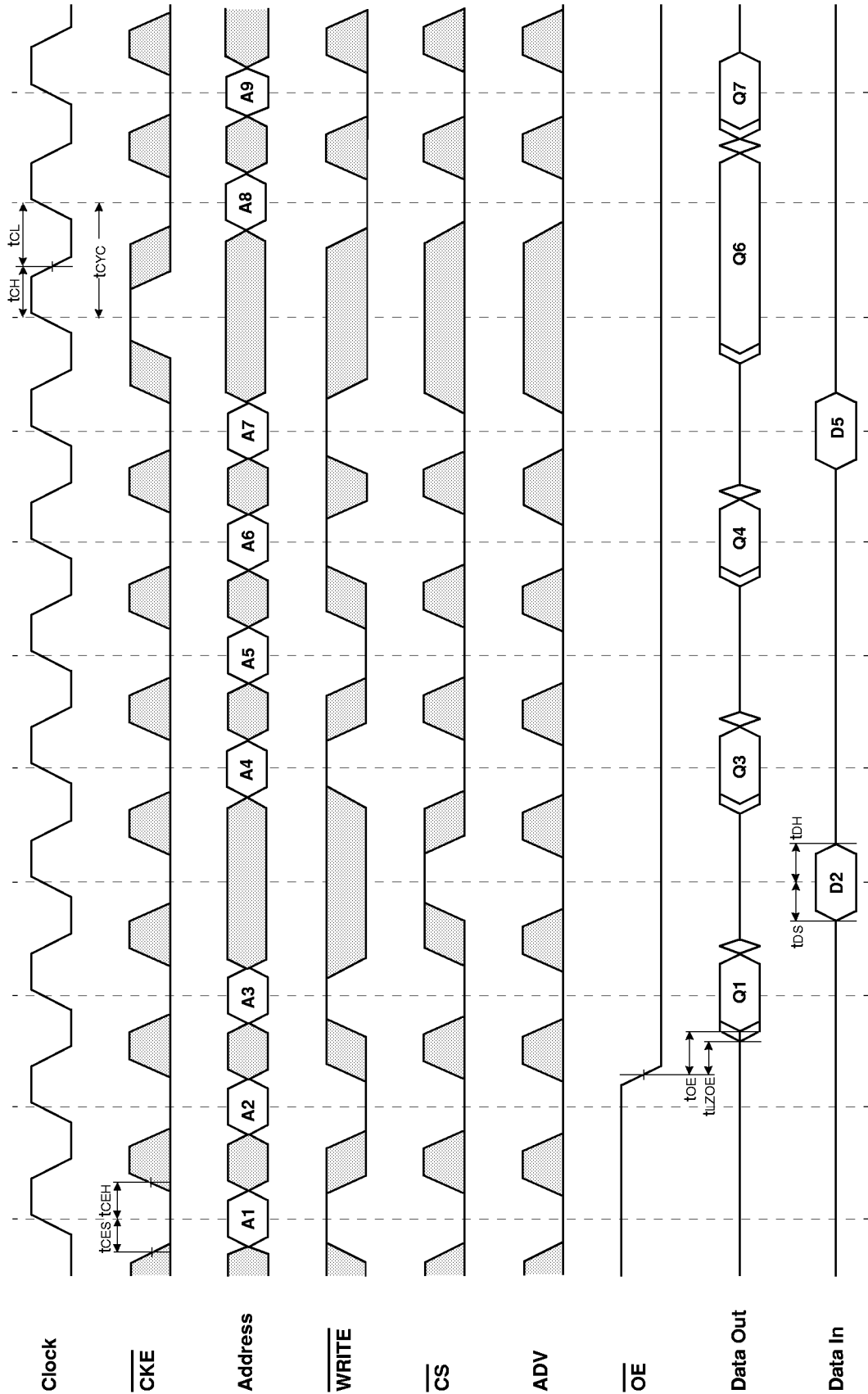
TIMING WAVEFORM OF WRTE CYCLE



Don't Care
 Undefined

NOTES : $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BW}}_x = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

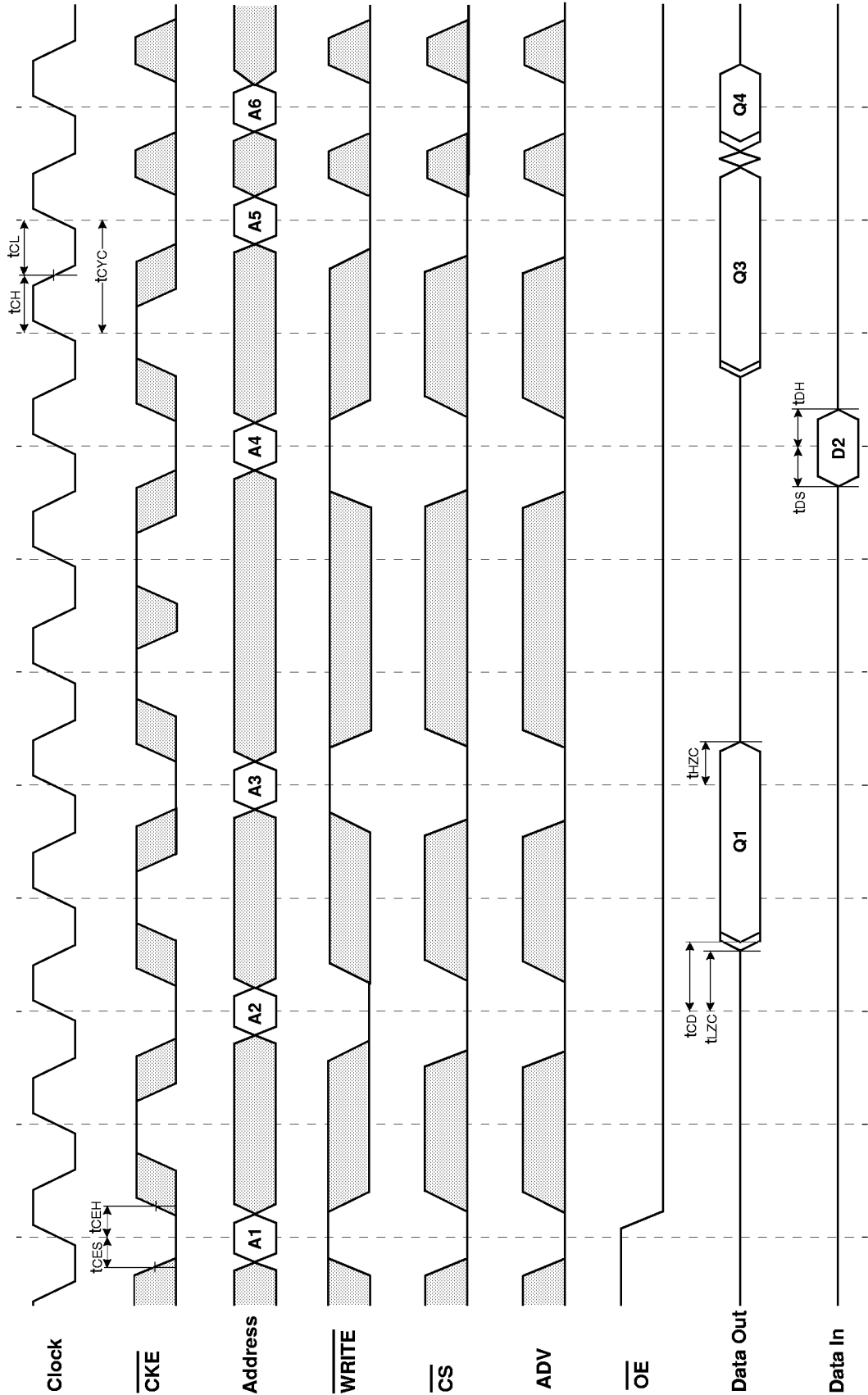
TIMING WAVEFORM OF SINGLE READ/WRITE



Don't Care
 Undefined

NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS1}} = \text{L}$, $\overline{\text{CS2}} = \text{H}$ and $\overline{\text{CS2}} = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS1}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$ and $\overline{\text{CS2}} = \text{H}$, or $\overline{\text{CS1}} = \text{L}$, and $\overline{\text{CS2}} = \text{L}$

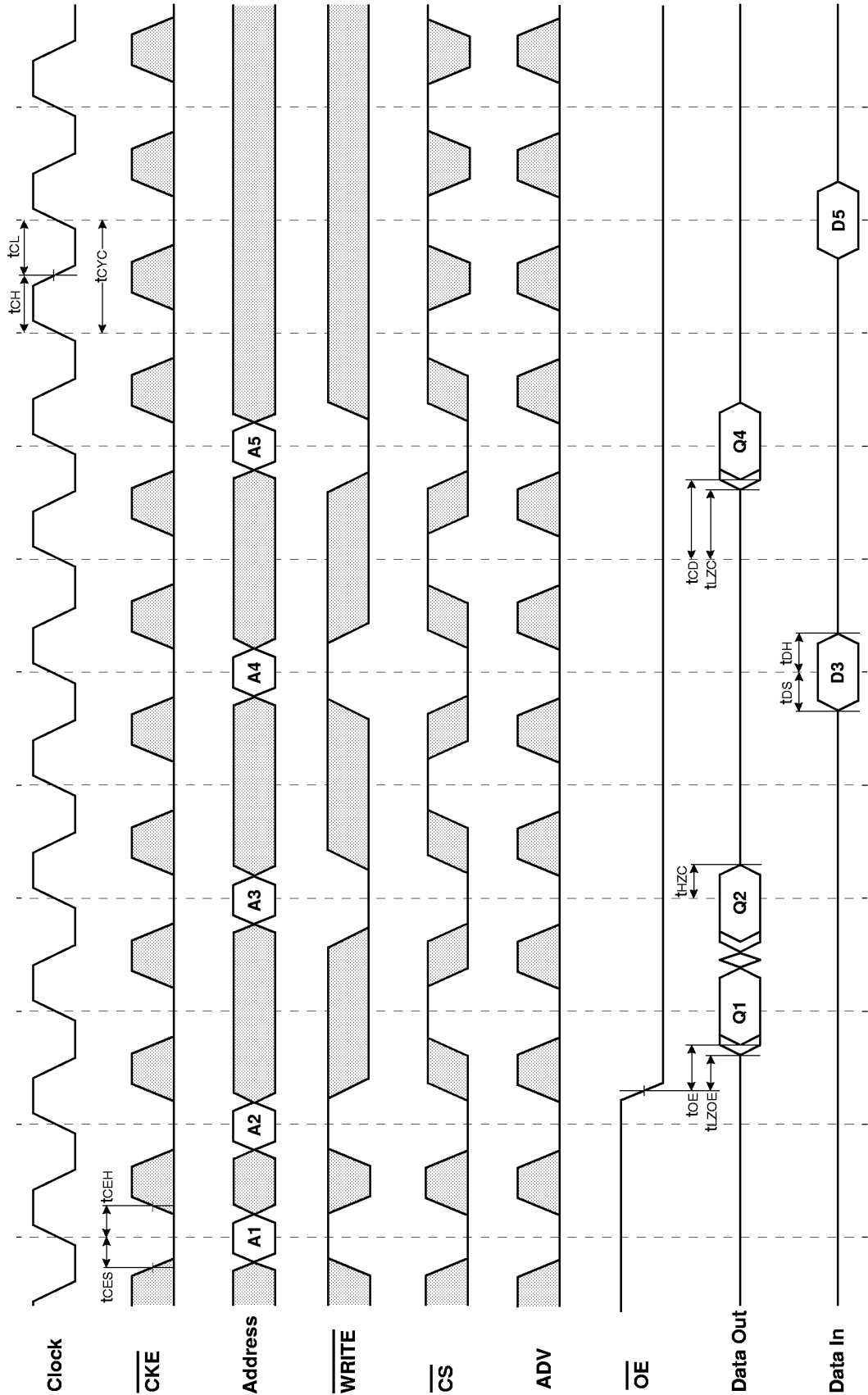
TIMING WAVEFORM OF CKE OPERATION



☐ Don't Care
 ☒ Undefined

NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

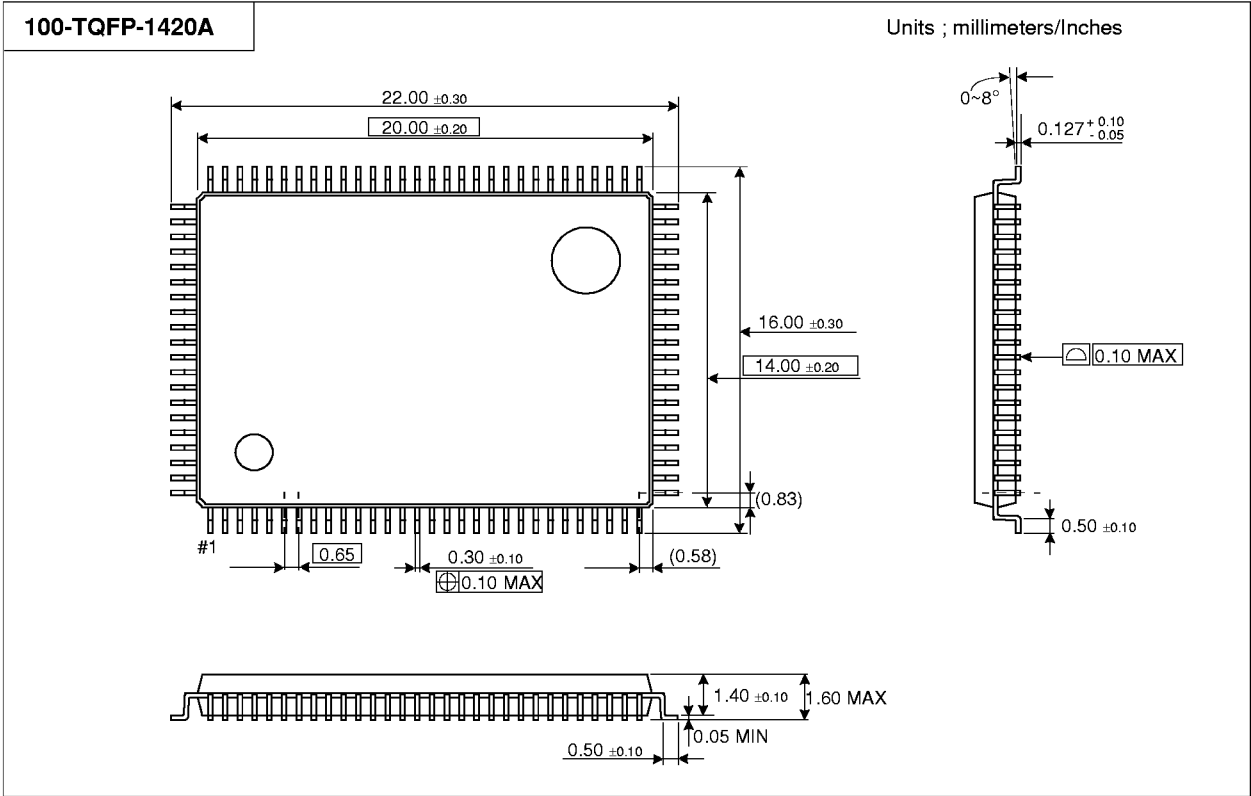
TIMING WAVEFORM OF CS OPERATION



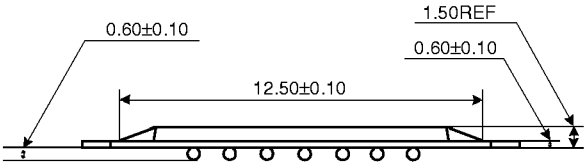
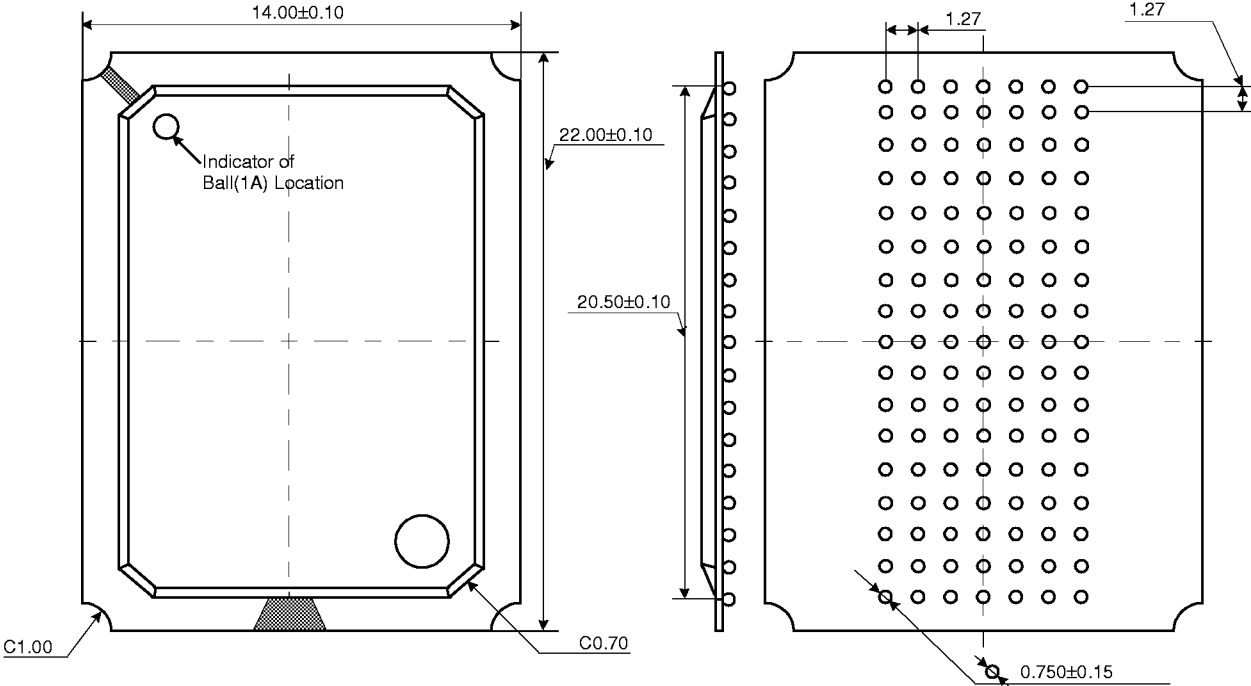
☐ Don't Care
 ☒ Undefined

NOTES: WRITE = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

PACKAGE DIMENSIONS



119BGA PACKAGE DIMENSIONS



- NOTE :**
- 1. All Dimensions are in Millimeters.
 - 2. Solder Ball to PCB Offset : 0.10 MAX.
 - 3. PCB to Cavity Offset : 0.10 MAX.