NEC

MOS INTEGRATED CIRCUIT

μPD432937

2M-BIT CMOS SYNCHRONOUS FAST SRAM
64K-WORD BY 36-BIT
PIPELINED OPERATION / HSTL INTERFACE

Description

The μPD432937 is a 65,536-word by 36-bit synchronous static RAM fabricated with advanced CMOS technology using N-channel four-transistor memory cell.

The μPD432937 integrates unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (K).

The μPD432937 is suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as cache and buffer memory.

The μPD432937GF is packaged in 100-pin plastic LQFP for high density and low capacitive loading.

Features

- 3.3 V (Chip) / 1.6 V (I/O) Supply
- Synchronous operation
- Internally self-timed write control
- Burst read / write : Interleaved burst sequence
- Fully registered inputs and outputs for 4-1-1-1 pipelined burst operation
- All registers triggered off positive clock edge
- Three chip enables for easy depth expansion
- Common I/O using three state outputs
- Internally controlled burst advance
- Free running active high and active low echo clock outputs
- AND tree testability
- Power down mode :

ZZ pin used to place SRAM in power down mode. Stop clock method for power down mode.

Part number	Class	Clock frequency MHz	Maximum supply current		Supply voltage	
			Active mA	Standby mA	Chip V	I/O V
μPD432937	A29	350	400	60	3.3 ± 0.15	1.6 + 0.1/ - 0.15
	A31	325				
	A33	300	350	50		
	A36	275				
	A40	250				

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Ordering Information

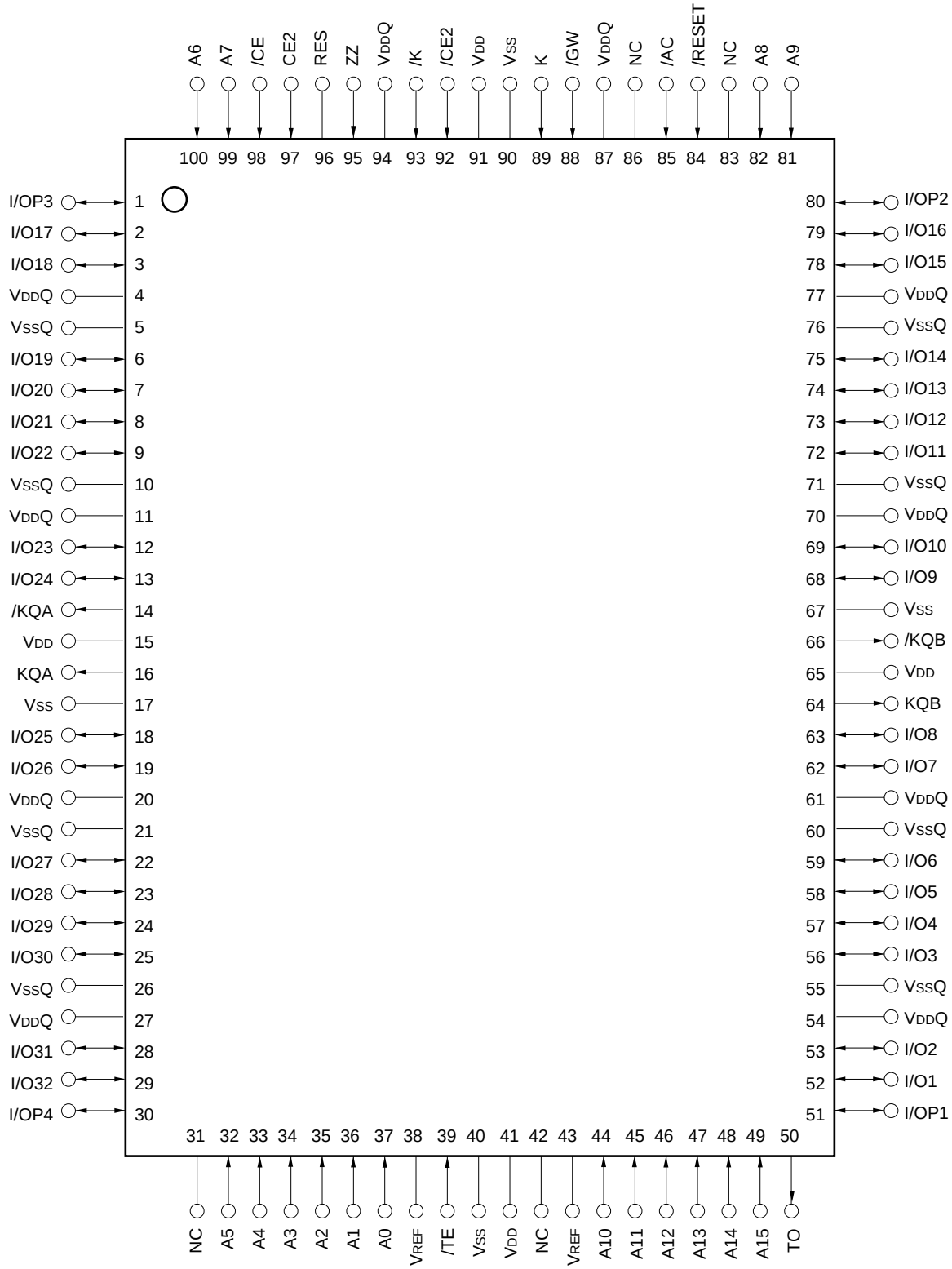
Part number	Clock frequency MHz	Package
μPD432937GF-A29	350	100-pin plastic LQFP (14 × 20 mm)
μPD432937GF-A31	325	
μPD432937GF-A33	300	
μPD432937GF-A36	275	
μPD432937GF-A40	250	

Pin Configuration (Marking Side)

/xxx indicates active low signal.

100-pin plastic LQFP (14 x 20 mm)

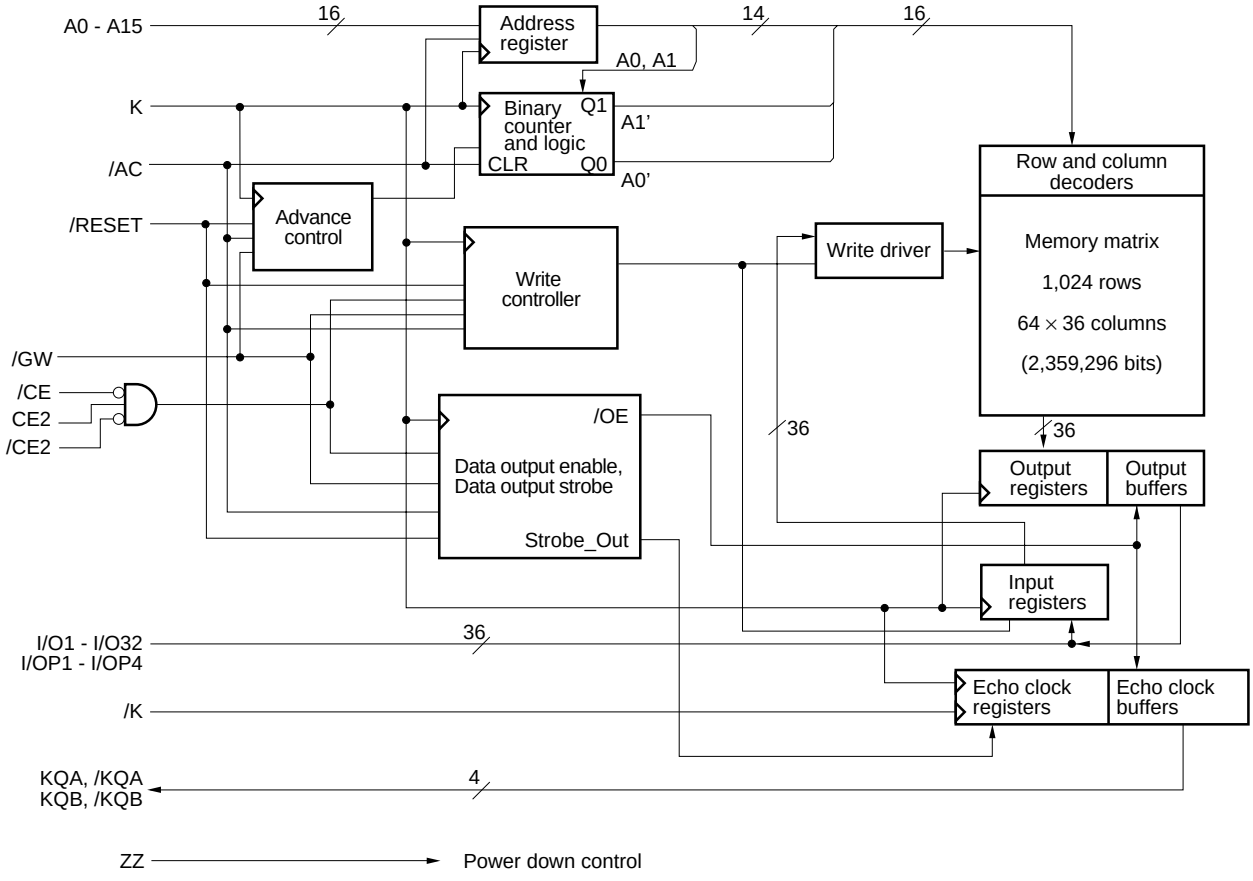
[μPD432937GF]



Pin Identification

Symbol	Pin number	Description
A0 - A15	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49	Synchronous Address Input
I/O1 - I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous Data Out
I/OP1 - I/OP4	51, 80, 1, 30	Synchronous Data In (Parity), Synchronous Data Out (Parity)
KQA, /KQA, KQB, /KQB	16, 14, 64, 66	Echo Clock Output
/AC	85	Synchronous Address Status Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/GW	88	Synchronous Global Write Input
K, /K	89, 93	Differential Input Clock Pair
/RESET	84	Asynchronous Input Initialize internal state at power up
ZZ	95	Asynchronous Power Down State Input
/TE	39	Test Enable Input
TO	50	Test Output
V_{REF}	38, 43	Input Reference Voltage
V_{DD}	15, 41, 65, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77, 87, 94	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	31, 32, 83, 86	No Connection
RES	96	Reserved It must be tied LOW during normal operation

Block Diagram



Burst Sequence

Interleaved Burst Sequence Table

External Address	A15 - A2, A1, A0
1st Burst Address	A15 - A2, A1, /A0
2nd Burst Address	A15 - A2, /A1, A0
3rd Burst Address	A15 - A2, /A1, /A0

Synchronous Truth Table

Operation	/CE	CE2	/CE2	/AC	/GW	I/O	Address
Deselected [Note]	H	×	×	L	×	Hi-Z	None
Deselected [Note]	L	L	×	L	×	Hi-Z	None
Deselected [Note]	L	×	H	L	×	Hi-Z	None
Read Cycle / Begin Burst	L	H	L	L	H	Hi-Z	External
Read Cycle / Continue Burst	×	×	×	H	×	Hi-Z	Current
Read Cycle / Continue Burst	×	×	×	H	×	Hi-Z	Current
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	Next
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	Next
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	Next
Read Cycle / Continue Burst	×	×	×	H	×	Data-out	None
Write Cycle / Begin Burst	L	H	L	L	L	Hi-Z	External
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Current
Write Cycle / Continue Burst	×	×	×	H	L	Data-in	Next
Write Cycle / Continue Burst	×	×	×	H	×	Data-in	Next
Write Cycle / Continue Burst	×	×	×	H	×	Hi-Z	Next

Note Deselect status is held until new “Begin Burst” entry.

Remark × : don’t care

Asynchronous Truth Table

ZZ	/RESET	/TE	I/O	Operation
H	H	H	Hi-Z	Sleep Mode
×	L	H	Hi-Z	Reset
×	×	L	Hi-Z	Test Mode
L	H	H	Data-out	Read
L	H	H	Data-in	Write

Remark × : don’t care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		–0.5		+4.0	V	
Output supply voltage	$V_{DD}Q$		–0.5		V_{DD}	V	
Input voltage	V_{IN}		–0.5		$V_{DD}Q$ + 0.5	V	1
Input / Output voltage	$V_{I/O}$		–0.5		$V_{DD}Q$ + 0.5	V	1
Operating ambient temperature	T_A		0		70	°C	
Storage temperature	T_{stg}		–55		+125	°C	

Note 1. –1.0 V (MIN.) (Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		3.15	3.3	3.45	V	
Output supply voltage	$V_{DD}Q$		1.45	1.6	1.7	V	
High level input voltage	V_{IH}		V_{REF} + 0.1		$V_{DD}Q$ + 0.3	V	
Low level input voltage	V_{IL}		–0.3		V_{REF} – 0.1	V	1
Input reference voltage	V_{REF}		0.7	$V_{DD}Q$ / 2	0.85	V	

Note 1. –1.0 V (MIN.) (Pulse width : 2 ns)

Recommended AC Operating Conditions (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input reference voltage	$V_{REF(RMS)}$		–5 %		+5 %	V	
Low level input voltage	V_{IL}		–0.3		V_{REF} – 0.2	V	
High level input voltage	V_{IH}		V_{REF} + 0.2		$V_{DD}Q$ + 0.3	V	

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Note
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF	
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			7	pF	
Clock input capacitance	C_{clk}	V_{clk} = 0 V			7	pF	1

Note 1. C_{clk} is for both K and /K.

Remark These parameters are periodically sampled and not 100% tested.

DC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.15 V)

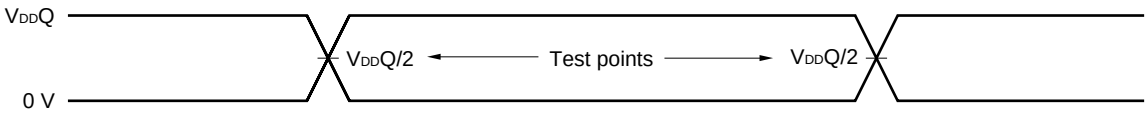
Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit	Note
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{DD}		–2		+2	μA	
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{DD}, Output disabled.		–2		+2	μA	
Operating supply current	I_{DD}	Device selected, Cycle = MAX.,	-A29			400	mA	
		$V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}Q$ – 0.2 V	-A31			400		
			-A33			350		
			-A36			350		
			-A40			350		
Operating $V_{DD}Q$ supply current	$I_{DD}Q$	All outputs toggling, Cycle = MAX.,	-A29			437	mA	1
		C_L = 20 pF	-A31			406		
			-A33			374		
			-A36			343		
			-A40			311		
Standby supply current	I_{SB}	Device deselected, Cycle = MAX.,	-A29			150	mA	
		$V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}Q$ – 0.2 V,	-A31			150		
		All inputs are static.	-A33			110		
			-A36			110		
			-A40			110		
	I_{SB1}	Device deselected,	-A29			60	mA	
		Cycle = 0 MHz,	-A31			60		
		$V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}Q$ – 0.2 V,	-A33			50		
		All inputs are static.	-A36			50		
			-A40			50		
	I_{SB2}	Sleep Mode (ZZ = V_{IH}), All inputs are static.				5.0	mA	
High level output voltage	V_{OH}	$V_{DD}Q$ = 1.45 to 1.7 V, I_{OH} = –1 mA		$V_{DD}Q$–0.4			V	
Low level output voltage	V_{OL}	$V_{DD}Q$ = 1.45 to 1.7 V, I_{OL} = +1 mA				0.4	V	

Note 1. See next page.

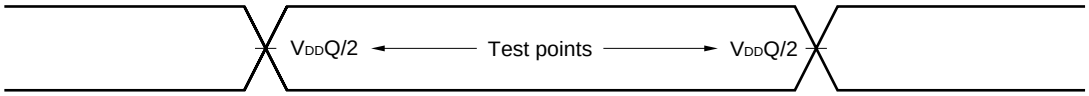
AC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.15 V, $V_{DD}Q$ = 1.45 to 1.7 V)

AC Test Conditions

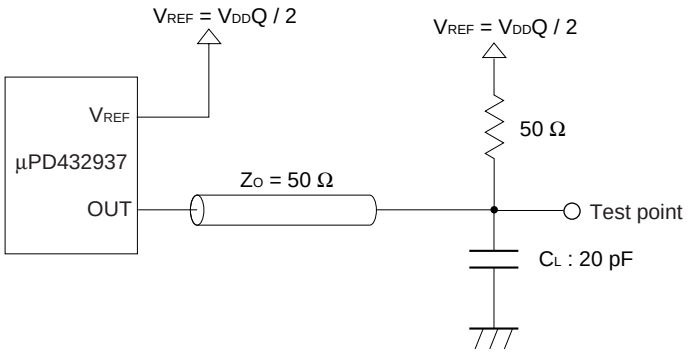
Input waveform (Rise / Fall time : 1.0 V / ns)



Output waveform



Output load condition

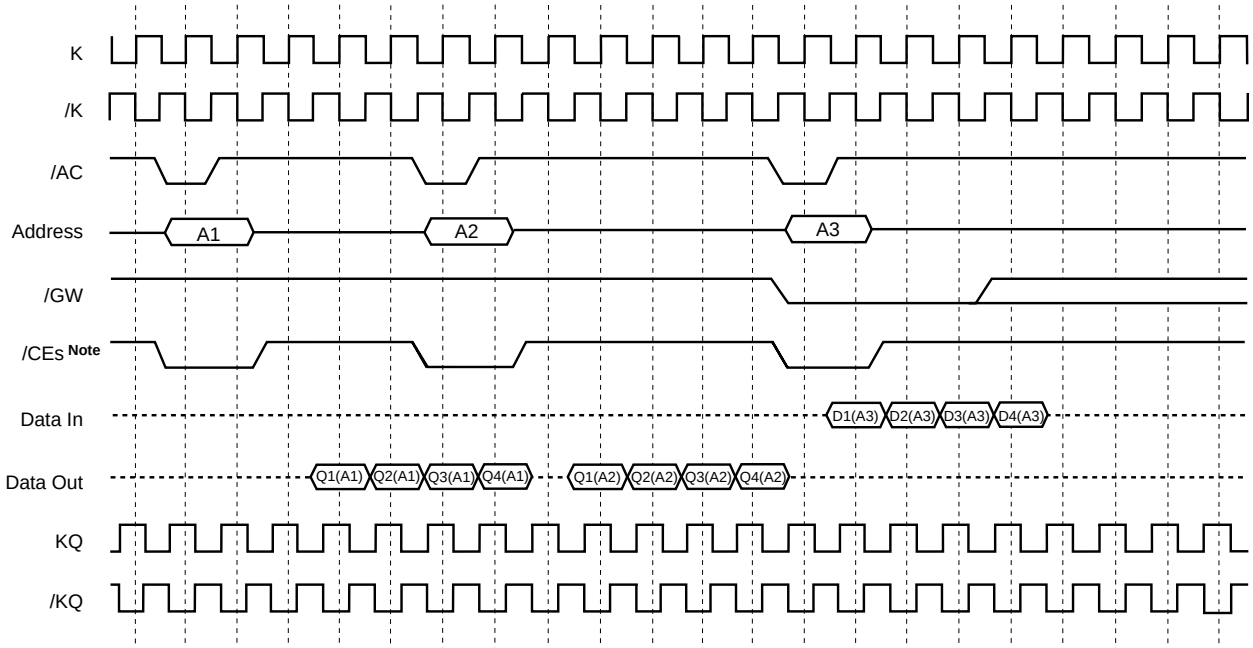


Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

Parameter		Symbol	-A29 (350 MHz)		-A31 (325 MHz)		-A33 (300 MHz)		-A36 (275 MHz)		-A40 (250 MHz)		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time		TKHKH	2.85	–	3.07	–	3.3	–	3.6	–	4.0	–	ns	
Clock high pulse width		TKHKL	1.02	–	1.1	–	1.2	–	1.32	–	1.45	–	ns	
Clock low pulse width		TKLKH	1.02	–	1.1	–	1.2	–	1.32	–	1.45	–	ns	
Clock (K) to clock (/K)		TKHKB	1.28	1.58	1.38	1.70	1.50	1.83	1.65	1.99	1.82	2.18	ns	
Clock to echo clock (/KQ) low		TKHKE	1.1	2.1	1.1	2.3	1.1	2.6	1.1	2.9	1.1	3.2	ns	
Output setup to Echo clock (/KQ)		TQVKE	0.9	–	0.9	–	0.9	–	0.9	–	0.9	–	ns	
Output hold from echo clock (/KQ)		TKEQX	0.9	–	0.9	–	0.9	–	0.9	–	0.9	–	ns	
Setup time	Address	TAVKH	0.7	–	0.8	–	0.9	–	1.0	–	1.2	–	ns	
	Address status	TADSVKH	0.7	–	0.8	–	0.9	–	1.0	–	1.2	–	ns	
	Data-in	TDVKH	0.8	–	0.9	–	1.0	–	1.1	–	1.3	–	ns	
	Global write	TWVKH	0.7	–	0.8	–	0.9	–	1.0	–	1.2	–	ns	
	Chip enable	TCVKH	0.7	–	0.8	–	0.9	–	1.0	–	1.2	–	ns	
Hold time	Address	TKHAX	2.6	–	2.9	–	3.2	–	3.6	–	4.0	–	ns	
	Address status	TKHADSX	0.25	–	0.35	–	0.45	–	0.6	–	0.7	–	ns	
	Data-in	TKHDX	0.15	–	0.25	–	0.35	–	0.5	–	0.65	–	ns	
	Global write	TKHWX	0.25	–	0.35	–	0.45	–	0.6	–	0.5	–	ns	
	Chip enable	TKHCX	2.6	–	2.9	–	3.2	–	3.6	–	4.0	–	ns	
ZZ recovery time		TZZR	2	–	2	–	2	–	2	–	2	–	clocks	

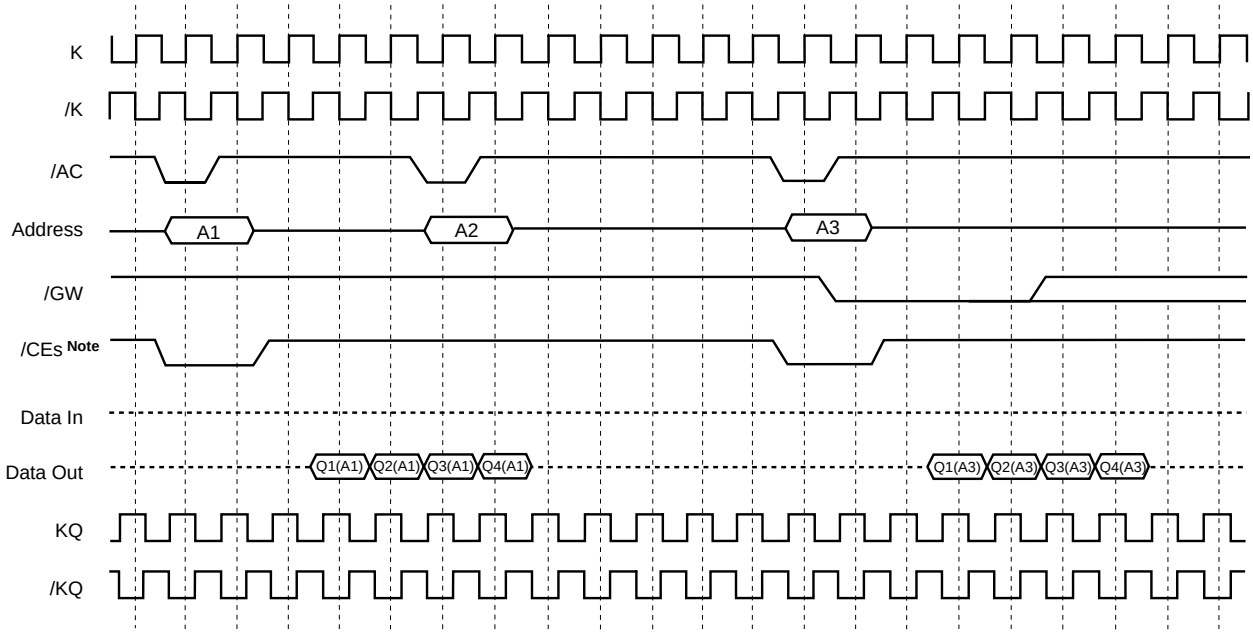
READ - READ - WRITE



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

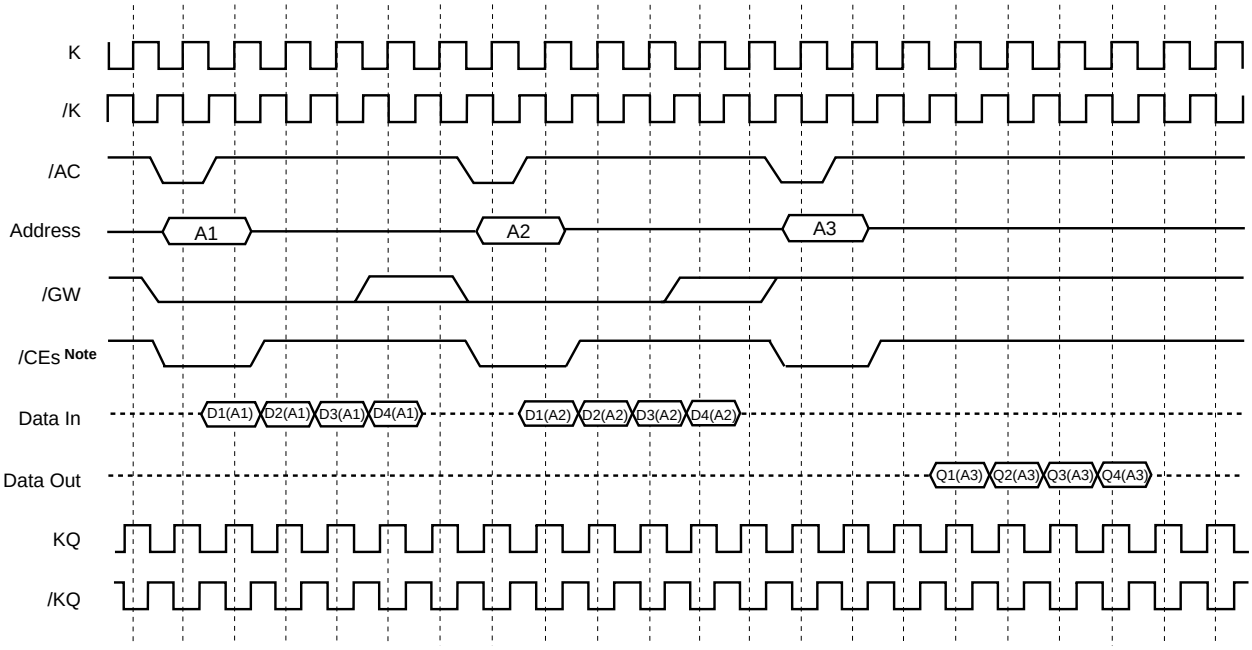
READ - DESELECT (standby) - READ



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

Remark Qn(A1) refers to output from address A1. Q1-Q4 refer to outputs according to burst sequence.

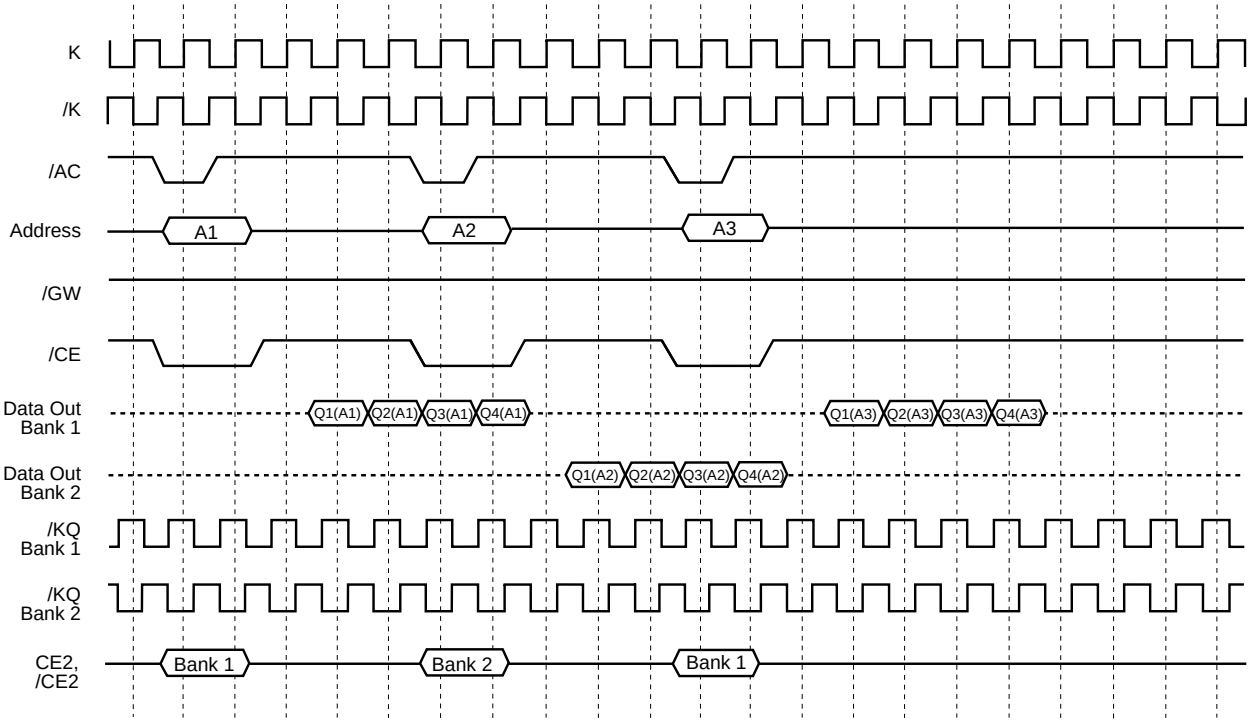
WRITE - WRITE - READ



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

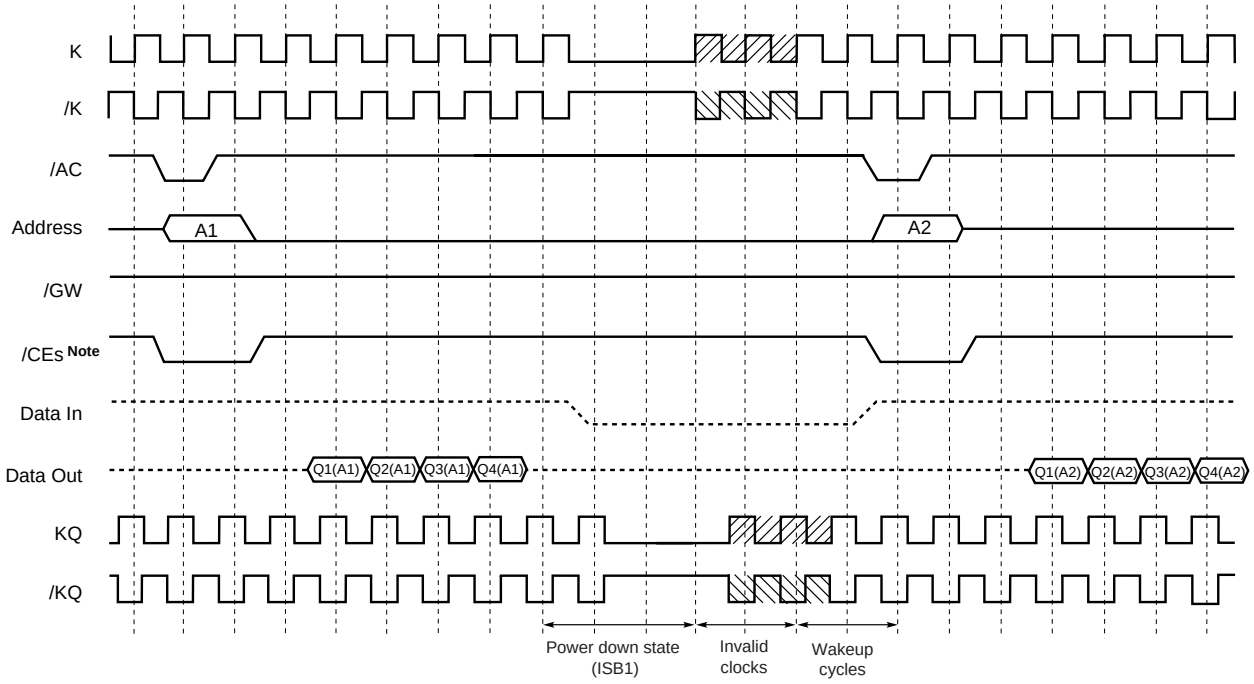
Remark Qn(A3) refers to output from address A3. Q1-Q4 refer to outputs according to burst sequence.

DUAL BANK READ



Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

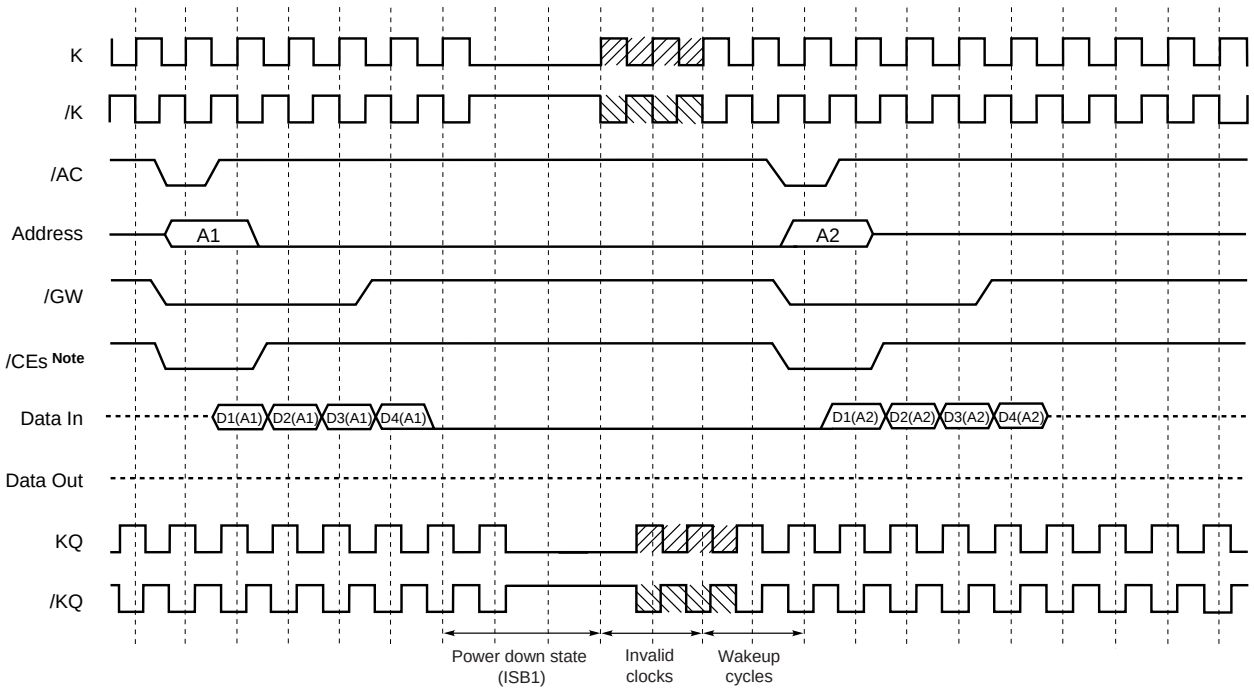
STOP CLOCK OPERATION (READ)



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

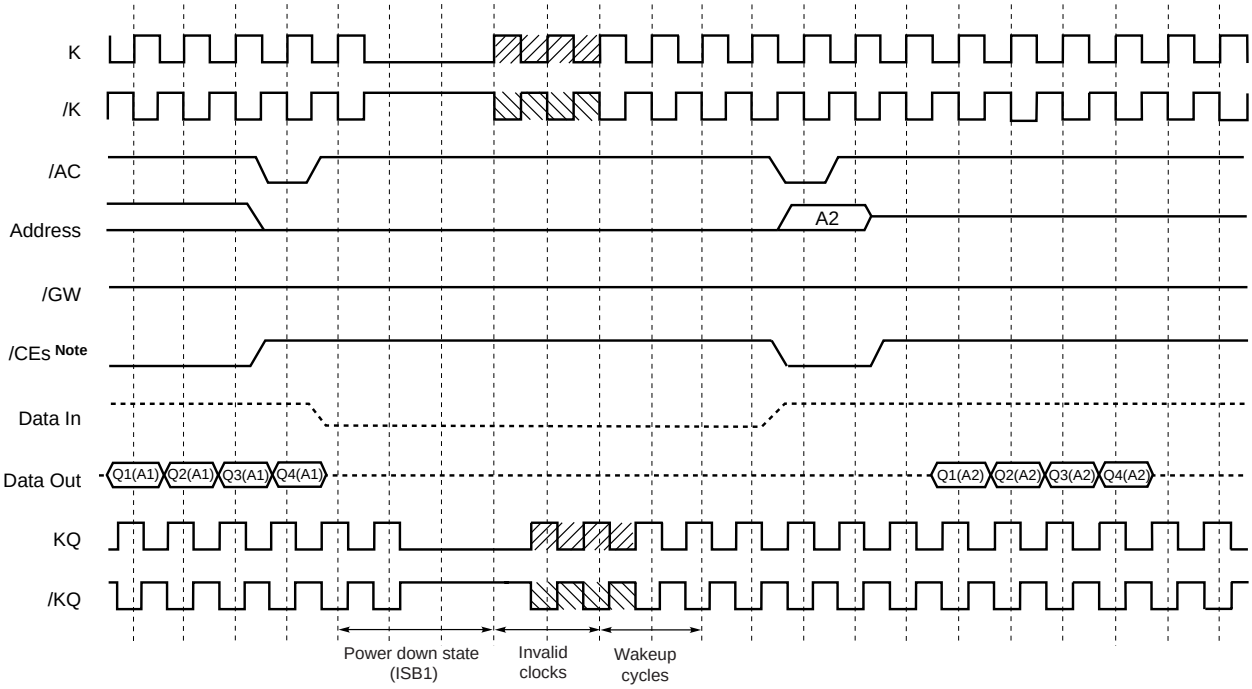
Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

STOP CLOCK OPERATION (WRITE)



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

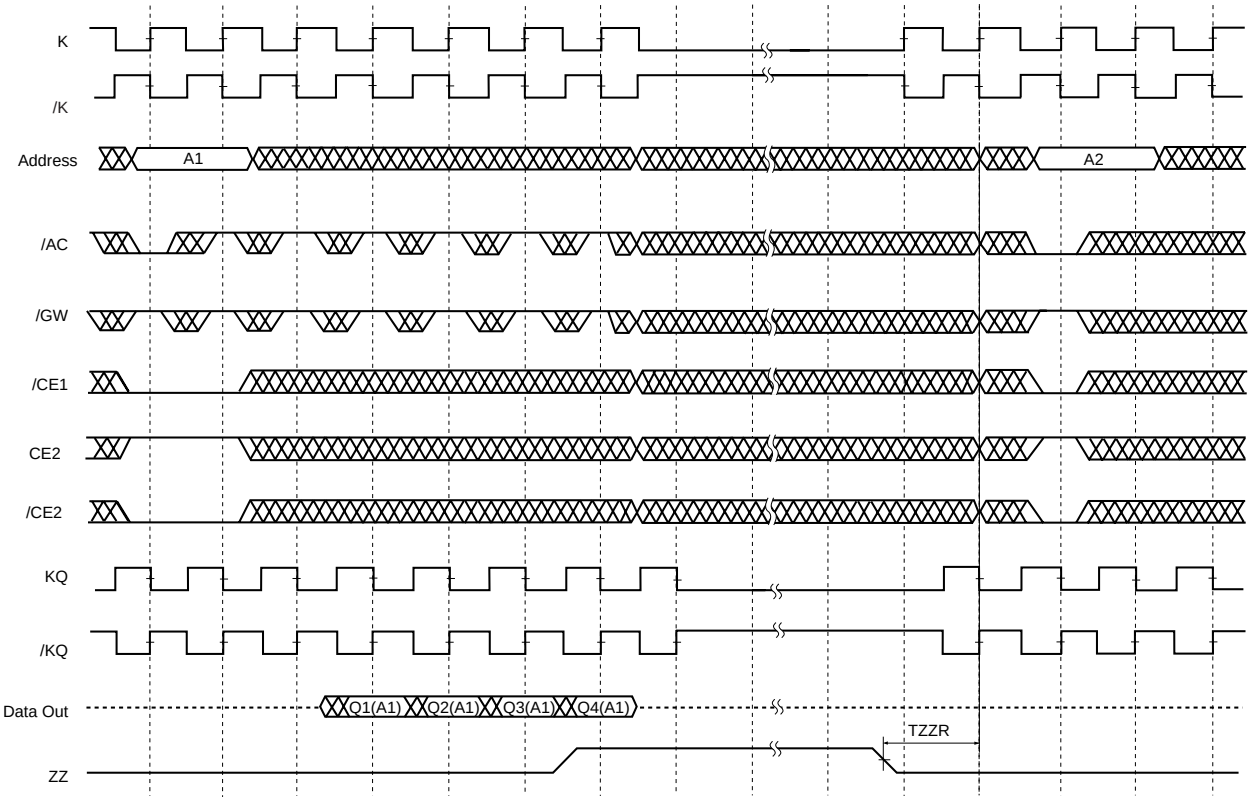
STOP CLOCK OPERATION (DESELECT)



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

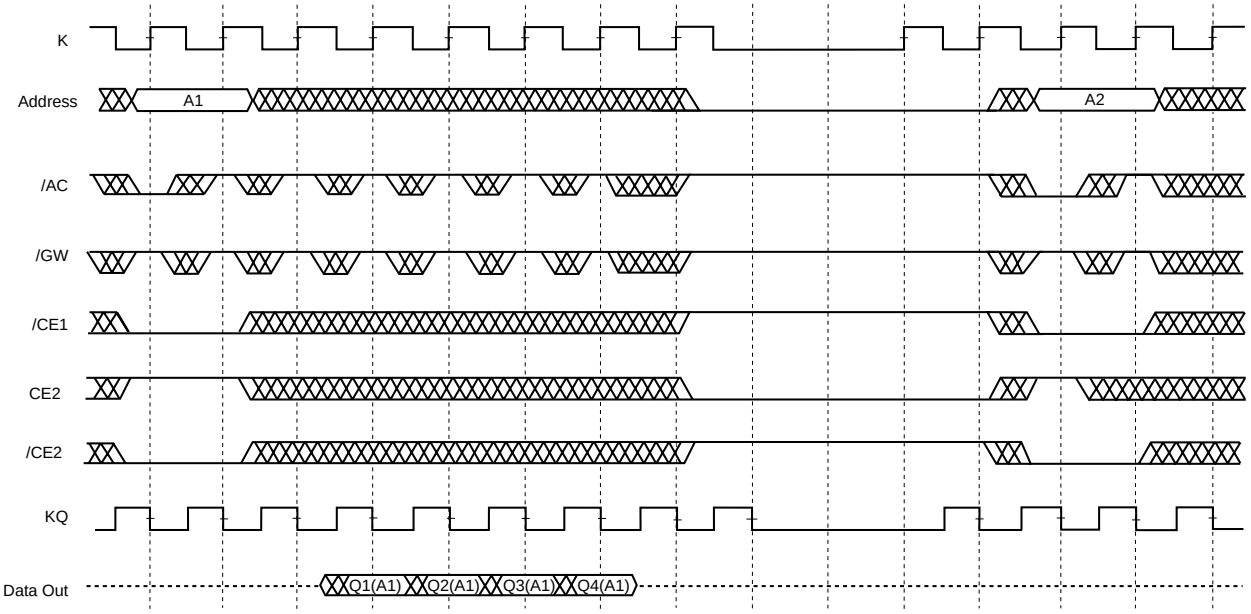
Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

POWER DOWN CYCLE (using ZZ)



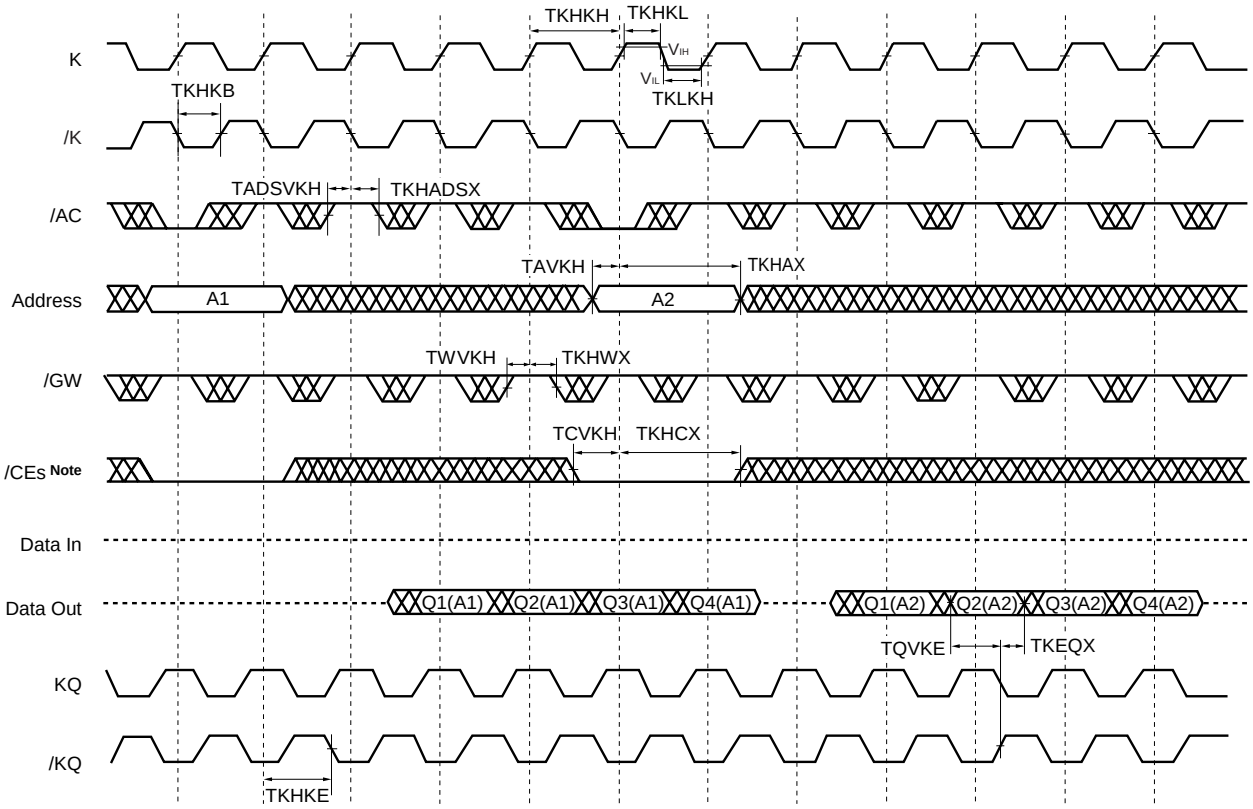
Remark Qn(A1) refers to output from address A1. Q1-Q4 refer to outputs according to burst sequence.

POWER DOWN CYCLE (using STOP CLOCK Method)



Remark Qn(A1) refers to output from address A1. Q1-Q4 refer to outputs according to burst sequence.

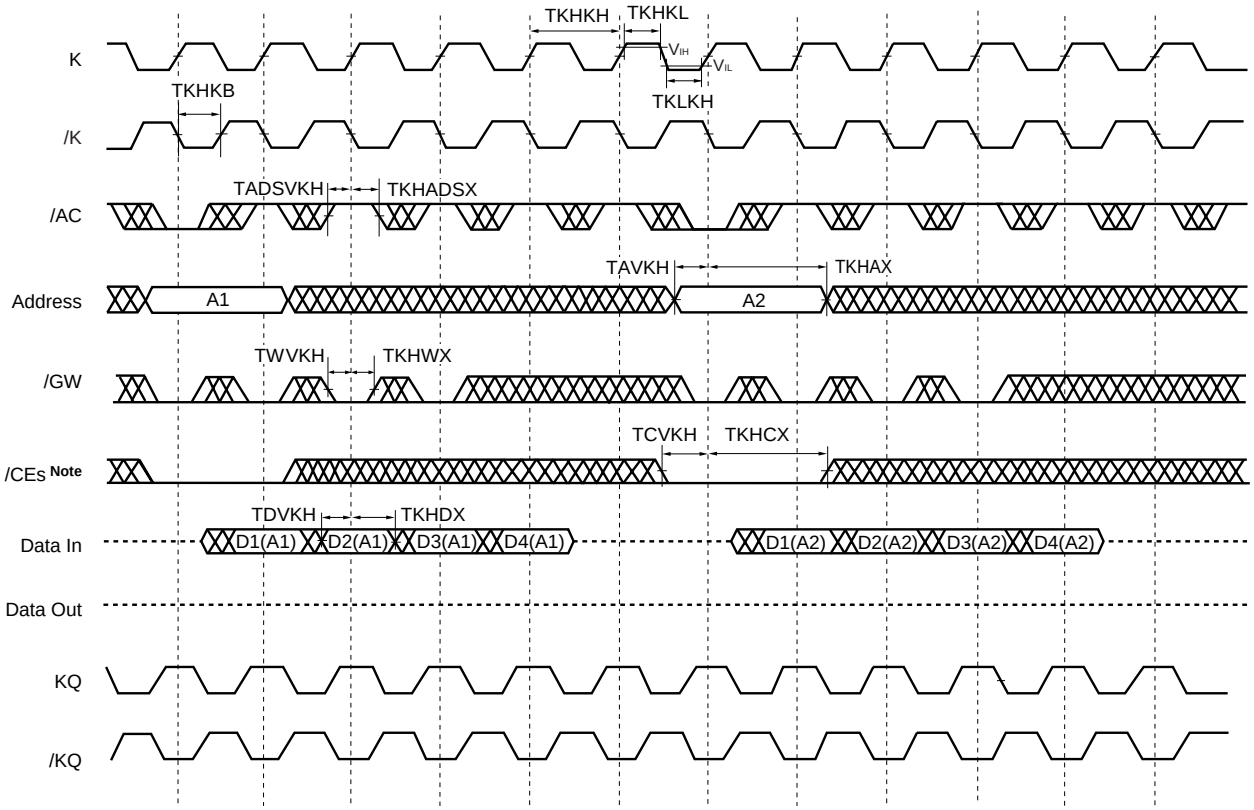
READ CYCLE



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

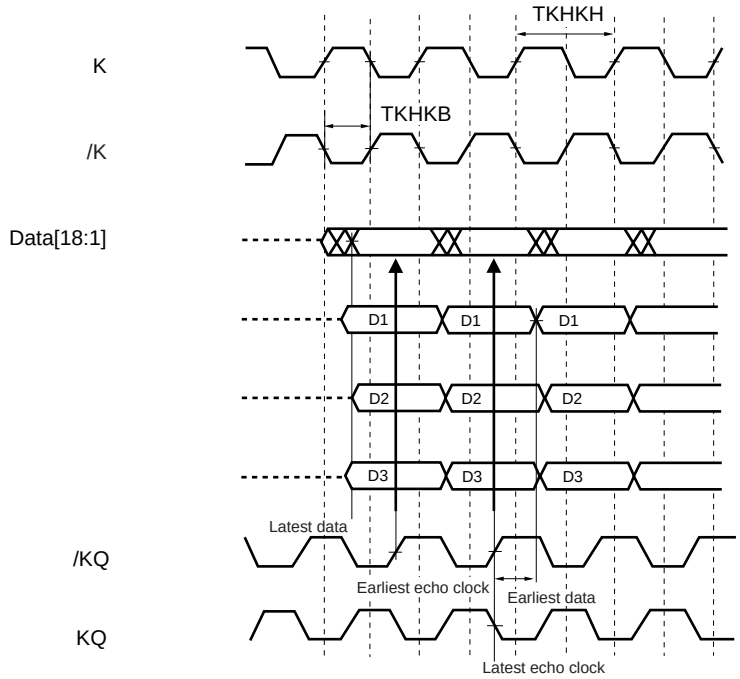
Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

WRITE CYCLE

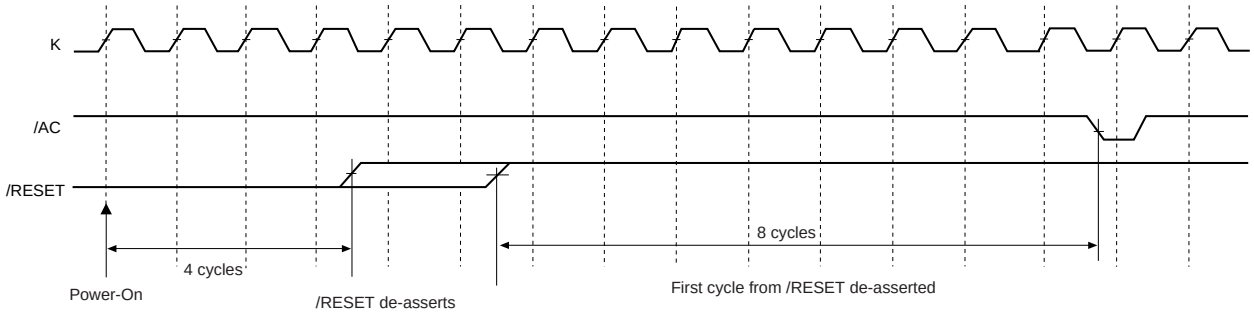


Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

TIMING DIAGRAM REFERENCE for CENTERED ECHO CLOCK



RESET OPERATION

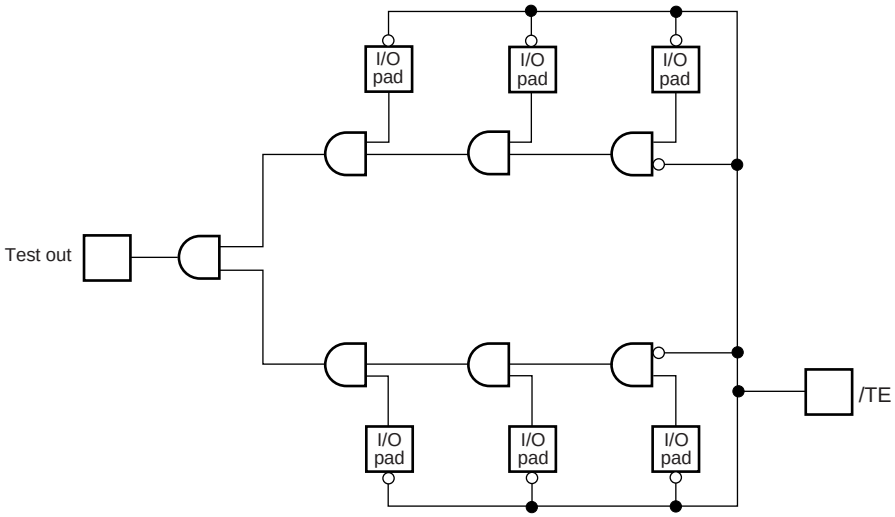


Remark This device needs this RESET OPERATION after power-up.

Testability

Testability in this device is achieved by the use of a cascaded AND tree structure. Test mode is selected by asserting the Test Enable pin (/TE) low. When in Test Mode, the all of the pins of this device that make an actual connection with the die, with the exception of /TE, Test Out (TO), V_{DD}, $V_{DD}Q$, V_{REF}, V_{SS} and all clock pins, act as inputs to a large, cascaded AND tree structure to produce a single output on the Test Out (TO) pin. Input voltages during test mode are operated off $V_{DD}Q$. During test mode, V_{REF} will operate as normal within the range specified in the DC Characteristic section earlier in this document. A simplified illustration of this AND tree is shown below. By walking specific values around the pins of this device, open connections between the circuit board and this device can be detected on the TO pin. When /TE is deasserted, the device operates in a normal manner.

AND TREE STRUCTURE EXAMPLE



Truth Table for /TE and TO Pins

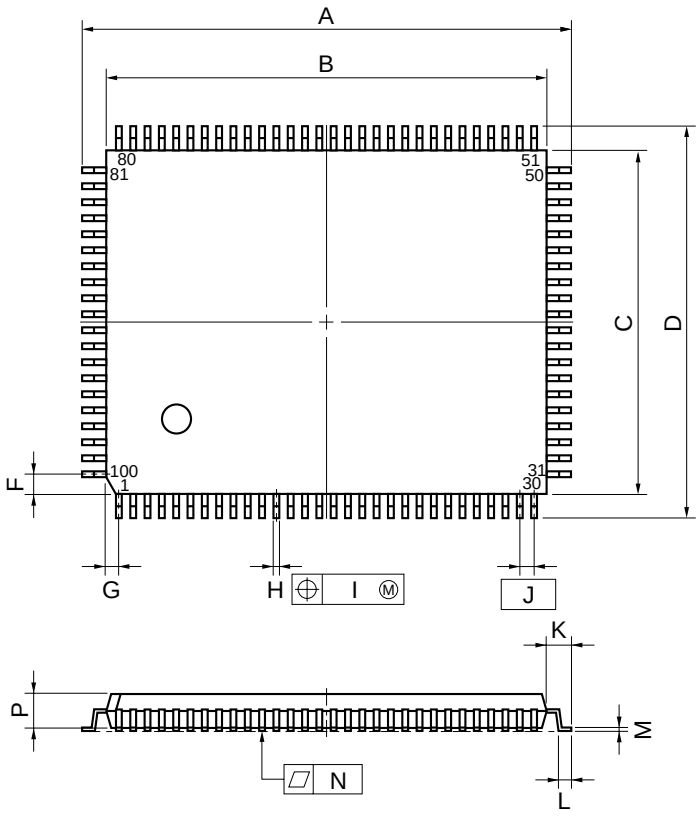
/TE	TO	Mode
0	AND of all listed inputs	Test Mode
1	Hi-Z	Normal Mode

Test input assignments for μPD432937 (64 K words x 36 bits), 100 pin plastic LQFP

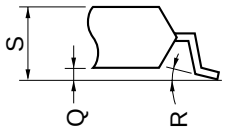
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
I/OP3	1	I/O30	28	A10	44	I/O3	56
I/O17	2	A7	99	A11	45	I/O4	57
I/O18	3	A6	100	A12	46	I/O5	58
I/O19	6	I/O32	29	A1	36	I/O6	59
I/O20	7	I/OP4	30	A0	37	I/O7	62
I/O21	8	A5	32	RES	96	I/O8	63
I/O22	9	/CE	98	/RESET	84	I/O9	68
I/O23	12	/CE2	92	A13	47	I/O10	69
I/O24	13	ZZ	95	A14	48	I/O11	72
I/O25	18	A4	33	A15	49	I/O12	73
I/O26	19	A3	34	A9	81	I/O13	74
I/O27	22	A2	35	A8	82	I/O14	75
I/O28	23	CE2	97	I/OP1	51	I/O15	78
I/O29	24	/GW	88	I/O1	52	I/O16	79
I/O30	25	/AC	85	I/O2	53	I/OP4	80

Package Drawing

100 PIN PLASTIC LQFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	0.825	0.032
G	0.575	0.023
H	$0.32^{+0.08}_{-0.07}$	0.013±0.003
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.06}_{-0.05}$	0.007±0.002
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S100GF-65-8ET

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD432937.

Type of Surface Mount Devices

μPD432937GF : 100-pin plastic LQFP (14 x 20 mm)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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