OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC245-1 is an integrated circuit chip consisting of eight transceivers with noninverted outputs.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

Use of silicon gate technology allows the M74HC245-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS245. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state noninverted outputs have their inputs and outputs connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

When DIR is high, the A data ports will become input terminals and the B data ports will become output terminals.

When DIR is low, B will become input terminals and A will become output terminals.

When output enable OE is high, A and B will both become high-impedance state and they will be separated.

PIN CONFIGURATION (TOP VIEW)

Outline 20P4
20P2N

LOGIC DIAGRAM (EACH TRANSCEIVER)

FUNCTION TABLE (Note 1)
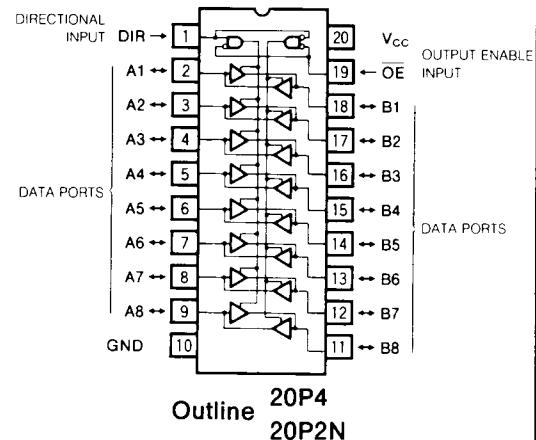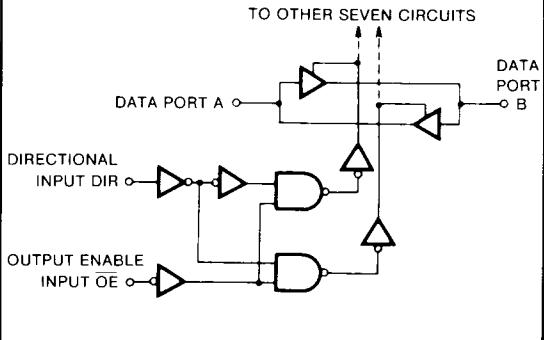
Inputs		Data ports	
OE	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1 : I : Input pin
O : Output pin
Z : High impedance (A and B are separated.)
X : Irrelevant

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ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85℃$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_I	Input voltage		$-0.5 \sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5 \sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	20	
I_O	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature		$-65 \sim +150$	℃

Note 2: M74HC245-1FP : $T_a = -40 \sim +75℃$ and $T_a = 75 \sim 85℃$ are derated at $-7mW/℃$

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85℃$)

Symbol	Parameter		Limits		Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC}=2.0V$	0		500	
		$V_{CC}=4.5V$	0		50	ns/V
		$V_{CC}=6.0V$	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃			$-40 \sim +85℃$	
			$V_{CC}(V)$	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$ $I_O=20\mu A$	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$ $I_O=20\mu A$	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I=V_{IL}$, V_{IH} $I_{OH}=-20\mu A$	2.0	1.9			1.9		V
		$I_{OH}=-20\mu A$	4.5	4.4			4.4		
		$I_{OH}=-20\mu A$	6.0	5.9			5.9		
		$I_{OH}=-24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I=V_{IH}$, V_{IL} $I_{OL}=20\mu A$	2.0			0.1		0.1	V
		$I_{OL}=20\mu A$	4.5			0.1		0.1	
		$I_{OL}=20\mu A$	6.0			0.1		0.1	
		$I_{OL}=24mA$	4.5			0.44		0.53	
I_{IH}	High-level input current	$V_I=6V$	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I=0V$	6.0			-0.1		-1.0	μA
I_{OZH}	Off-state high-level output current	$V_I=V_{IH}$, V_{IL}, $V_O=V_{CC}$	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I=V_{IH}$, V_{IL}, $V_O=GND$	6.0			-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I=V_{CC}$, GND, $I_O=0\mu A$	6.0			5.0		50.0	μA

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SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L=50pF (Note 4)			10	ns
t_{THL}					10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (A—B, B—A)				16	ns
t_{PHL}					16	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$—A, B)	C_L=5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$—A, B)	C_L=50pF (Note 4)			27	ns
t_{PZH}					27	ns
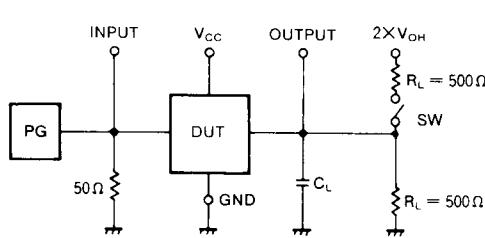
SWITCHING CHARACTERISTICS (V_{CC}=2～6V, T_a=−40～+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits					Unit
				25℃			−40～+85℃		
				Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and high-to low-level		2.0		16	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t_{THL}	output transition time		2.0		23	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level		2.0		26	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t_{PHL}	output propagation time (A—B, B—A)	C_L=50pF (Note 4)	2.0		27	85		105	ns
			4.5		10	17		21	
			6.0		8	14		18	
t_{PLZ}	Low-level and high-level		2.0		21	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t_{PHZ}	output disable time ($\overline{OE}$—A, B)		2.0		24	140		175	ns
			4.5		12	28		35	
			6.0		11	24		30	
t_{PZL}	Low-level and high-level		2.0		32	140		175	ns
			4.5		11	28		35	
			6.0		10	24		30	
t_{PZH}	output enable time ($\overline{OE}$—A, B)		2.0		33	140		175	ns
			4.5		12	28		35	
			6.0		9	24		30	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$=V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				56.3				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during operation under no-load condition is calculated using the following formula :
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$
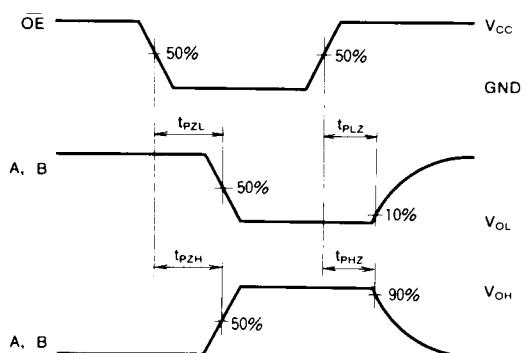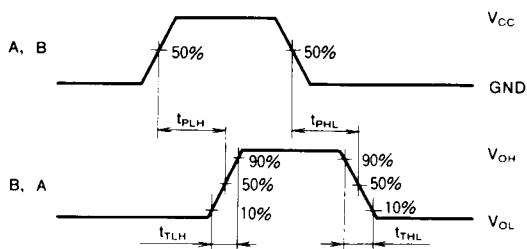
Note 4 : Test Circuit

Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

1 : The pulse generator (PG) has the following characteristics (10%～90%) : t_r=3ns, t_f=3ns
2 : The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

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TIMING DIAGRAM
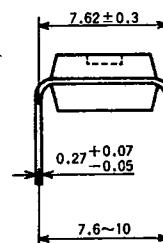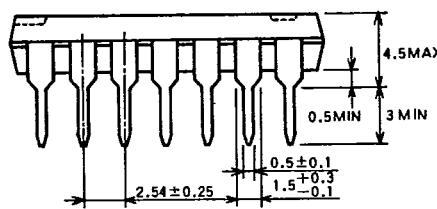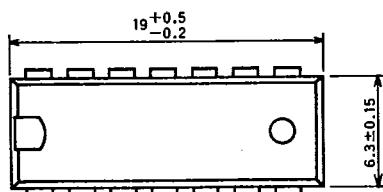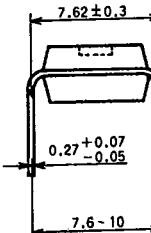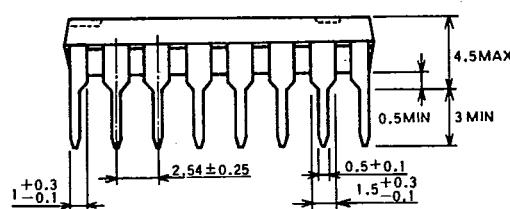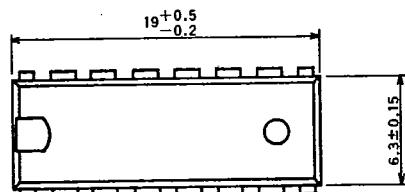
TYPE 14P4 14-PIN MOLDED PLASTIC DIP   Dimension in mm

$19^{+0.5}_{-0.2}$

6.3 ± 0.15

4.5MAX

0.5MIN   3 MIN

0.5 ± 0.1
$1.5^{+0.3}_{-0.1}$

2.54 ± 0.25

7.62 ± 0.3

$0.27^{+0.07}_{-0.05}$

$7.6 \sim 10$

TYPE 16P4 16-PIN MOLDED PLASTIC DIP   Dimension in mm

$19^{+0.5}_{-0.2}$

6.3 ± 0.15

4.5MAX

0.5MIN   3 MIN

$1^{+0.3}_{-0.1}$

2.54 ± 0.25

$0.5 + 0.1$
$1.5^{+0.3}_{-0.1}$

7.62 ± 0.3

$0.27^{+0.07}_{-0.05}$

$7.6 \sim 10$

91D D █ 6249827 0012850 5 █
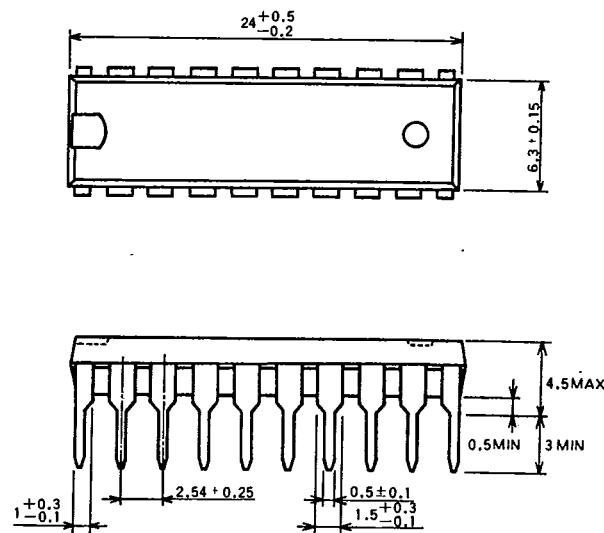
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PACKAGE OUTLINES
91D 12850   D T-90-20

6249827 MITSUBISHI (DGTL LOGIC)
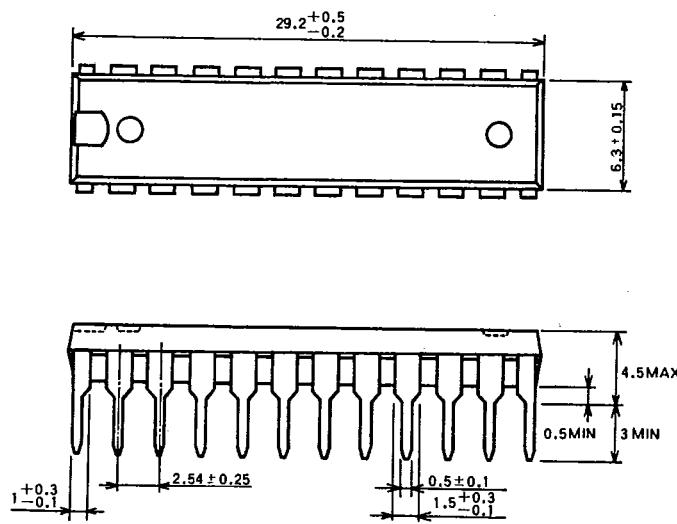
TYPE 20P4 20-PIN MOLDED PLASTIC DIP   Dimension in mm

$24^{+0.5}_{-0.2}$

6.3 ± 0.15

7.62 ± 0.3

4.5MAX

0.5MIN 3 MIN

$0.27^{+0.07}_{-0.05}$

$1^{+0.3}_{-0.1}$ 2.54 + 0.25   0.5 ± 0.1 $1.5^{+0.3}_{-0.1}$

7.6~10

TYPE 24P4D 24-PIN MOLDED PLASTIC DIP   Dimension in mm
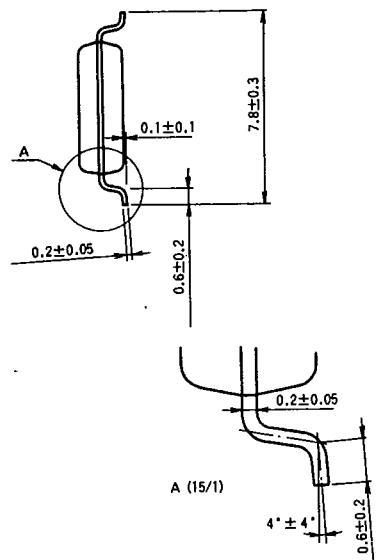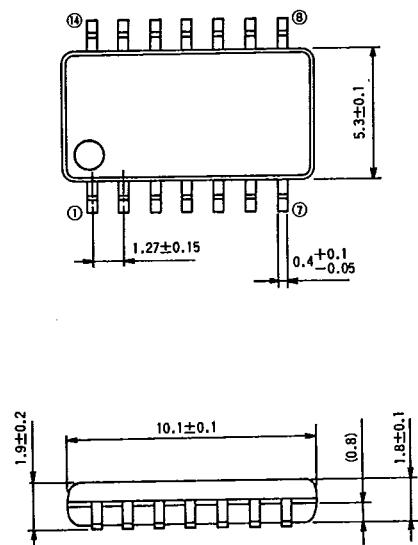
$29.2^{+0.5}_{-0.2}$

6.3 ± 0.15

7.62 ± 0.3

4.5MAX

0.5MIN 3 MIN

$0.27^{+0.07}_{-0.05}$

$1^{+0.3}_{-0.1}$ 2.54 ± 0.25   0.5 ± 0.1 $1.5^{+0.3}_{-0.1}$

7.6~10

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PACKAGE OUTLINES

91D 12851   D T-90.20

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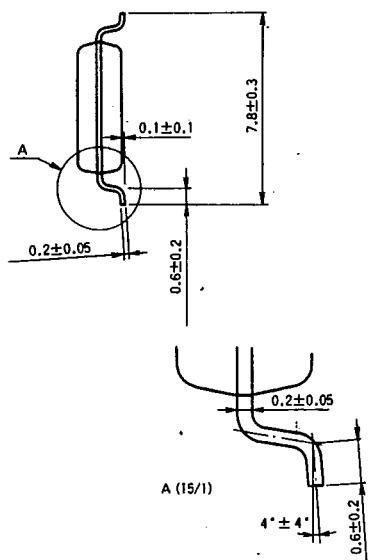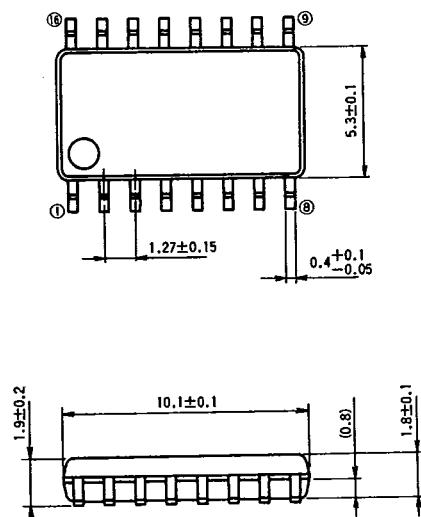
TYPE 14P2N 14PIN MOLDED PLASTIC SOP   Dimension in mm

5.3±0.1

7.8±0.3

0.1±0.1

A

0.2±0.05

0.6±0.2

1.27±0.15

0.4 +0.1 −0.05

1.9±0.2

10.1±0.1

(0.8)

1.8±0.1

0.2±0.05

A (15/1)

4°±4°

0.6±0.2
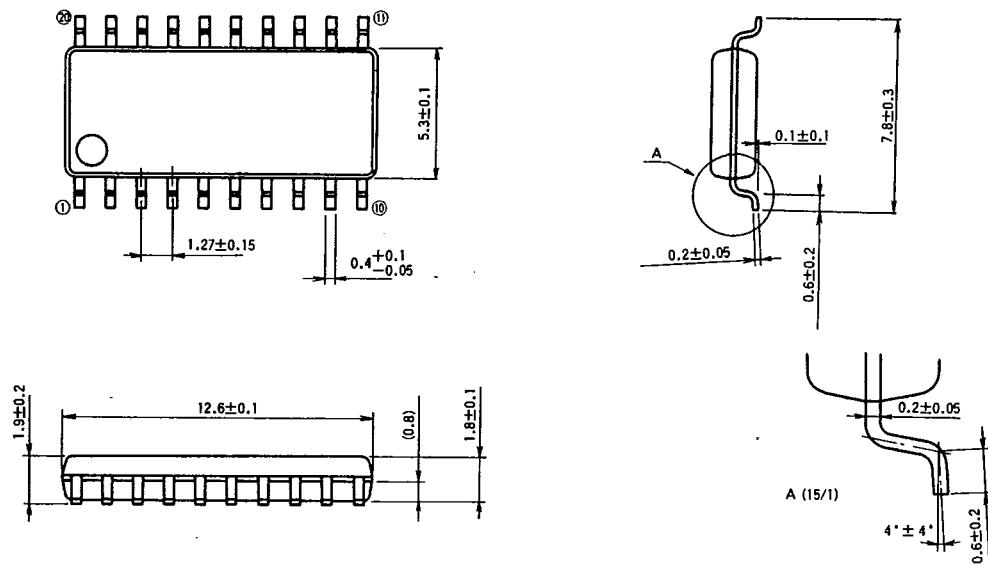
TYPE 16P2N 16PIN MOLDED PLASTIC SOP   Dimension in mm

5.3±0.1

7.8±0.3

0.1±0.1

A

0.2±0.05

0.6±0.2

1.27±0.15

0.4 +0.1 −0.05

1.9±0.2

10.1±0.1

(0.8)

1.8±0.1

0.2±0.05

A (15/1)

4°±4°

0.6±0.2

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PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)
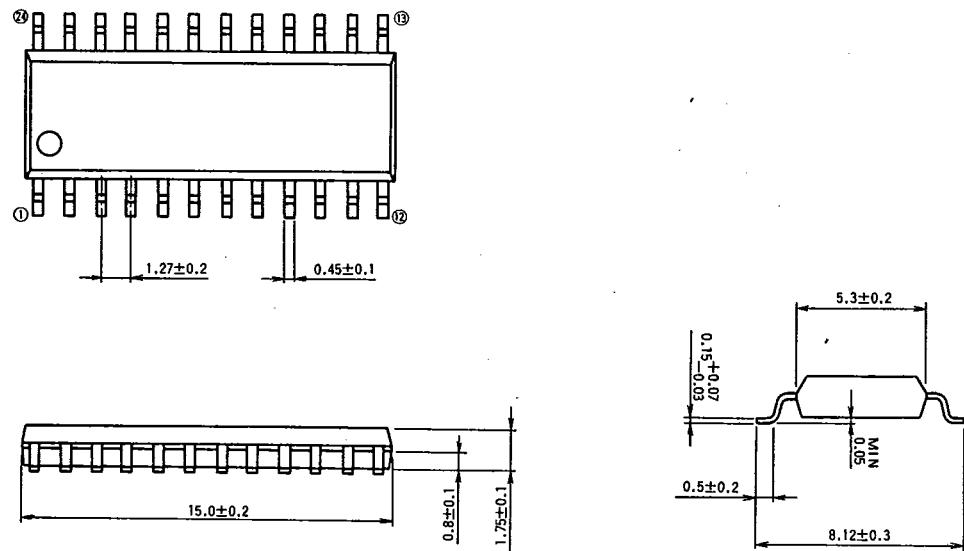
91D 12852   D . T-90-20

TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm

5.3±0.1

1.27±0.15

0.4 +0.1 −0.05

1.9±0.2

12.6±0.1

(0.8)

1.8±0.1

7.8±0.3

0.1±0.1

A

0.2±0.05

0.6±0.2

0.2±0.05

A (15/1)

4°±4°

0.6±0.2

TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

1.27±0.2

0.45±0.1

15.0±0.2

0.8±0.1

1.75±0.1

5.3±0.2

0.15+0.1 0.07−0.03

MIN 0.05

0.5±0.2

8.12±0.3

2935   G-04

1-54
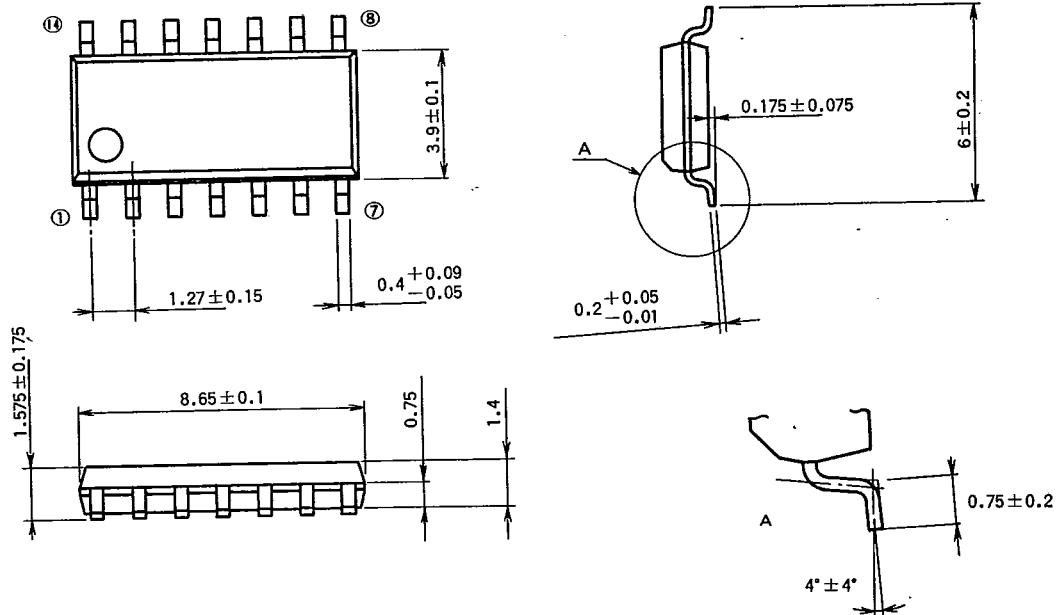
◆ MITSUBISHI
ELECTRIC
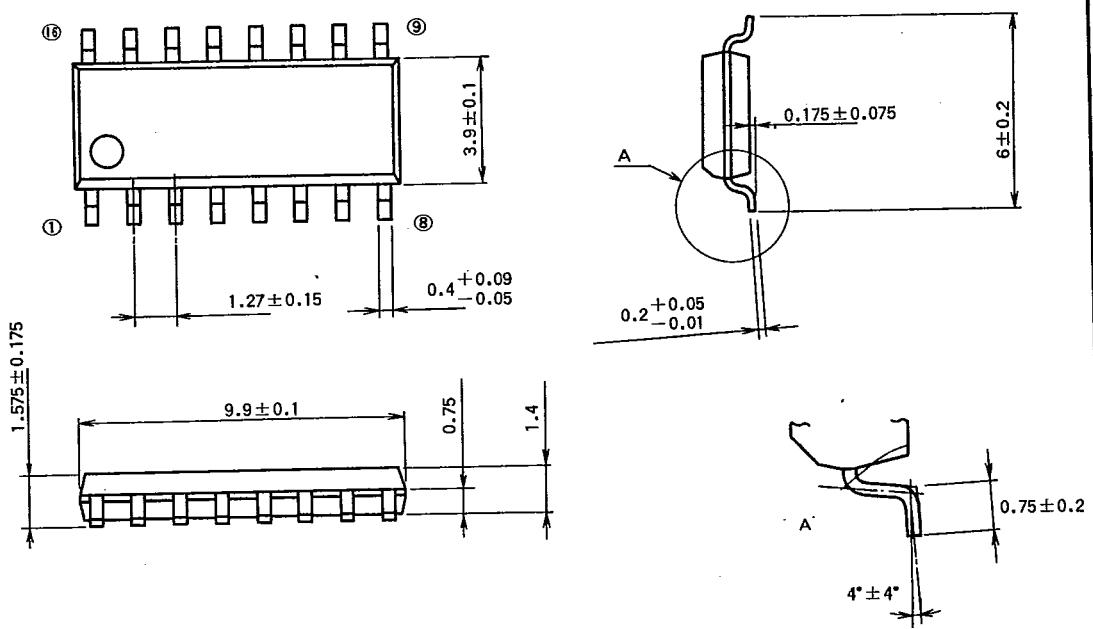
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm

3.9±0.1

6±0.2

0.175±0.075

A

$0.2^{+0.05}_{-0.01}$

1.27±0.15 $0.4^{+0.09}_{-0.05}$

1.575±0.175

8.65±0.1   0.75   1.4

A

0.75±0.2

4°±4°

TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm

3.9±0.1

6±0.2

0.175±0.075

A

$0.2^{+0.05}_{-0.01}$

1.27±0.15 $0.4^{+0.09}_{-0.05}$

1.575±0.175

9.9±0.1   0.75   1.4

A

0.75±0.2

4°±4°

MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12854   D T-90-20

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm

⑳ ⑪

① ⑩

7.5±0.1

1.27±0.15   0.4 +0.09 -0.05

10.3±0.3

A   0.2±0.1

0.25 +0.07 -0.02

2.5±0.15

12.8±0.1   1.025   2.3

0.8±0.2

4°±4°

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