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## LM6161/LM6261/LM6361 High Speed Operational Amplifier

### General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/ $\mu$ s and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

### Features

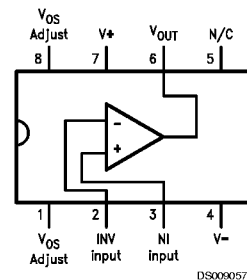
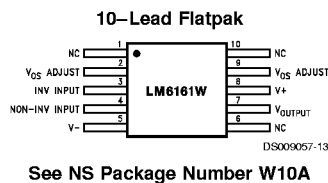
- High slew rate 300 V/ $\mu$ s

- High unity gain freq 50 MHz
- Low supply current 5 mA
- Fast settling 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase 0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

### Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

### Connection Diagrams



See NS Package Number J08A,  
N08E or M08A

Temperature Range			Package	NSC Drawing
Military -55°C ≤ T <sub>A</sub> ≤ +125°C	Industrial -25°C ≤ T <sub>A</sub> ≤ +85°C	Commercial 0°C ≤ T <sub>A</sub> ≤ +70°C		
	LM6261N	LM6361N	8-Pin Molded DIP	N08E
LM6161J/883 5962-8962101PA		LM6361J	8-Pin Ceramic DIP	J08A
	LM6261M	LM6361M	8-Pin Molded Surface Mt.	M08A
LM6161WG/883 5962-8962101XA			10-Lead Ceramic SOIC	WG10A
LM6161W/883 5962-8962101HA			10-Pin Ceramic Flatpak	W10A

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## Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V^+ - V^-$ )	36V
Differential Input Voltage (Note 8)	$\pm 8V$
Common-Mode Voltage Range (Note 10)	$(V^+ - 0.7V)$ to $(V^- + 0.7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J) Soldering (10 sec.)	260°C
Small Outline Package (M) Vapor Phase (60 sec.) Infrared (15 sec.)	215°C 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	-65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 6, 7)	$\pm 700V$

## Operating Ratings (Note 12)

Temperature Range (Note 2)	
LM6161	$-55^\circ C \leq T_J \leq +125^\circ C$
LM6261	$-25^\circ C \leq T_J \leq +85^\circ C$
LM6361	$0^\circ C \leq T_J \leq +70^\circ C$
Supply Voltage Range	4.75V to 32V

## DC Electrical Characteristics

The following specifications apply for Supply Voltage =  $\pm 15V$ ,  $V_{CM} = 0$ ,  $R_L \geq 100\text{ k}\Omega$  and  $R_S = 50\Omega$  unless otherwise noted. **Boldface** limits apply for  $T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_J = 25^\circ C$ .

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
$V_{OS}$	Input Offset Voltage		5	7 <b>10</b>	7 <b>9</b>	20 <b>22</b>	mV Max
$V_{OS}$ Drift	Input Offset Voltage Average Drift		10				$\mu V/^\circ C$
$I_b$	Input Bias Current		2	3 <b>6</b>	3 <b>5</b>	5 <b>6</b>	$\mu A$ Max
$I_{OS}$	Input Offset Current		150	350 <b>800</b>	350 <b>600</b>	1500 <b>1900</b>	nA Max
$I_{OS}$ Drift	Input Offset Current Average Drift		0.4				$nA/^\circ C$
$R_{IN}$	Input Resistance	Differential	325				k $\Omega$
$C_{IN}$	Input Capacitance	$A_V = +1$ @ 10 MHz	1.5				pF
$A_{VOL}$	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$ , $R_L = 2\text{ k}\Omega$ (Note 9)	750	550 <b>300</b>	550 <b>400</b>	400 <b>350</b>	V/V Min
		$R_L = 10\text{ k}\Omega$ (Note 9)	2900				V/V
$V_{CM}$	Input Common-Mode Voltage Range	Supply = $\pm 15V$	+14.0 -13.2	+13.9 <b>+13.8</b> -12.9 <b>-12.7</b>	+13.9 <b>+13.8</b> -12.9 <b>-12.7</b>	+13.8 <b>+13.7</b> -12.8 <b>-12.7</b>	Volts Min Volts Min
		Supply = +5V (Note 4)	4.0 1.8	3.9 <b>3.8</b> 2.0 <b>2.2</b>	3.9 <b>3.8</b> 2.0 <b>2.2</b>	3.8 <b>3.7</b> 2.1 <b>2.2</b>	Volts Min Volts Max
CMRR	Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	94	80 <b>74</b>	80 <b>76</b>	72 <b>70</b>	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \leq V^\pm \leq \pm 16V$	90	80 <b>74</b>	80 <b>76</b>	72 <b>70</b>	dB Min

## DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage =  $\pm 15\text{V}$ ,  $V_{CM} = 0$ ,  $R_L \geq 100\text{ k}\Omega$  and  $R_S = 50\Omega$  unless otherwise noted. **Boldface** limits apply for  $T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
$V_O$	Output Voltage Swing	Supply = $\pm 15\text{V}$ and $R_L = 2\text{ k}\Omega$	+14.2	+13.5 <b>+13.3</b>	+13.5 <b>+13.3</b>	+13.4 <b>+13.3</b>	Volts Min
			-13.4	-13.0 <b>-12.7</b>	-13.0 <b>-12.8</b>	-12.9 <b>-12.8</b>	Volts Min
		Supply = +5V and $R_L = 2\text{ k}\Omega$ (Note 4)	4.2	3.5 <b>3.3</b>	3.5 <b>3.3</b>	3.4 <b>3.3</b>	Volts Min
			1.3	1.7 <b>2.0</b>	1.7 <b>1.9</b>	1.8 <b>1.9</b>	Volts Max
	Output Short Circuit Current	Source	65	30 <b>20</b>	30 <b>25</b>	30 <b>25</b>	mA Min
		Sink	65	30 <b>20</b>	30 <b>25</b>	30 <b>25</b>	mA Min
$I_S$	Supply Current		5.0	6.5 <b>6.8</b>	6.5 <b>6.7</b>	6.8 <b>6.9</b>	mA Max

## AC Electrical Characteristics

The following specifications apply for Supply Voltage =  $\pm 15\text{V}$ ,  $V_{CM} = 0$ ,  $R_L \geq 100\text{ k}\Omega$  and  $R_S = 50\Omega$  unless otherwise noted. **Boldface** limits apply for  $T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
GBW	Gain-Bandwidth Product	@ $f = 20\text{ MHz}$	50	40 <b>30</b>	40 <b>35</b>	35 <b>32</b>	MHz Min
		Supply = $\pm 5\text{V}$	35				MHz
SR	Slew Rate	$A_V = +1$ (Note 8)	300	200 <b>180</b>	200 <b>180</b>	200 <b>180</b>	V/ $\mu\text{s}$ Min
		Supply = $\pm 5\text{V}$ (Note 8)	200				V/ $\mu\text{s}$
PBW	Power Bandwidth	$V_{OUT} = 20 V_{PP}$	4.5				MHz
$t_S$	Settling Time	10V Step to 0.1% $A_V = -1$ , $R_L = 2\text{ k}\Omega$	120				ns
$\phi_m$	Phase Margin		45				Deg
$A_D$	Differential Gain	NTSC, $A_V = +4$	<0.1				%
$\phi_D$	Differential Phase	NTSC, $A_V = +4$	0.1				Deg
$e_{np-p}$	Input Noise Voltage	$f = 10\text{ kHz}$	15				nV/ $\sqrt{\text{Hz}}$
$i_{np-p}$	Input Noise Current	$f = 10\text{ kHz}$	1.5				pA/ $\sqrt{\text{Hz}}$

**Note 1:** Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ .

**Note 2:** The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is  $105^\circ\text{C/W}$ , the molded plastic SO (M) package is  $155^\circ\text{C/W}$ , and the cerdip (J) package is  $125^\circ\text{C/W}$ . All numbers apply for packages soldered directly into a printed circuit board.

**Note 3:** Limits are guaranteed by testing or correlation.

**Note 4:** For single supply operation, the following conditions apply:  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 2.5\text{V}$ ,  $V_{OUT} = 2.5\text{V}$ . Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 ( $V^-$ ) to realize maximum output swing. This connection will degrade  $V_{OS}$ ,  $V_{OS}$  Drift, and Input Voltage Noise.

**Note 5:**  $C_L \leq 5\text{ pF}$ .

**Note 6:** In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

## AC Electrical Characteristics (Continued)

**Note 7:** The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

**Note 8:**  $V_{IN} = 8V$  step. For supply =  $\pm 5V$ ,  $V_{IN} = 5V$  step.

**Note 9:** Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

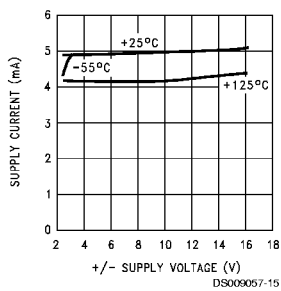
**Note 10:** The voltage between  $V^+$  and either input pin must not exceed 36V.

**Note 11:** A military RETS electrical test specification is available on request. At the time of printing, the RETS6161X specs complied with all **Boldface** limits in this column.

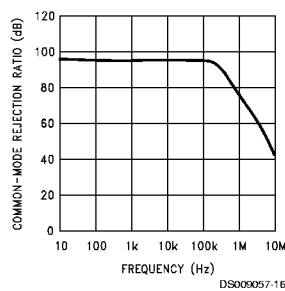
**Note 12:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

## Typical Performance Characteristics ( $R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$ unless otherwise specified)

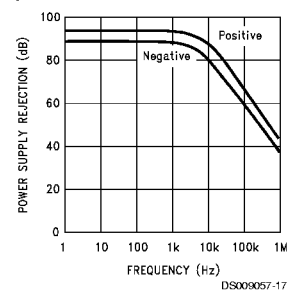
**Supply Current vs Supply Voltage**



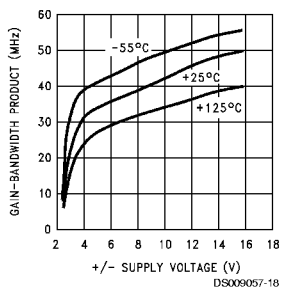
**Common-Mode Rejection Ratio**



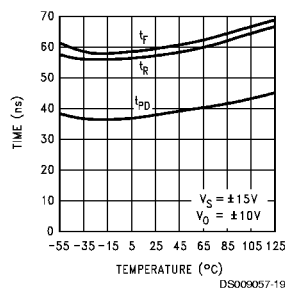
**Power Supply Rejection Ratio**



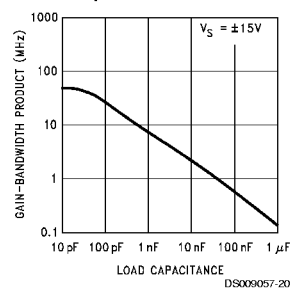
**Gain-Bandwidth Product**



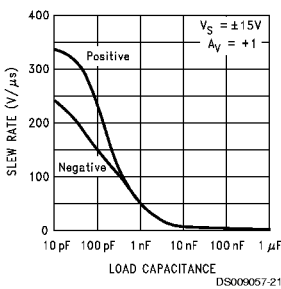
**Propagation Delay Rise and Fall Times**



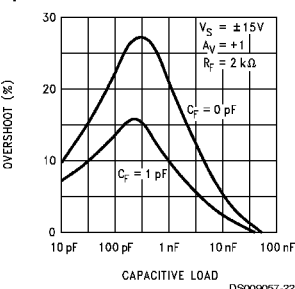
**Gain-Bandwidth Product vs Load Capacitance**



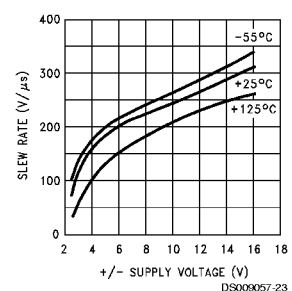
**Slew Rate vs Load Capacitance**



**Overshoot vs Capacitive Load**

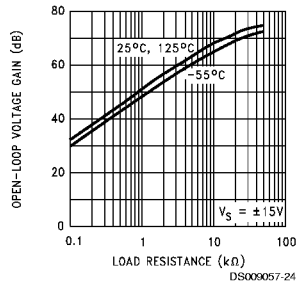


**Slew Rate**

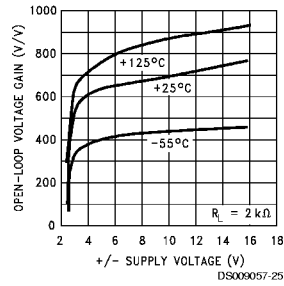


**Typical Performance Characteristics** ( $R_L = 10\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified) (Continued)

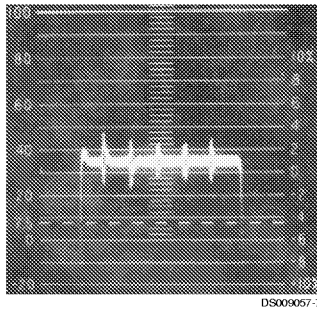
**Voltage Gain vs Load Resistance**



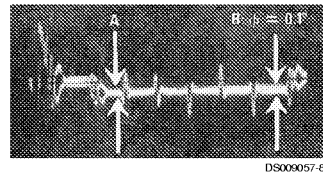
**Gain vs Supply Voltage**



**Differential Gain (Note 13)**

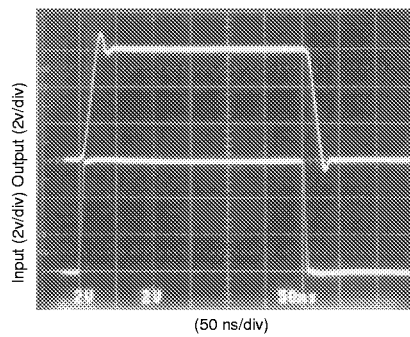


**Differential Phase (Note 13)**



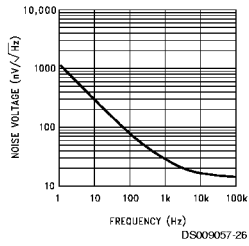
**Note 13:** Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

**Step Response;  $A_v = +1$**

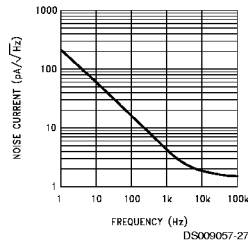


**Typical Performance Characteristics** ( $R_L = 10\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified) (Continued)

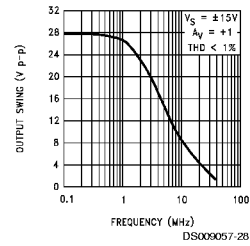
**Input Noise Voltage**



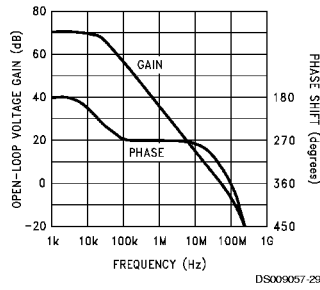
**Input Noise Current**



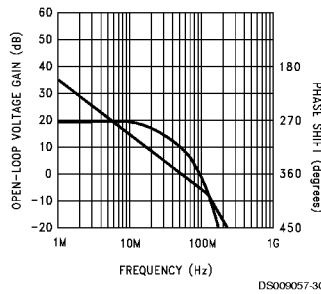
**Power Bandwidth**



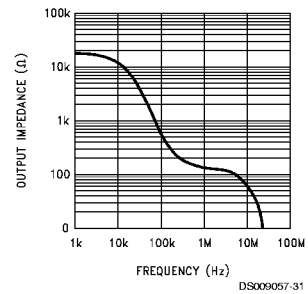
**Open-Loop Frequency Response**



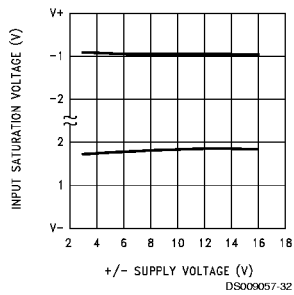
**Open-Loop Frequency Response**



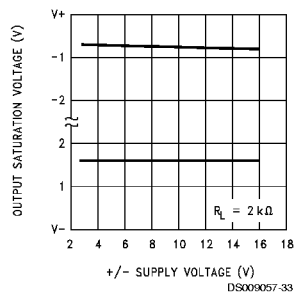
**Output Impedance (Open-Loop)**



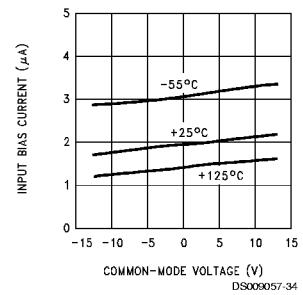
**Common-Mode Input Saturation Voltage**



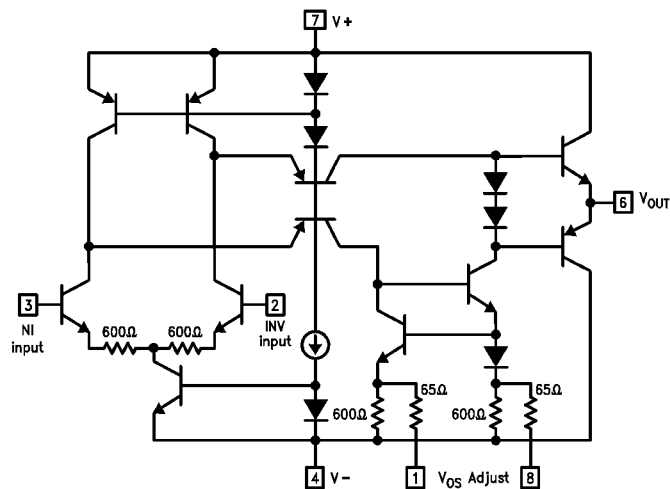
**Output Saturation Voltage**



**Bias Current vs Common-Mode Voltage**



## Simplified Schematic



DS000057-3

## Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced  $A_{VOL}$  is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, how-

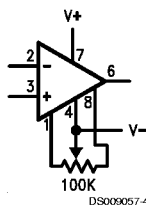
ever, improve the stability and transient response and is recommended for every design. 0.01  $\mu$ F to 0.1  $\mu$ F ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2  $\mu$ F to 10  $\mu$ F of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

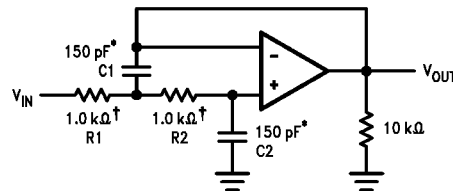
## Typical Applications

### Offset Voltage Adjustment



DS000057-4

### 1 MHz Low-Pass Filter



DS000057-10

†1% tolerance

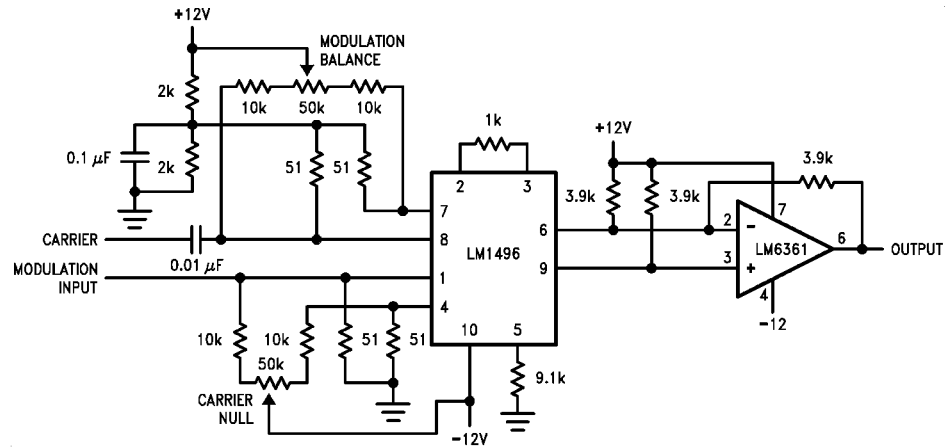
\*Matching determines filter precision

$$f_c = (2\pi \sqrt{R1 R2 C1 C2})^{-1}$$



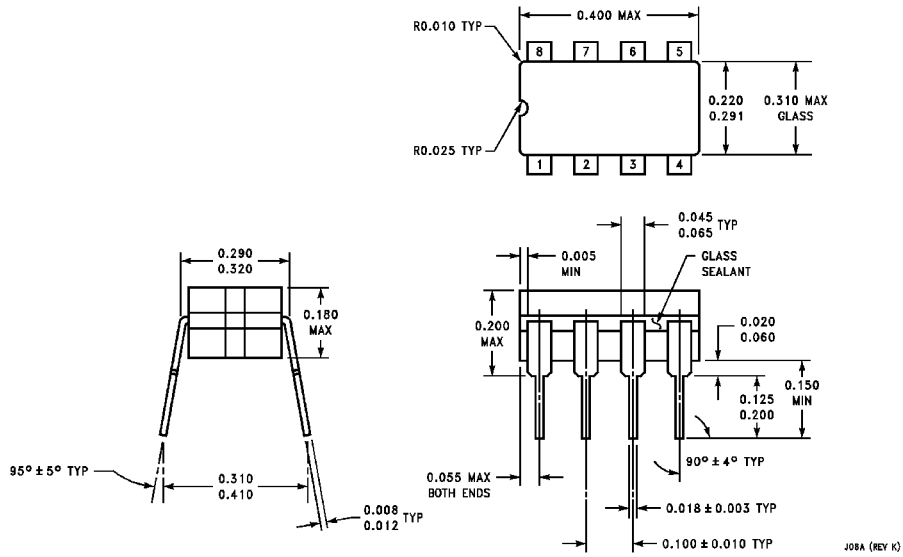
## Typical Applications (Continued)

### Modulator with Differential-to-Single-Ended Converter

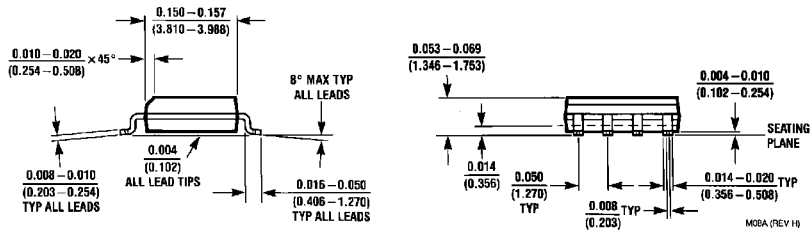
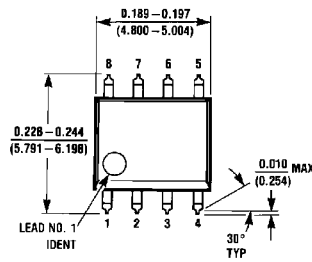


DS009057-11

**Physical Dimensions** inches (millimeters) unless otherwise noted

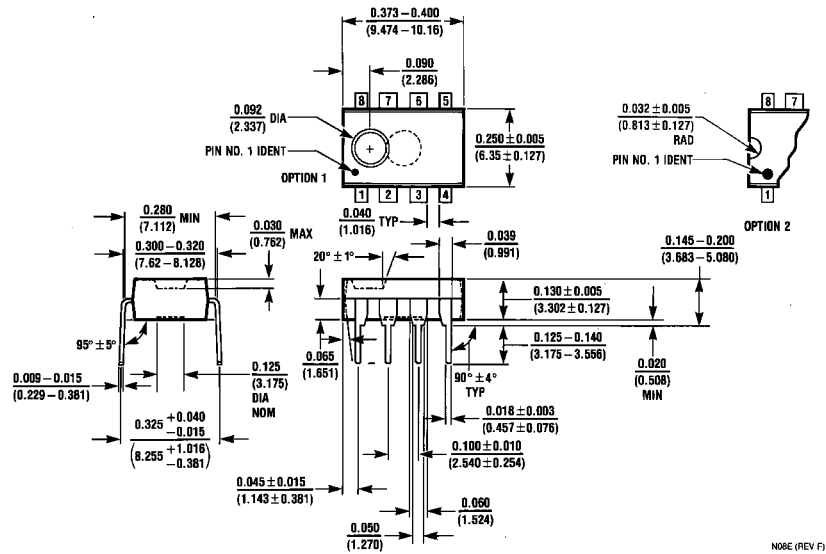


**Ceramic Dual-In-Line Package (J)**  
**Order Number LM6161J/883**  
**NS Package Number J08A**

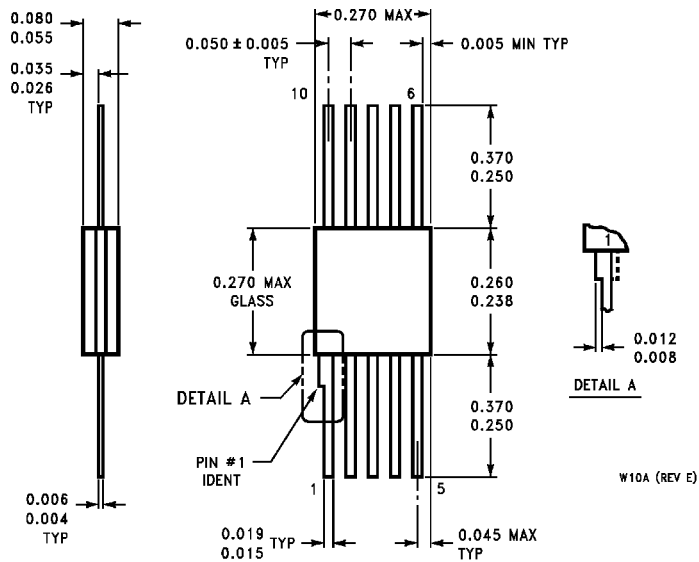


**Molded Package SO (M)**  
**Order Number LM6261M or LM6361M**  
**NS Package Number M08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number LM6261N or LM6361N**  
**NS Package Number N08E**



**10-Pin Ceramic Flatpak**  
**Order Number LM6161W/883**  
**NS Package Number W10A**