The documentation and process conversion measures necessary to comply with this revision shall be completed by 24 February 2005.

INCH-POUND

MIL-PRF-19500/406F
24 November 2004
SUPERSEDING
MIL-PRF-19500/406E
8 September 2003

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICES, DIODE, SILICON, VOLTAGE REGULATOR, TYPES 1N4460, 1N4460C, 1N4460D THROUGH 1N4496, 1N4496C, 1N4496D, AND 1N6485, 1N6485C, 1N6485D THROUGH 1N6491, 1N6491C, 1N6491D, 1N4460US, 1N4460CUS, 1N4460DUS THROUGH 1N4496US, 1N4496CUS, 1N4496DUS, AND 1N6485US, 1N6485CUS, 1N6485DUS THROUGH 1N6491US, 1N6491CUS, 1N6491DUS, PLUS C AND D TOLERANCE SUFFIX; JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for microminiature 1.5 watt silicon, low leakage, voltage regulator diodes with tolerances of 5 percent, 2 percent, and 1 percent. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500.

* 1.2 Physical dimensions. See figure 1 (similar to DO-41), and figure 2 (surface mount).

* 1.3 Maximum ratings. Maximum ratings are as shown in maximum and primary test ratings (see 3.11) herein and as follows: P_T = 1.5 W (derate at 10 mW/°C above T_A = +25°C); -55°C < T_J < +175°C; -65°C < T_{STG} < +175°C, derating: See figures 3 and 4 herein.

1.4 Primary electrical characteristics. Primary electrical characteristics are as shown in maximum and primary test ratings (see 3.11) and as follows:

3.3 V dc ≤ V_Z ≤ 200 V dc (nominal).

a. 1N4460D through 1N4496D and 1N6485D through 1N6491D are 1 percent voltage tolerance.

b. 1N4460C through 1N4496C and 1N6485C through 1N6491C are 2 percent voltage tolerance.

c. 1N4460 through 1N4496 and 1N6485 through 1N6491 are 5 percent voltage tolerance.

$R_{\theta JL}$ = 42°C/W (max) at L = .375 inch (9.52 mm) (nonsurface mount).
$R_{\theta JEC}$ = 20°C/W (max) (surface mount).

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500, and as follows:

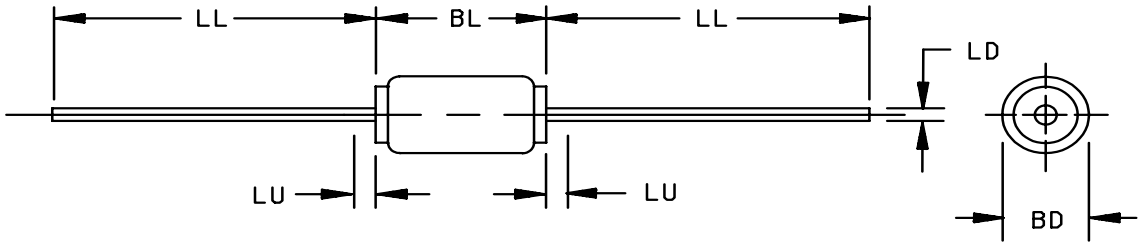
EC ..... End-cap.
US ..... Surface mount case outline, square end cap.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 and 2 herein.

3.4.1 Diode construction. These devices shall be constructed utilizing the requirements of MIL-PRF-19500 and as follows.

3.4.1.1 Metallurgical bond for diodes with V_Z greater than 6.8 V dc. Category I metallurgical bonds for diodes with V_Z greater than 6.8 V dc as defined in MIL-PRF-19500 shall be utilized.

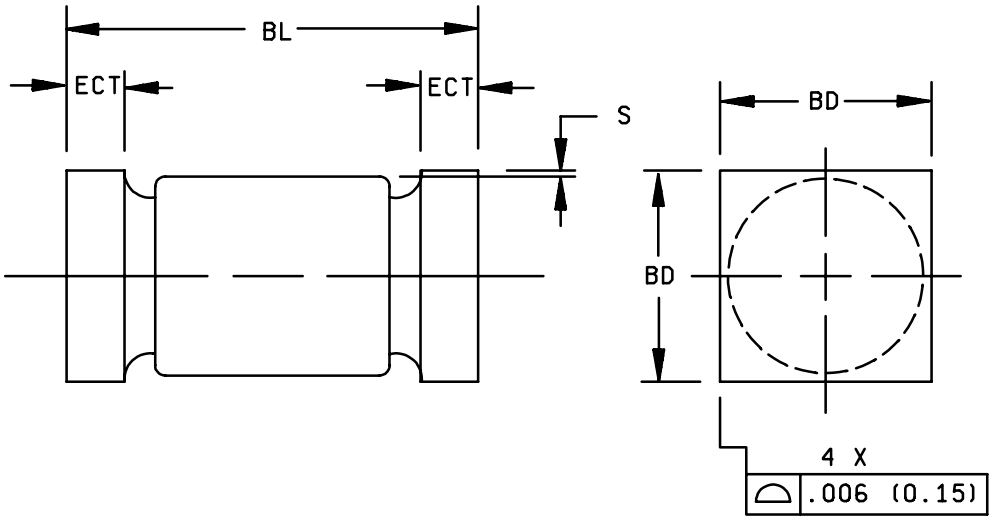
3.4.1.2 Metallurgical bond for diodes with V_Z less than or equal to 6.8 V dc. Category I, or category III metallurgical bonds as defined in MIL-PRF-19500.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.106	.160	2.69	4.06	3
BD	.060	.085	1.52	2.16	3
LL	.800	1.300	20.32	33.02	
LD	.028	.032	0.71	0.81	
LU		.050		1.27	4

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Package contour optional with BD and length BL. Heat slugs, if any, shall be included within this cylinder but shall not be subject to minimum limit of BD.
4. The specified lead diameters apply in the zone between .050 inch (1.27 mm) from the diode body and the end of the lead.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions of nonsurface mount device (similar to DO-41).



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.168	.200	4.28	5.08
ECT	.019	.028	0.48	0.71
S	.003		0.08	
BD	.091	.103	2.31	2.62

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions of surface mount device, US(D5A).

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.5.1 Marking of US version devices. For US version devices only, all marking may be omitted from the device except for the cathode marking. All marking which is omitted from the body of the device shall appear on the label of the initial container.

3.6 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. When solder alloy is used for lead finish the maximum lead temperature shall be 175°C max. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.7 Polarity. The polarity of all types shall be indicated with a contrasting color band to denote the cathode end. Alternatively, for US suffix devices, a minimum of three contrasting color dots spaced around the periphery on the cathode end may be used.

3.8 Selection of tighter tolerance devices. The C and D suffix devices shall be selected from JAN, JANTX, JANTXV, or JANS devices, which have successfully completed all applicable screening, and groups A, B, and C testing as ±5 percent tolerance devices. All sublots of C and D suffix devices shall pass table I, subgroup 2, at tightened tolerances. Tighter tolerances for mounting clip temperature shall be maintained for reference purposes to establish correlation. For C and D tolerance levels, T_L = 25°C +1°C, -3°C at .375 inch (9.53 mm) from body or equivalent.

3.9 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, table I, and table II herein.

3.10 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.11 Maximum and primary test ratings. Maximum and primary test ratings for voltage regulator diodes are specified in table III herein.

3.12 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.1.1 Lot accumulation. Lot accumulation period shall be 3 months in lieu of 6 weeks.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein. Supplier imposed requirements shall be documented in the QM plan and must be submitted to the qualifying activity for approval. Radiation characterization may be submitted in the QM plan at the option of the manufacturer.

4.2.1 Group E qualification. Group E qualification shall be performed herein for qualification or requalification only. In case qualification was awarded to a prior revision of the associated specification that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot to this revision to maintain qualification.

* 4.3 Screening (JANS, JANTXV and JANTX levels only). Screening shall be in accordance with appendix E, table IV of MIL-PRF-19500, and as specified herein. Specified electrical measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurements	
	JANS level	JANTX and JANTXV levels
1a	Required	Not required
1b	Required	Required (JANTXV only)
2	Not required	Not required
3a 3b (1) 3c	Required Not applicable Thermal impedance, see 4.3.2	Required Not applicable Thermal impedance, see 4.3.2
4	Not applicable	Not applicable
5	Not applicable	Not applicable
6	Not applicable	Not applicable
7	Optional	Optional
8	Required	Not required
9	I_{R1} and V_Z (1N4466 thru 1N4496 only)	Not applicable
10	Required for device > 10 V dc.	Not applicable.
11	I_{R1} and V_Z $\Delta I_{R1} \leq \pm 100$ percent of initial reading or 50 nA dc, whichever is greater. $\Delta V_Z \leq \pm 2$ percent of initial reading. (2)	I_{R1} and V_Z
12	Required see 4.3.3	Required see 4.3.3
(2) (3) 13	Required Scope display see 4.5.8. Subgroups 2 and 3 of table I herein; ΔI_{R1} (max) $\leq \pm 100$ percent of initial reading or 50 nA, whichever is greater; $\Delta V_Z \leq \pm 2$ percent of initial reading.	Required Subgroup 2 of table I herein; ΔI_{R1} (max) $\leq \pm 100$ percent of initial reading or 50 nA, whichever is greater; $\Delta V_Z \leq \pm 2$ percent of initial reading.
14a	Not applicable	Not applicable
(4) 14b	Required	Required
15	Required	Not required
16	Required	Not required

(1) This test shall be performed anytime after screen 3.
(2) Delta limits applicable to 1N4466 thru 1N4496 only.
(3) Thermal impedance not applicable, if already performed 100 percent.
(4) For clear glass diodes, the hermetic seal (gross leak) may be performed at any time after temperature cycling.

* 4.3.2 Thermal impedance ($Z_{\theta JX}$ measurements) The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3101 of MIL-STD-750. The maximum screen limit shall be developed by the supplier using statistical methods and it shall not exceed the value specified in table I, subgroup 2 herein.

4.3.3 Power burn-in conditions. Power burn-in conditions are as follows: The test current I_Z shall be adjusted to produce a junction temperature of +125°C minimum and I_Z minimum shall be equal to 50 percent of column 8 of table III. Use method 3100 of MIL-STD-750 to measure T_J (see 4.5.7).

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be in accordance with MIL-PRF-19500 and table I herein. Thermal impedance conditions are as follows:

a. I_M measurement current..... 1 mA to 10 mA.

b. I_H forward heating current ..... 3 A to 10 A.

c. t_H heating time ..... 10 ms.

d. t_{MD} measurement delay time..... 100 μs maximum.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E table VIa (JANS) and VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500. Electrical measurements (end-points) shall be in accordance with the applicable inspections of table I, subgroup 2 herein. $Z_{\theta JX}$ is an end-point for these subgroups: B2 and B3 (JAN, JANTX and JANTXV product levels only).

* 4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1056	0°C to +100°C, 25 cycles, n = 22 c = 0.
B3	1051	-55°C to +175°C, 100 cycles, n = 22 c = 0.
B4	1037	I_Z = column 8 of table III at T_A = room ambient as defined in the general requirements of paragraph 4.5 of MIL-STD-750; for 2,000 cycles.
B5	1027	I_Z = 40 percent of column 8 of table III minimum; adjust T_A and or I_Z to achieve T_J minimum. Temporary leads may be added for surface mount devices.
		Option 1: T_A = +100°C max; T_J = +275°C minimum; t = 96 hours. n = 22, c = 0.
	or	Option 2: T_A = +30°C max; T_J = +175°C minimum; t = 1,000 hours, n = 45, c = 0.

* 4.4.2.2 Group B inspection, table VIb (JAN, JANTX and JANTXV of MIL-PRF-19500).

Subgroup	Method	Condition
B2	1056	0°C to +100°C, 10 cycles, n = 22 c = 0.
B2	1051	-55°C to +175°C, 25, cycles, n = 22 c = 0.
B2	1071	Test condition E only NOTE: For non-transparent devices, hermetic seal may be performed after electrical measurements.
B3	1027	I_Z(min) = 50 percent of column 8 of table III minimum. Adjust I_Z or T_A to achieve T_J = 150°C min (see 4.5.7).

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E table VII of MIL-PRF-19500 and herein. Electrical measurements (end-points) shall be in accordance with the applicable inspections of table I, subgroup 2 herein. $Z_{\theta JX}$ is an endpoint for these subgroups: C2 and C6 (JAN, JANTX and JANTXV product levels only).

* 4.4.3.1 Group C inspection, table VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	1056	0°C to +100°C, 15 cycles, n = 22 c = 0.
C2	1051	-55°C to +175°C, 25 cycles, n = 22 c = 0.
C2	2036	Tension - test condition A; 10 lbs; t = 15 s ±3 s. Lead fatigue - Test condition E. NOTE: Not applicable to US versions.
C2	1071	Test condition E only. NOTE: For non-transparent devices, hermetic seal may be performed after electrical measurements.
C5	3101 or 4081	See 4.5.6.
C6	1027	I_Z(min) = 50 percent of column 8 of table III minimum. Adjust I_Z or T_A to achieve T_J = 150°C min (see 4.5.7).
C7		Not applicable.
C8	4071	Temperature coefficient for JAN, JANTX and JANTXV only; I_Z = column 5 of table III; T_{A1} = +25°C ±5°C; T_{A2} = +125°C ±5°C; limit = column 14 of table III (see 4.5.3).

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Surge current (I_{ZSM}). The peak currents specified in column 10 of table III shall be applied in the reverse direction and shall be superimposed on the current (I_Z = column 5 of table III) a total of five surges at 1 minute intervals. Each individual surge shall be at one-half square wave pulse of 8.3 millisecond duration or an equivalent sine wave with the same effective (rms) current.

* 4.5.2 Voltage regulation (V_Z(reg)). A current of 10 percent of I_Z (column 8 of table III) shall be maintained until thermal equilibrium is attained and the V_Z shall be noted. The current shall then be increased to a level of 50 percent of I_Z (column 8 of table III) and maintained at this level until thermal equilibrium is attained at which time the voltage change shall not exceed column 9 of table III. For this test, the diode shall be suspended by its leads (nonsurface mount) with mounting clips whose inside edge is located at .375 ± .010 inch (9.53 ±0.25 mm) from the body and the lead temperature at inside edge of the mounting clips shall be maintained at a temperature between +23°C and +33°C. For surface mount packages, the diode shall be suspended by the end-caps with the temperature of the end-caps being maintained between +23°C and +33°C. This measurement may be performed after a shorter time interval following application of the test current than that which provides thermal equilibrium if correlation can be established to the satisfaction of the qualifying activity.

4.5.3 Temperature coefficient of regulator voltage (α_{VZ}). The device shall be temperature stabilized with current applied prior to reading regulator voltage at the specified ambient temperature.

* 4.5.4 Regulator voltage. The test current (column 5 of table III) shall be applied until thermal equilibrium is attained prior to reading the regulator voltage. For this test, the diode shall be suspended by its leads (non-surface mount) with mounting clips whose inside edge is located at .375 ± .010 inch (9.53 ±0.25 mm) from the body and the lead temperature at inside edge of the mounting clips shall be maintained at a temperature of +23°C to +33°C. For surface mount diodes, the diode shall be suspended by the end-caps with the temperature of the end-caps being maintained at +23°C to +33°C. This measurement may be performed after a shorter time following application of the test current than that which provides thermal equilibrium if correlation to stabilized readings can be established to the satisfaction of the qualifying activity.

4.5.5 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL-STD-750.

4.5.6 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with test method 3101 of MIL-STD-750. $R_{\theta JL}$ = 42° C/W maximum at L = .375 inch (9.53 mm). $R_{\theta JEC}$ = 20°C/W maximum for US types. The following test conditions shall apply:

a. I_H = 2.0 A dc minimum.

b. I_M = 1 to 10 mA.

c. t_{MD} = 100 μs maximum.

d. t_H = thermal equilibrium.

The device shall be allowed to reach thermal equilibrium at current I_H before the measurement shall be made.

Lead spacing: LS = .375 inches (9.53 mm) for leaded devices as defined on figure 5.
LS = 0 (end-cap mount) for US devices.

* 4.5.7 Free air burn-in. Deliberate heat sinking, baffles to create an oven, forced air-cooling or heating is prohibited unless otherwise approved by the qualifying activity. The use of a current limiting or ballast resistor is permitted provided that each DUT still sees the full P_t (minimum) and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period. T_J = 125°C minimum for screening and T_J = 150°C for 4.4.2 and 4.4.3 life tests.

4.5.8 Scope display evaluation. Scope display evaluation shall be sharp and stable in accordance with method 4023 of MIL-STD-750. Scope display may be performed on ATE (automatic test equipment) for screening only, with the approval of the qualifying activity. Scope display in table I, subgroup 4 shall be performed on a scope. The reverse current (I_{BR}) over the knee shall be 500 μA peak.

4.5.8.1 Scope display option. At the suppliers option, 100-percent scope display evaluation may be discontinued after three consecutive lots are 100-percent tested with zero failures. Any table I failure shall require 100-percent scope display to be reinvoked.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits 2/		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance	3101	Category I bond Category III bond (See 4.4.1)	$Z_{\theta JX}$		4.5 7.5	°C/W °C/W
Forward voltage	4011	I_F = 200 mA dc	V_{F1}		1.0	V dc
Forward voltage	4011	I_F = 1 A dc	V_{F2}		1.5	V dc
Reverse current leakage	4016	DC method; V_R = column 11 of table III	I_{R1}		Column 12	µA dc
Regulator voltage	4022	I_Z = column 5 of table III (see 4.5.4)	V_Z	Column 3 -5, -2, -1 percent	Column 4 +5, +2, +1 percent	V dc
Subgroup 3						
High temperature operation		T_A = +150°C				
Reverse current leakage	4016	DC method; V_R = column 11 of table III	I_{R2}		Column 15	µA dc
Subgroup 4						
Small-signal reverse breakdown impedance	4051	I_Z = column 5 of table III I_{sig} = 10 percent I_Z	Z_Z		Column 6	ohms
Knee impedance	4051	I_{ZK} = column 14 of table III I_{sig} = 10 percent I_{ZK}	Z_{ZK}		Column 7	ohms
Scope display evaluation	4023	See 4.5.8				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits 2/		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	I_{ZSM} = column 10 of table III at T_A +25°C (see 4.5.1).	I_{ZSM}		Column 10	
End-point electrical measurements		See table I, subgroup 2 except $Z_{\theta JX}$				
Subgroup 7						
Voltage regulation		See 4.5.2	$V_{Z(reg)}$		Column 9	V dc
Temperature coefficient of regulator voltage	4071	JANS level only I_Z = column 5 of table III T_{A1} = +25°C ±5°C, T_{A2} = 120°C ≤ T_2 ≤ 130°C	α_{VZ}		Column 13	%/°C

1/ For sampling plan, see MIL-PRF-19500.
2/ Column references are to table III.

* TABLE II. Group E inspection (all quality levels).

Inspection 1/	MIL-STD-750		Sampling plan
	Method	Conditions	
Subgroup 1			22 devices c = 0
Thermal shock	1056	20 cycles, condition D except low temperature shall be achieved using liquid nitrogen (-195°C). Do a visual for cracked glass.	
Temp cycling	1051	-65°C to +175°C, 500 cycles.	
Electrical measurements		See table I, subgroup 2	
Subgroup 2			22 devices c = 0
Steady-state intermittent operating life	1037	$I_Z = I_{Z2}$ (column 8 of table III) at T_A = room ambient for 10,000 cycles. No forced air cooling on the device shall be permitted.	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			
Thermal impedance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report.	
Subgroups 5 and 6			
Not applicable			
Subgroup 8			
Resistance to glass cracking	1057	Step stress to destruction by increased cycles or up to a maximum of 25 cycles.	n = 45

1/ A separate sample may be pulled for each test.

TABLE III. Electrical characteristics and test conditions (all case outlines).

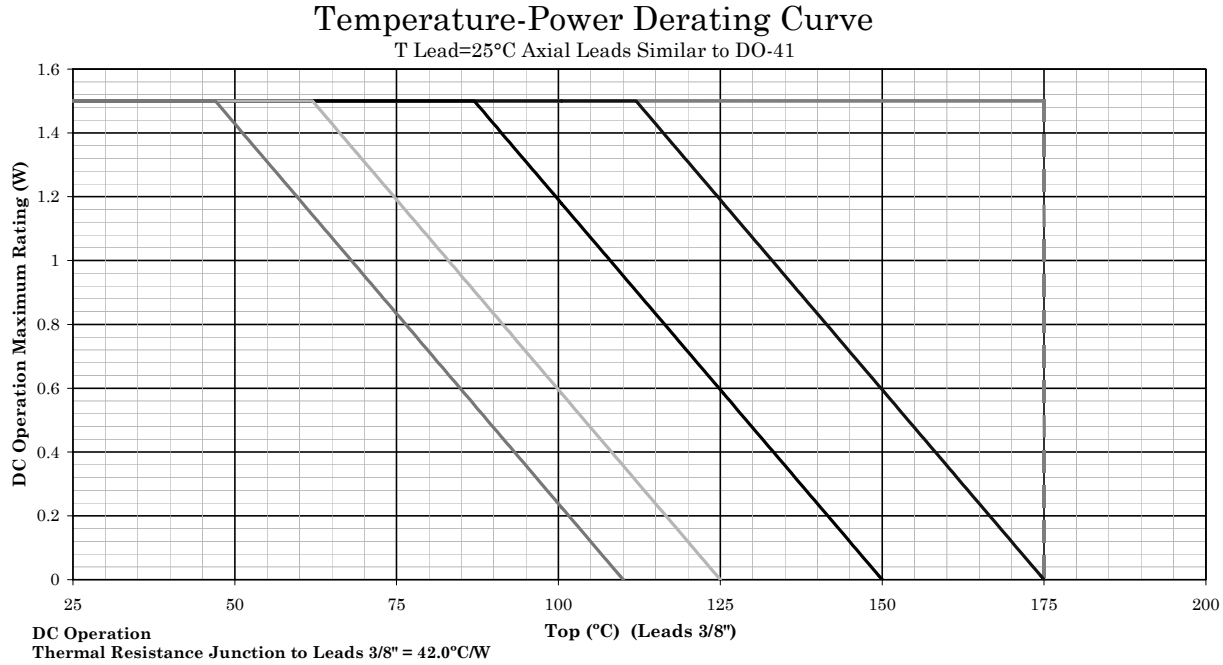
Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15
Device type	V_Z Nom	V_Z Min 1/ 2/	V_Z Max 1/ 2/	I_Z test current T_A = +25°C	Z_Z Imped-ance	Z_K Knee imped-ance	I_Z Max dc current T_A = +25°C	V_Z(reg) voltage regula-tion 3/	I_{ZSM} T_A = +25°C 4/	V_R Reverse voltage	I_R Reverse current dc I_{R1}	α_{VZ} Temper-ature coeffi-cient 5/	I_{ZK} Test current	I_R Reverse current dc T_A = +150°C I_{R2}
	V	V	V	mA	Ω	Ω	mA	V	A	V	µA	%/°C	mA	µA
1N6485	3.3	3.14	3.46	76	10	400	433	0.9	4.2	1.0	50.00	-.075	1.00	500
1N6486	3.6	3.42	3.78	69	10	400	397	0.8	3.9	1.0	50.00	-.070	1.00	200
1N6487	3.9	3.71	4.09	64	9	400	366	.75	3.6	1.0	35.00	-.060	1.00	100
1N6488	4.3	4.09	4.51	58	9	400	332	.70	3.3	1.0	5.00	-.050	1.00	100
1N6489	4.7	4.47	4.93	53	8	500	304	.60	3.0	1.0	4.00	±.025	1.00	100
1N6490	5.1	4.85	5.35	49	7	500	280	.5	2.7	1.0	1.00	±.030	1.00	100
1N6491	5.6	5.32	5.88	45	5	600	255	.40	2.5	2.0	0.50	±.040	1.00	100
1N4460	6.2	5.89	6.51	40	4	200	230	.35	2.3	3.72	10.00	+.050	1.00	50
1N4461	6.8	6.46	7.14	37	2.5	200	210	.30	2.1	4.08	5.00	+.057	1.00	20
1N4462	7.5	7.13	7.87	34	2.5	400	191	.35	1.9	4.50	1.00	+.061	0.50	10
1N4463	8.2	7.79	8.61	31	3.0	400	174	.40	1.7	4.92	0.50	+.065	0.50	5
1N4464	9.1	8.65	9.55	28	4.0	500	157	.45	1.6	5.46	0.30	+.068	0.50	3
1N4465	10	9.50	10.50	25	5.0	500	143	.50	1.4	8.0	0.30	+.071	0.25	3
1N4466	11	10.45	11.55	23	6.0	550	130	.55	1.3	8.8	0.30	+.073	0.25	2
1N4467	12	11.40	12.60	21	7.0	550	119	.60	1.2	9.6	0.20	+.076	0.25	2
1N4468	13	12.35	13.65	19	8.0	550	110	.65	1.1	10.4	0.05	+.079	0.25	2
1N4469	15	14.25	15.75	17	9.0	600	95	.75	.95	12.0	0.05	+.082	0.25	2
1N4470	16	15.20	16.80	15.5	10.0	600	90	.80	.90	12.8	0.05	+.083	0.25	2
1N4471	18	17.10	18.90	14	11.0	650	79	.83	.79	14.4	0.05	+.085	0.25	2
1N4472	20	19.00	21.00	12.5	12.0	650	71	.95	.71	16.0	0.05	+.086	0.25	2
1N4473	22	20.90	23.10	11.5	14	650	65	1.0	.65	17.6	0.05	+.087	0.25	2
1N4474	24	22.80	25.20	10.5	16	700	60	1.1	.60	19.2	0.05	+.088	0.25	2
1N4475	27	25.70	28.30	9.5	18	700	53	1.3	.53	21.6	0.05	+.090	0.25	2
1N4476	30	28.50	31.50	8.5	20	750	48	1.4	.48	24.0	0.05	+.091	0.25	2
1N4477	33	31.40	34.60	7.5	25	800	43	1.5	.43	26.4	0.05	+.092	0.25	2

See footnotes at end of table.

TABLE III. Electrical characteristics and test conditions - Continued. (all case outlines)

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15
Device type	V_Z Nom	V_Z Min 1/ 2/	V_Z Max 1/ 2/	I_Z test current T_A = +25°C	Z_Z Imped-ance	Z_K Knee imped-ance	I_Z Max dc current T_A = +25°C	V_Z(reg) voltage regula-tion 3/	I_{ZSM} T_A = +25°C 4/	V_R Reverse voltage	I_R Reverse current dc I_{R1}	α_{VZ} Temper-ature coeffi-cient 5/	I_{ZK} Test current	I_R Reverse current dc T_A = +150°C I_{R2}
	V	V	V	mA	Ω	Ω	mA	V	A	V	µA	%/°C	mA	µA
1N4478	36	34.2	37.8	7.0	27	850	40	1.7	.40	28.8	.05	+.093	0.25	2
1N4479	39	37.1	40.9	6.5	30	900	37	1.8	.37	31.2	.05	+.094	0.25	2
1N4480	43	40.9	45.1	6.0	40	950	33	1.9	.33	34.4	.05	+.095	0.25	2
1N4481	47	44.7	49.3	5.5	50	1000	30	2.1	.30	37.6	.05	+.095	0.25	2
1N4482	51	48.5	53.5	5.0	60	1100	28	2.3	.28	40.8	.05	+.096	0.25	2
1N4483	56	53.2	58.8	4.5	70	1300	26	2.5	.26	44.8	.25	+.096	0.25	10
1N4484	62	58.9	65.1	4.0	80	1500	23	2.7	.23	49.6	.25	+.097	0.25	10
1N4485	68	64.6	71.4	3.7	100	1700	21	3.0	.21	54.4	.25	+.097	0.25	10
1N4486	75	71.3	78.7	3.3	130	2000	19	3.3	.19	60.0	.25	+.098	0.25	10
1N4487	82	77.9	86.1	3.0	160	2500	17	3.6	.17	65.6	.25	+.098	0.25	10
1N4488	91	86.5	95.5	2.8	200	3000	16	4.0	.16	72.8	.25	+.099	0.25	10
1N4489	100	95.0	105.0	2.5	250	3100	14	4.4	.14	80.0	.25	+.100	0.25	10
1N4490	110	104.5	115.5	2.3	300	4000	13	5.0	.13	88.0	.25	+.100	0.25	10
1N4491	120	114.0	126.0	2.0	400	4500	12	5.5	.12	96.0	.25	+.100	0.25	10
1N4492	130	123.5		1.9	500	5000	11	6.0	.11	104	.25	+.100	0.25	10
1N4493	150	142.5	157.5	1.7	700	6000	9.5	7.0	.095	120	.25	+.100	0.25	10
1N4494	160	152	168	1.6	1000	6500	8.9	8.0	.089	128	.25	+.100	0.25	10
1N4495	180	171	189	1.4	1300	7000	7.9	10.0	.079	144	.25	+.100	0.25	10
1N4496	200	190	210	1.2	1500	8000	7.2	12.0	.072	160	.25	+.100	0.25	10

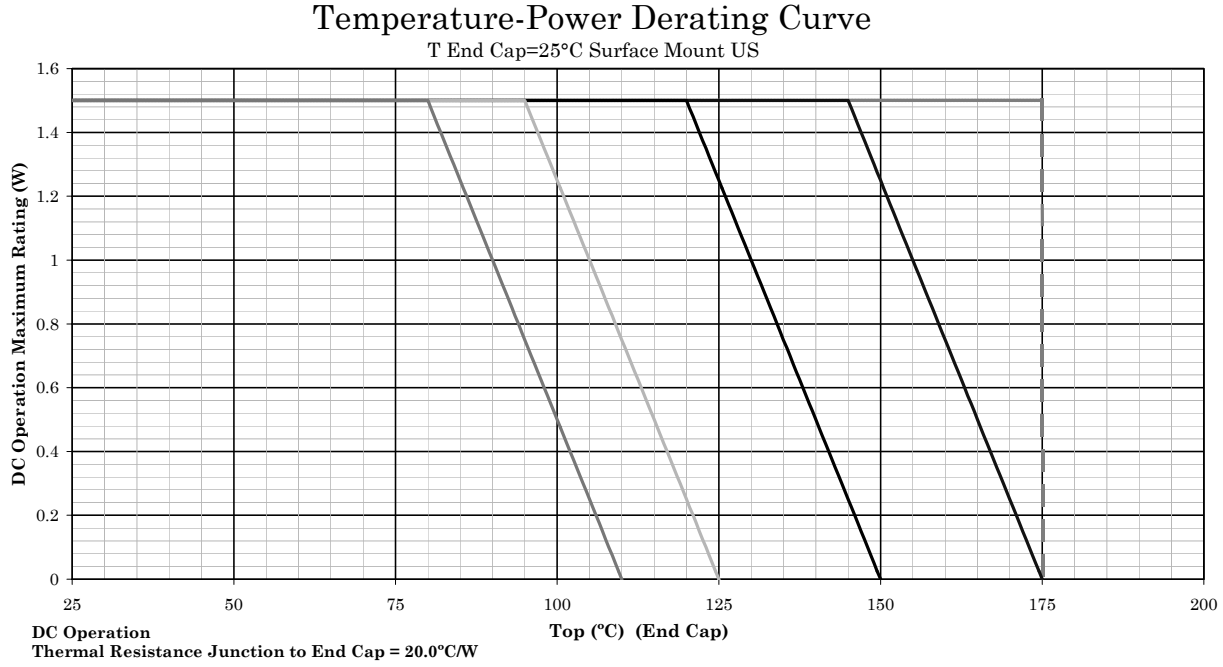
1/ See 4.5.5. Voltages shown are for 5 percent tolerance devices. Voltages for 2 and 1 percent tolerances devices shall be calculated accordingly.
2/ 1N4460D through 1N4496D and 1N6485D through 1N6491D are 1 percent voltage tolerance.
1N4460C through 1N4496C and 1N6485C through 1N6491C are 2 percent voltage tolerance.
1N4460 through 1N4496 and 1N6485 through 1N6491 are 5 percent voltage tolerance.
3/ See 4.5.2.
4/ See 4.5.1.
5/ See 4.5.3.



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperatures and current rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 3. Temperature/power derating curve.



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part.. Operating under this curve using these mounting conditions assures device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperatures and current rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 4. Temperature/power derating curve.

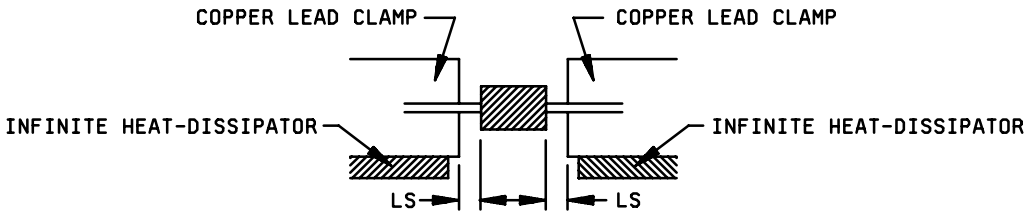


FIGURE 5. Mounting arrangement for thermal resistance measurements.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.6).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, MC
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2874)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.