REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16																	

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-01-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, CLOCK GENERATOR DRIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95715**

SHEET 1 OF 16

DESC FORM 193
JUL 94

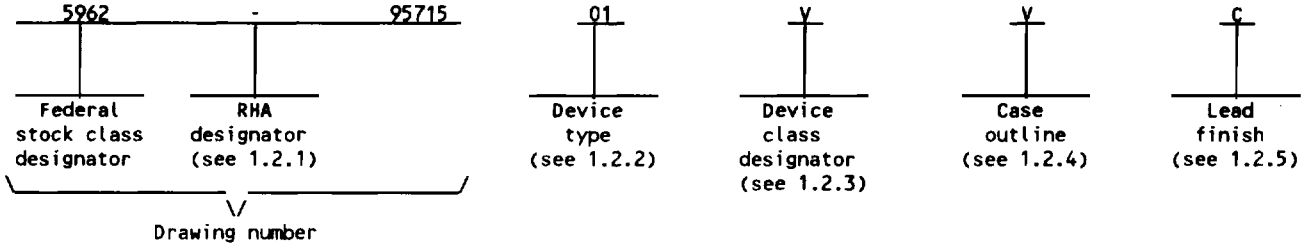
5962-E271-96

DISTRIBUTION STATEMENT A Approved for public release; distribution is unlimited

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82C84A/7	Latchup resistance CMOS clock generator driver

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	CDIP2-T18	18	Dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+7.0 V dc
Input or output voltage range	V_{SS} -0.3 V dc to V_{DD} +0.3 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+175°C
Maximum package power dissapation at T_A = +125°C (P_d) 2/	0.64 W
Thermal resistance, Junction-to-case (θ_{JC})	13°C/W
Thermal resistance, Junction-to-ambient (θ_{JA})	78°C/W
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Operating supply voltage range (V_{CC})	4.5 V dc to +5.5 V dc
Operating temperature range (T_A)	-55°C to +125°C
Input low voltage range, except RESET (V_{IL})	0 V dc to +0.8 V dc
Input high voltage range, except RESET (V_{IH})	2.2 V dc to V_{CC}
Input low voltage range (V_{IL}) RESET	0 V dc to +0.5 V dc
Input high voltage range, RESET (V_{IH})	0.86 V_{CC} to V_{CC}

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capability provide heat sinking or derate linearly (derating is based on θ_{JA}) at a rate of 12.8 mW/°C.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveform and test circuit. The timing waveform and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical input 1 voltage	V_{IH}	V_{CC} = 5.5 V, 2/ 3/	1,2,3	All	2.2		V
Logical input 2 voltage	V_{IL}	V_{CC} = 4.5 V, 2/ 3/ 4/	1,2,3	All		0.8	V
Reset logical 1 input voltage	V_{IHR}	V_{CC} = 5.5 V, Pin 11 3/	1,2,3	All	4.7		V
Reset logical 0 input voltage	V_{ILR}	V_{CC} = 4.5 V, 3/ Pin 11	1,2,3	All		0.5	V
Reset input hystersis	V_H	V_{CC} = 4.5 V, V_{CC} = 5.5 V Pin 11	1,2,3	All	$0.2*V_{CC}$		V
Output high voltage	V_{OH1}	V_{CC} = 4.5 V, I_{OH} = -2.5 mA Pins 2,5,10,12,16 5/	1,2,3	All	V_{CC}-0.4		V
Output high voltage	V_{OH2}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA Pins 8 5/	1,2,3	All	V_{CC}-0.4		V
Output low voltage	V_{OL1}	V_{CC} = 4.5 V, I_{OH} = 2.5 mA Pins 2,5,10,12,16 5/	1,2,3	All	0.4		V
Output low voltage	V_{OL2}	V_{CC} = 4.5 V, I_{OH} = 4.0 mA Pins 8 5/	1,2,3	All	0.4		V
High input leakage current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = V_{CC} Pins 1,3,4,6,7,11,13,14 untested pins = V_{CC} or GND 6/	1,2,3	All		1.0	µA
Low input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND Pins 1,3,4,6,7,11,13,14 untested pins = V_{CC} or GND 6/	1,2,3	All	-1.0		µA
Operating power supply current	I_{CCOP}	V_{DD} = 5.5 V 7/ Output open	1,2,3	All		40	mA
Input capacitance	C_{IN}	See 4.4.1c V_{CC} = Open f = 1 MHz	4	All		10	pF
Output capacitance	C_{OUT}	See 4.4.1c V_{CC} = Open f = 1 MHz	4	All		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional tests		V_{CC} = 4.5 V V_{CC} = 5.5 V	7,8	All			
TIMING REQUIREMENTS							
RDY1, RDY2 active setup time to CLK ASYNC = H	t_{R1VCL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	35		ns
RDY1, RDY2 active setup time to CLK ASYNC = L	t_{R1VCH}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	35		ns
RDY1, RDY2 inactive setup time to CLK ASYNC = L	t_{R1VCH}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	35		ns
RDY1, RDY2 hold to CLK	t_{CLR1X}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	0		ns
$\overline{\text{ASYNC}}$ setup to CLK	t_{AYVCL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	50		ns
$\overline{\text{ASYNC}}$ hold to CLK	t_{CLAYX}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	0		ns
$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ setup to RDY1, RDY2	t_{A1VR1V}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	15		ns
$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ hold to CLK	t_{CLA1X}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	0		ns
CSYNC setup to EFI	t_{YHEH}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	20		ns
CSYNC hold to EFI	t_{EHYL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING REQUIREMENTS - CONTINUED.							
RES setup to CLK	t_{I1HCL}	V_{CC} = 4.5 V 3/ 8/ 9/ V_{CC} = 5.5 V	9,10,11	All	65		ns
External frequency high time	t_{EHEL}	V_{CC} = 4.5 V 3/ 8/ 10/ V_{CC} = 5.5 V	9,10,11	All	18		ns
External frequency low time	t_{ELEH}	V_{CC} = 4.5 V 3/ 8/ 10/ V_{CC} = 5.5 V	9,10,11	All	18		ns
EFI period	t_{ELEL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All	36		ns
OSC to CLK high time delay	t_{OLCH}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All		22	ns
OSC to CLK low time delay	t_{OLCL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All		35	ns
XTAL frequency		V_{CC} = 4.5 V 8/ 11/ V_{CC} = 5.5 V	9,10,11	All	2.4	25	MHz
TIMING RESPONES							
RES hold to CLK	t_{CLI1H}	V_{CC} = 4.5 V 3/ 8/ 9/ V_{CC} = 5.5 V	9,10,11	All	20		ns
CLK cycle period	t_{CLCL}	V_{CC} = 4.5 V 8/ 12/ V_{CC} = 5.5 V	9,10,11	All	125		ns
CLK high time	t_{CHCL}	V_{CC} = 4.5 V 8/ 12/ V_{CC} = 5.5 V	9,10,11	All	$(1/3)t_{CLCL}$ -2.0		ns
CLK low time	t_{CLCH}	V_{CC} = 4.5 V 8/ 12/ V_{CC} = 5.5 V	9,10,11	All	$(2/3)t_{CLCL}$ -15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING RESPONES - CONTINUED.							
CLK rise or fall time	t_{CH1CH2} t_{CL2CL1}	V_{CC} = 4.5 V 8/ V_{CC} = 5.5 V 1.0 V to 3.0 V	9,10,11	All		10	ns
PCLK high time	t_{PHPL}	V_{CC} = 4.5 V 8/ 12/ V_{CC} = 5.5 V	9,10,11	All	t_{CLCL}-20		ns
PCLK low time	t_{PLPH}	V_{CC} = 4.5 V 8/ 12/ V_{CC} = 5.5 V	9,10,11	All	t_{CLCL}-20		ns
Ready inactive to CLK	t_{RYLCL}	V_{CC} = 4.5 V 3/ 8/ 13/ V_{CC} = 5.5 V	9,10,11	All	-8		ns
Ready active to CLK	t_{RYHCH}	V_{CC} = 4.5 V 3/ 8/ 13/ V_{CC} = 5.5 V	9,10,11	All	$(2/3)t_{CLCL}$ -15		ns
CLK to reset delay	t_{CLIL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All		40	ns
CLK to PCLK high delay	t_{CLPH}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All		22	ns
CLK to PCLK low delay	t_{CLPL}	V_{CC} = 4.5 V 3/ 8/ V_{CC} = 5.5 V	9,10,11	All		22	ns
CSYNC width	t_{TYHYL}	15/ 16/	9,10,11	All	$2*t_{ELEL}$		ns
OSC to CLK high delay	t_{OLCH}	15/ 16/	9,10,11	All	-5		ns
OSC to CLK low delay	t_{OHCL}	15/ 16/	9,10,11	All	2		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ All Testing to be performed using worst case test conditions unless otherwise specified.

2/ F/$\overline{C}$ is a strap on option and should be held ≤ 0.8 V or ≥ 2.2 V. Does not apply to X1 or X2 pins.

3/ This test is performed as Go/No Go. There are no recorded measurements.

4/ CSYNC pin is tested with V_{IL} < = 0.8 V.

5/ Interchanging force and sense conditions is permitted.

6/ $\overline{\text{ASYNC}}$ pin includes an internal 17.5 k pull-up resistor. For $\overline{\text{ASYNC}}$ input at GND, $\overline{\text{ASYNC}}$ input leakage = 300 µA nominal

7/ f = 25 MHz may be tested using the extrapolated value based on measurements at f = 2 MHz and f = 10 MHz.

8/ F = 2.4 Mhz, V_{IH} = 2.6 V, V_{IL} = 0.4 V, V_{OH} ≥ 1.5 V, V_{OL} ≤ 1.5 V unless otherwise specified. $\overline{\text{RES}}$ and F/$\overline{C}$ must switch between 0.4 V and V_{CC} - 0.4 V. Input rise and fall times are driven at 1 ns/V. V_{IL} ≤ V_{IL}(max) - 0.4 V for CSYNCH pin.

9/ Setup and hold necessary only to guarantee recognition at next clock.

10/ TELEH and TEHEL are determined by 50 percent points.

11/ Tested using EFI or X1 input pin.

12/ Tested with EFI input frequency = 4.2 MHz.

13/ Applies only to T2 states.

14/ Applies only to T3, TW states.

15/ Input test signal must switch between V_{IL}(Max) - 0.4 V and V_{IH}(Min) + 0.4 V $\overline{\text{RES}}$ and F/$\overline{C}$ must switch between 0.4 V and V_{CC} - 0.4 V. Input rise and fall times driven at 1ns/V. V_{IL} = V_{IL}(Max) - 0.4 V for CSYNCH pin. V_{CC} = 4.5 V and 5.5 V.

16/ This parameter is guaranteed but not tested. This parameter is characterizedupon initial design or process change which affects this parameter.

Device type	All
Case outline	V
Terminal number	Terminal symbol
1	CSYNC
2	PCLK
3	$\overline{\text{AEN1}}$
4	RDY1
5	READY
6	RSY2
7	$\overline{\text{AEN2}}$
8	CLK
9	GND
10	RESET
11	$\overline{\text{RES}}$
12	OSC
13	F/$\overline{\text{C}}$
14	EFI
15	$\overline{\text{ASYNC}}$
16	X2
17	X1
18	V_{CC}

FIGURE 1. Terminal connections.

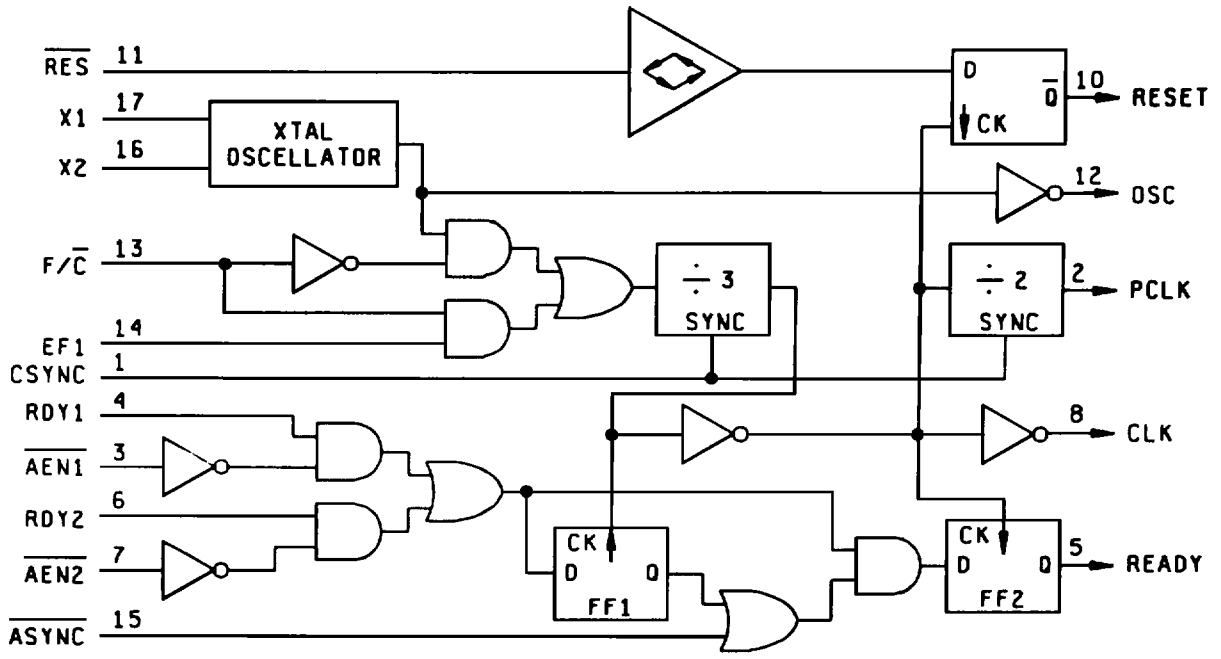
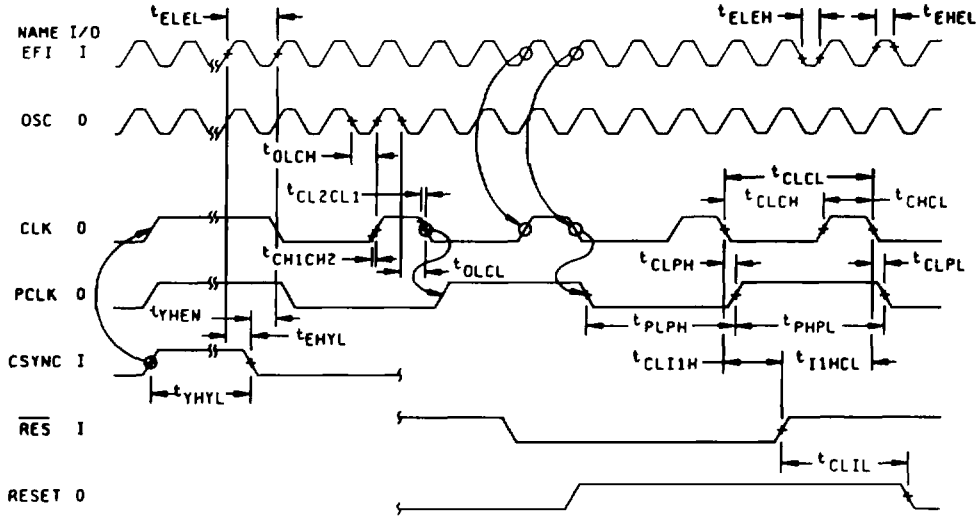
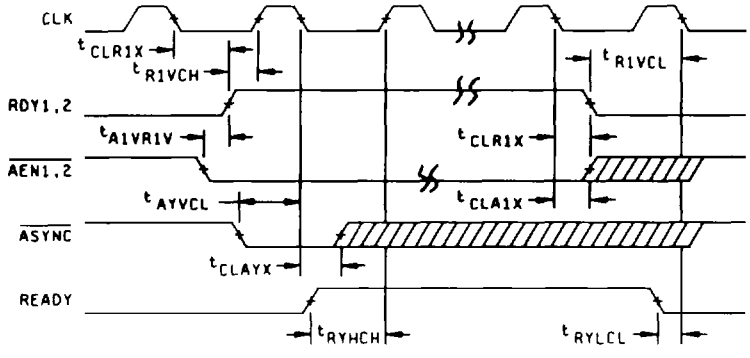


FIGURE 2. Block diagram.

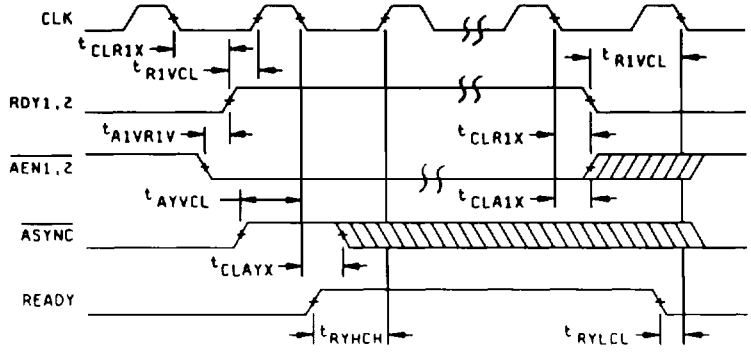
WAVEFORM FOR CLOCKS AND RESET SIGNALS



WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)



Note: All timings measurements are made at 1.5 V unless otherwise noted.

FIGURE 3. Timing waveform and test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535, or as modified in the device manufacturers approved Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535, or as modified in the QM plan, including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9, 1/ 10,11	1,2,3,7,8,1/ 9,10,11	1,2,3,7,2/ 8,9,10,11 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9 10,11	1,2,3,4,7,8,9 10,11	1,2,3,4,7,8,9 10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1,7 and delta's.
3/ Delta limits are as specified in Table IIB herein shall be required where specified and the delta values shall be completed with reference to the zero hour electrical parameters.

Table IIB

Parameter	Symbol	Delta limits
Standby power supply current	ICCSB	+/- 3.0 µA
Input leakage current	IIL,IIH	+/- 200 nA

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.
b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.
c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-01-11

Approved sources of supply for SMD 5962-95715 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9571501VVC	34371	MD82C84A/7

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne Fl 32902-0883