CA3240A, CA3240

Dual BiMOS Operational Amplifiers

With MOSFET Input, Bipolar Output

Features:
- *Dual version of CA3140*
- *Internally compensated*
- *MOSFET input stage*
  - (a) *Very high input impedance (Z_{IN}) - 1.5 TΩ typ.*
  - (b) *Very low input current (I_I) - 10 pA typ. at ±15 V*
  - (c) *Wide common-mode input-voltage range (V_{ICR}) - can be swung 0.5 volt below negative supply-voltage rail*
- *Directly replaces industry types 747 and 1458 in most applications*

The RCA-CA3240A and CA3240 are dual versions of the popular CA3140-series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating-temperature range of −40 to +85° C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix). The CA3240 is also available in chip form (H suffix).

Applications:
- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds - minutes - hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Intrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

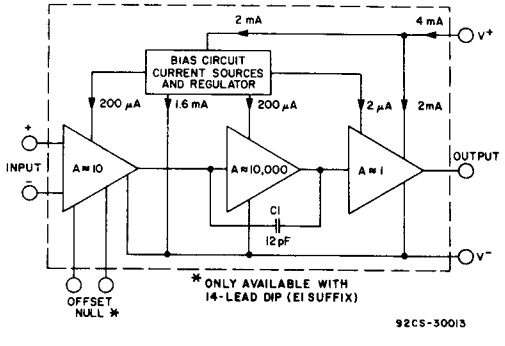


Fig. 1 — Block diagram of one-half CA3240 series.

File Number **1050**

CA3240A, CA3240

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	4 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	−40 to +85°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION●	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ±1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

● Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

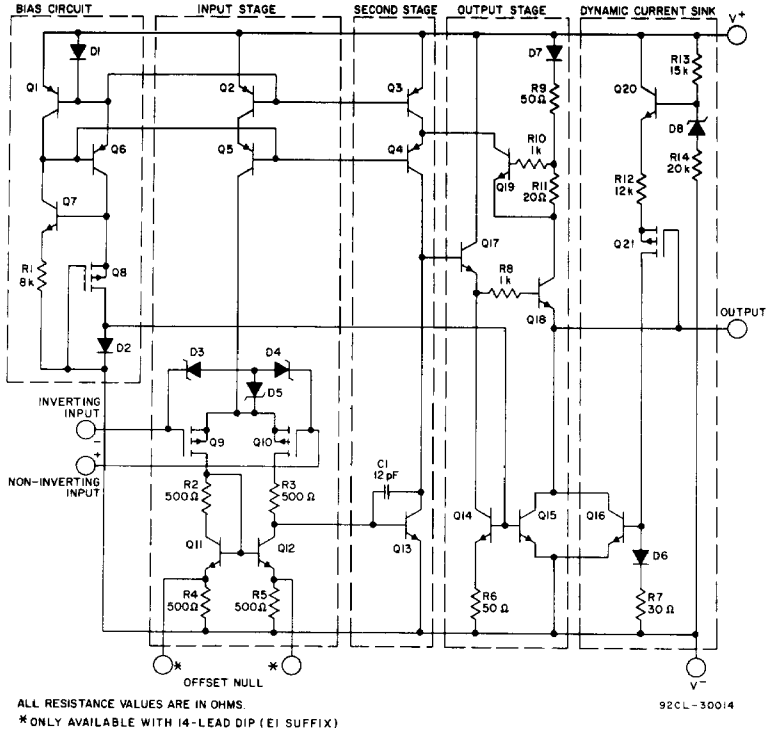


Fig. 2 — Schematic diagram of one-half CA3240 series.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and V^+.* The dynamic current sink becomes active whenever the output terminal is more negative than V^+ by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V^-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V (V_{CE}(sat)) of V^- with a 2-kΩ load to ground. *When the load is returned to V^+, it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (approx. 2 kΩ) between the output and V^-.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

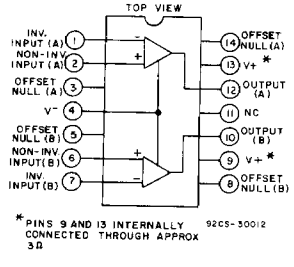
CHARACTERISTIC	LIMITS						UNITS
	CA3240A			CA3240			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO}\rvert$	–	2	5	–	5	15	mV
Input Offset Current, $\lvert I_{IO}\rvert$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}●	20 k	100 k	–	20 k	100 k	–	V/V
(See Figs. 4, 19)	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR	–	32	320	–	32	320	μV/V
(See Fig. 9)	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig. 16)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$ PSRR	–	100	150	–	100	150	μV/V
(See Fig. 11)	76	80	–	76	80	–	dB
Maximum Output Voltage,■ V_{OM}^+	+12	13	–	+12	13	–	V
(See Figs. 22, 16) V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Maximum Output Voltage,† V_{OM}^-	0.4	0.13	–	0.4	0.13	–	V
Supply Current, I^+ (See Fig. 7) For Both Amps.	–	8	12	–	8	12	mA
Total Device Dissipation, P_D	–	240	360	–	240	360	mW

● At V_O = 26 V_{p-p}, +12 V, −14 V and R_L = 2 kΩ.
■ At R_L = 2 kΩ.
† At V^+ = 5 V, V^- = GND, I_{Sink} = 200 μA.

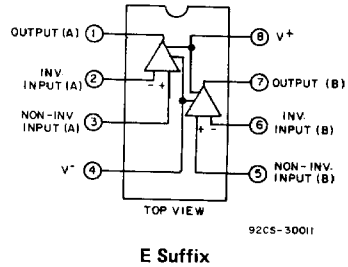
CA3240A, CA3240

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25°C$		TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}		18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz R_S = 1 MΩ		48	48	μV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz	R_S= 100 Ω	40	40	$nV/\sqrt{Hz}$
		f=10 kHz		12	12	
Short-Circuit Current to Opposite Supply Source	I_{OM}^+			40	40	mA
Sink	I_{OM}^-			11	11	
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T			4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR			9	9	V/μs
Transient Response: Rise Time	t_r	R_L=2 kΩ		0.08	0.08	μs
Overshoot (See Fig. 20)		C_L=100 pF		10	10	%
Settling Time at 10 V_{p-p}, (See Fig. 17)	t_s 1 mV	R_L=2 kΩ C_L=100 pF Voltage Follower		4.5	4.5	μs
	t_s 10 mV			1.4	1.4	
Crosstalk		f = 1 kHz		120	120	dB



E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 3 – Functional diagrams.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = −40 to +85°C Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\lvert V_{IO} \rvert$	3	10	mV
Input Offset Current,♦	$\lvert I_{IO} \rvert$	32	32	pA
Input Current,♦	I_I	640	640	pA
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}●	63 k	63 k	V/V
		96	96	dB
Common-Mode Rejection Ratio, (See Fig. 9)	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 16)	V_{ICR}	−15 to +12.3	−15 to +12.3	V
Power-Supply Rejection Ratio, (See Fig. 11)	$\frac{\Delta V_{IO}/\Delta V}{PSRR}$	150	150	μV/V
		76	76	dB
Maximum Output Voltage,■ (See Figs. 16, 22)	V_{OM}^+	12.4	12.4	V
	V_{OM}^-	−14.2	−14.2	
Supply Current, (See Fig. 7) For Both Amps.	I^+	8.4	8.4	mA
Total Device Dissipation,	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage,	$\Delta V_{IO}/\Delta T$	15	15	μV/°C

● At V_O = 26 V_{p-p}, +12 V, −14 V and R_L = 2 kΩ.
■ At R_L = 2 kΩ.
♦ At T_A = 85°C

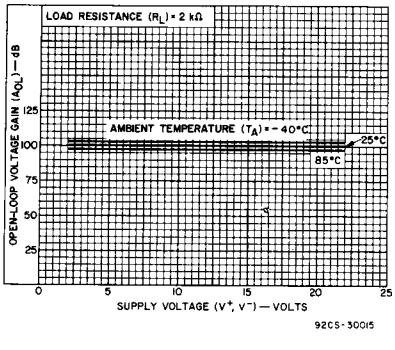


Fig. 4 — Open-loop voltage gain as a function of supply voltage and temperature.

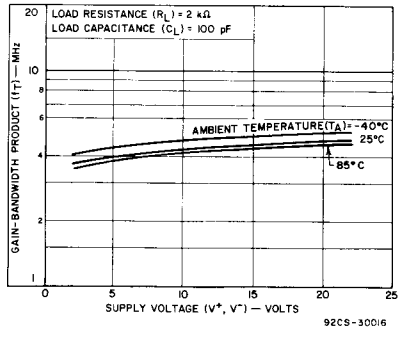


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

CA3240A, CA3240

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\|V_{IO}\|$	2	5	mV
Input Offset Current,	$\|I_{IO}\|$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	−0.5	−0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio,	PSRR	31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage, (See Figs. 16,22)	V_{OM}^+	3	3	V
	V_{OM}^-	0.3	0.3	
Maximum Output Current: Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW

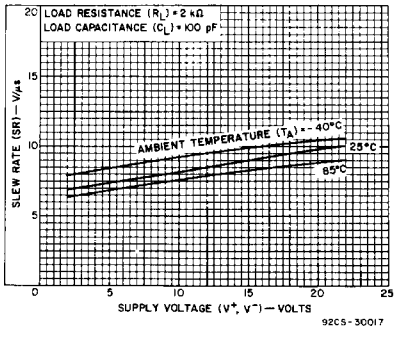


Fig. 6 — Slew rate as a function of supply voltage and temperature.

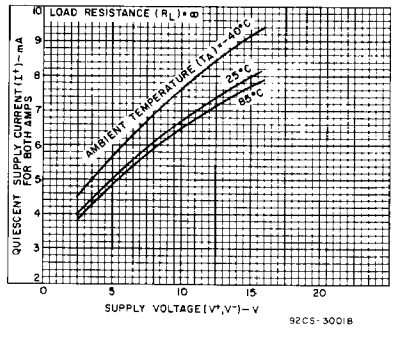


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

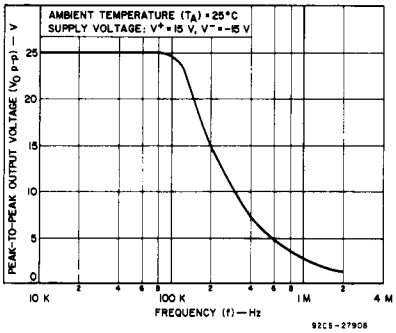


Fig. 8 – Maximum output voltage swing as a function of frequency.

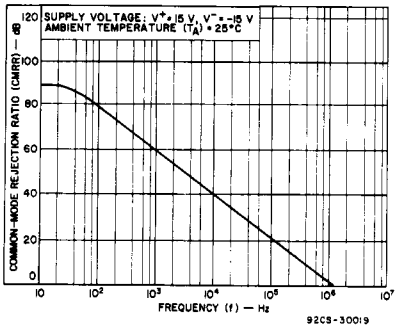


Fig. 9 – Common-mode rejection ratio as a function of frequency.

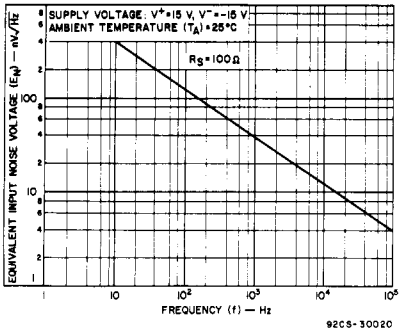


Fig. 10 – Equivalent input noise voltage as a function of frequency.

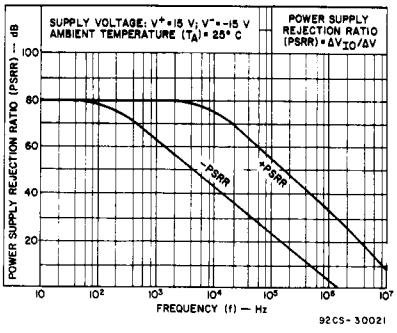


Fig. 11 – Power supply rejection ratio as a function of frequency.

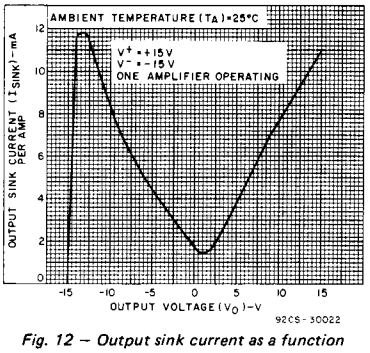


Fig. 12 – Output sink current as a function of output voltage.

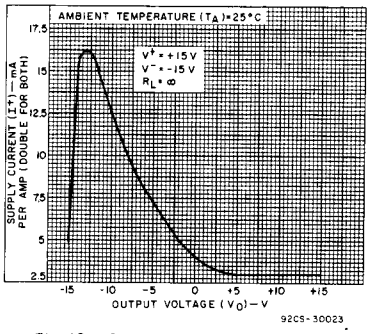


Fig. 13 – Supply current as a function of output voltage.

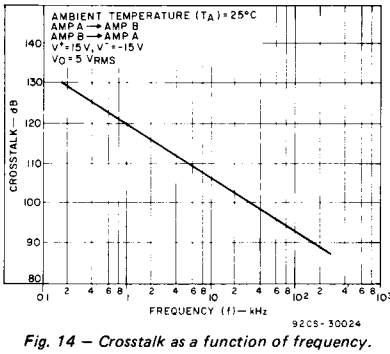


Fig. 14 – Crosstalk as a function of frequency.

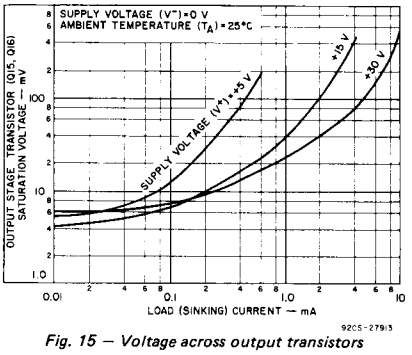


Fig. 15 – Voltage across output transistors Q15 and Q16 as a function of load current.

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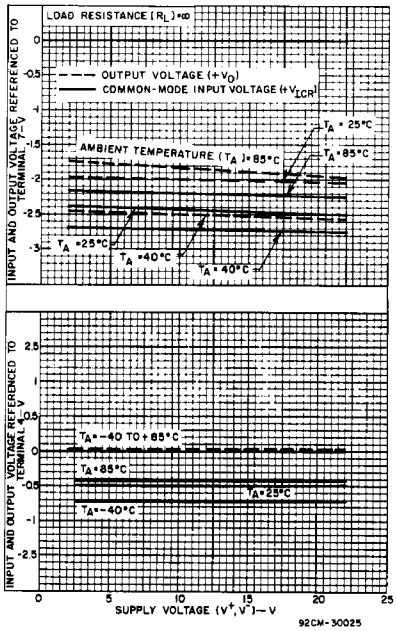


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

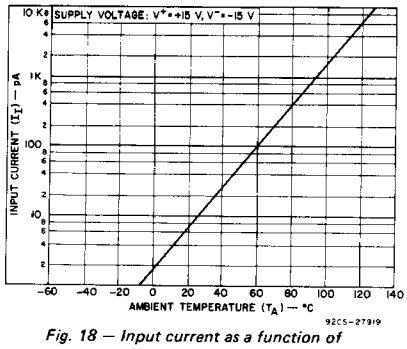


Fig. 18 — Input current as a function of ambient temperature.

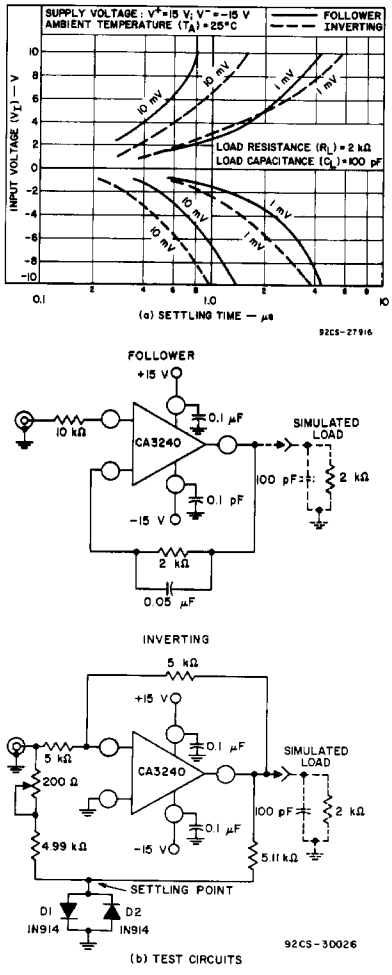


Fig. 17 — Input voltage as a function of settling time.

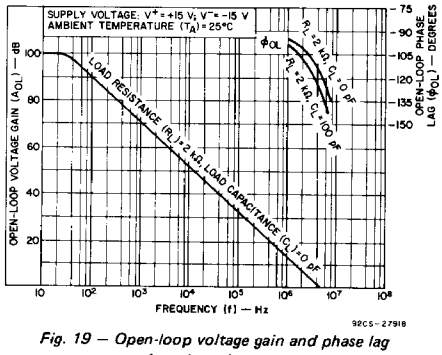
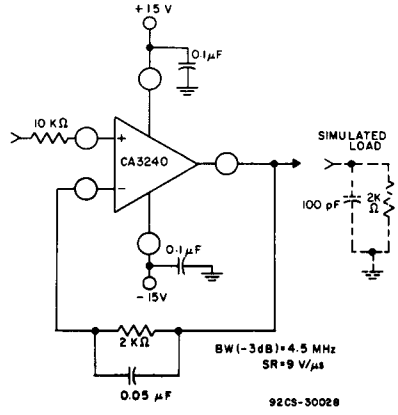
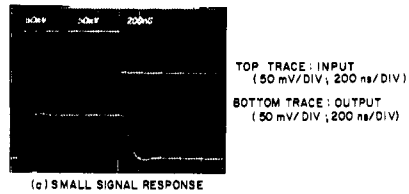
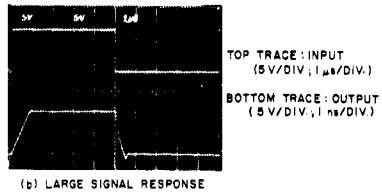


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.





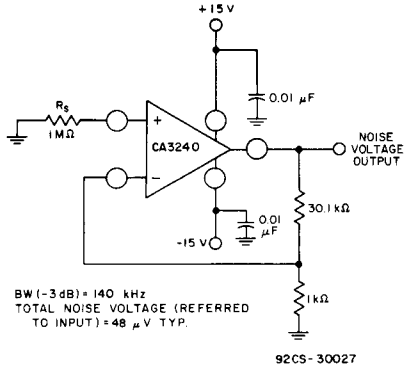
(a) SMALL SIGNAL RESPONSE



(b) LARGE SIGNAL RESPONSE

92CS-30029

Fig. 20 – Split-supply voltage-follower test circuit and associated waveforms.



92CS-30027

Fig. 21 – Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

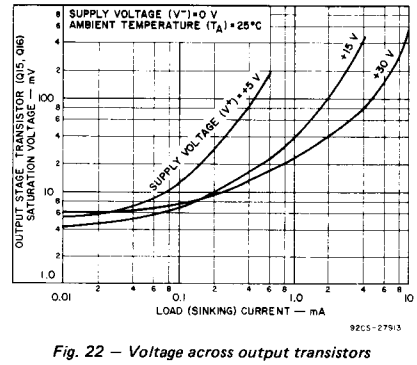


Fig. 22 – Voltage across output transistors Q15 and Q16 as a function of load current.

CA3240A, CA3240

APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

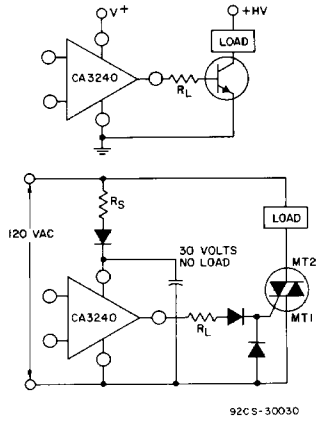


Fig. 23 — Methods of utilizing the $V_{CE(sat)}$ sinking-current capability of the CA3240 series.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

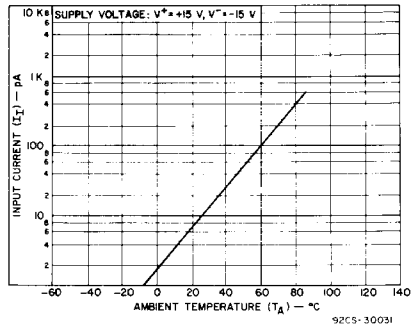


Fig. 24 — Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

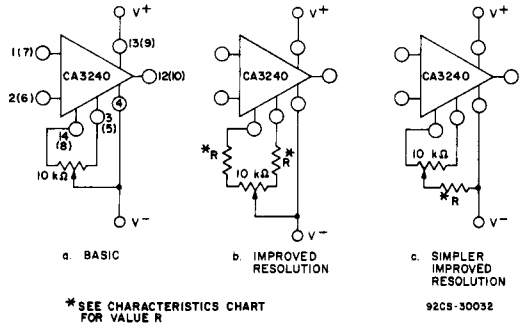


Fig. 25 – Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

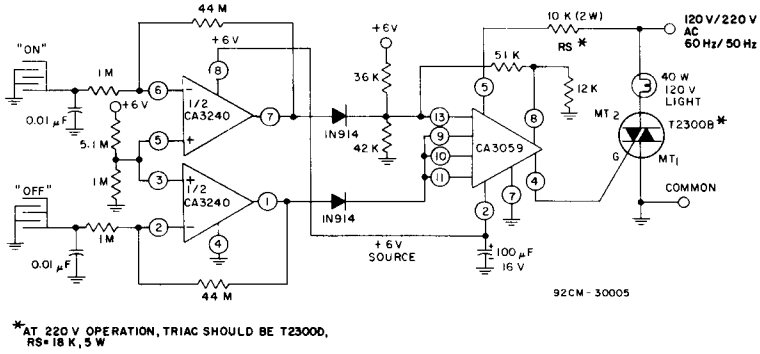


Fig. 26 – On/off touch switch.

CA3240A, CA3240

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

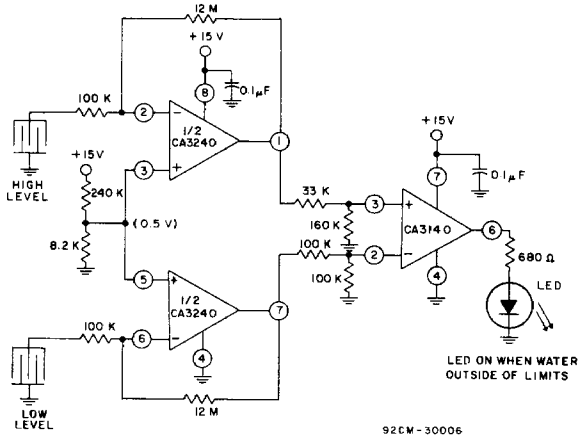


Fig. 27 – Dual level detector.

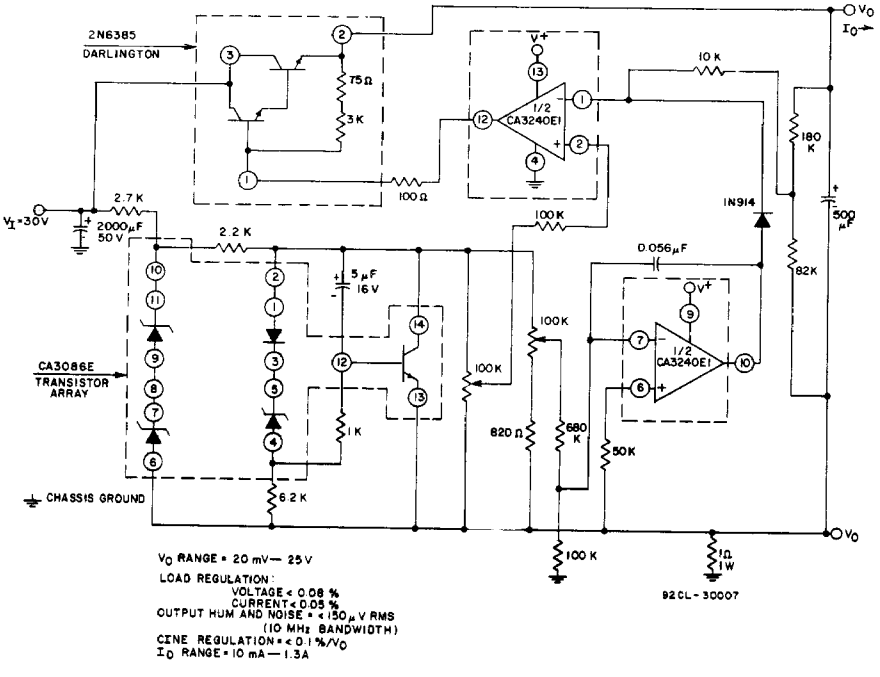
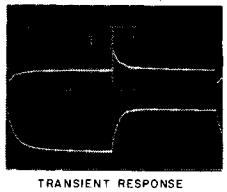


Fig. 28 – Constant-voltage/constant-current power supply.

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.



TRANSIENT RESPONSE

TOP TRACE: OUTPUT VOLTAGE
(500 mV/cm AND 5 μs/cm)
BOTTOM TRACE: COLLECTOR OF LOAD
SWITCHING TRANSISTOR
LOAD = 100 mA TO 1A
(5 V/cm AND 5 μs/cm)

92CS-30034

Fig. 29 — Transient response.

Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.

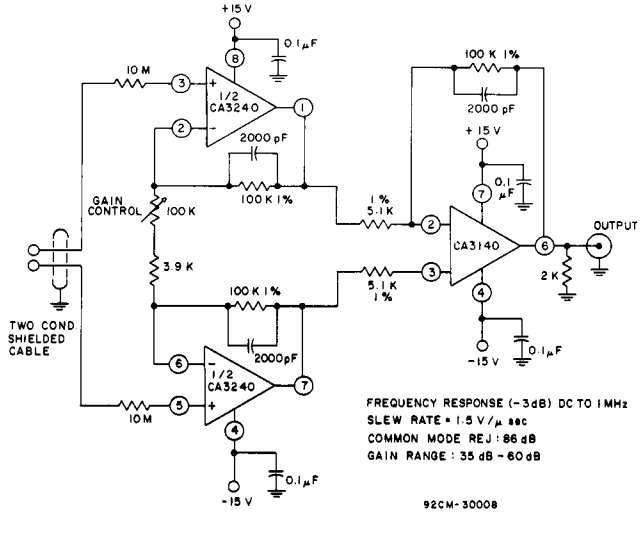


Fig. 30 — Precision differential amplifier.

CA3240A, CA3240

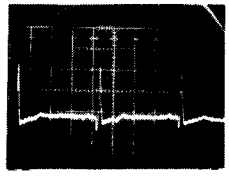


Fig. 31 – Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

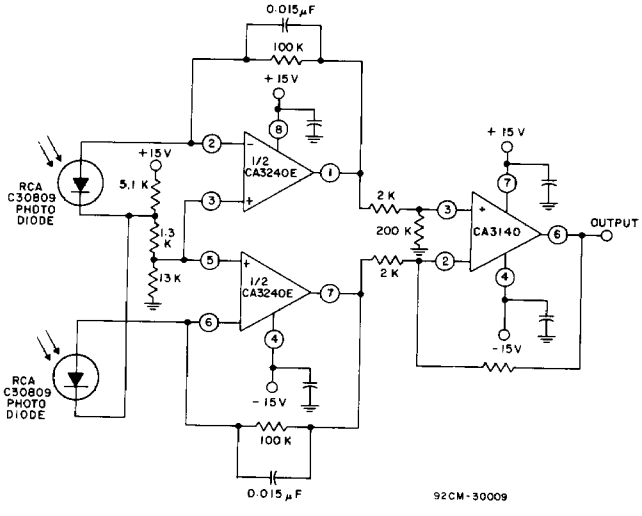
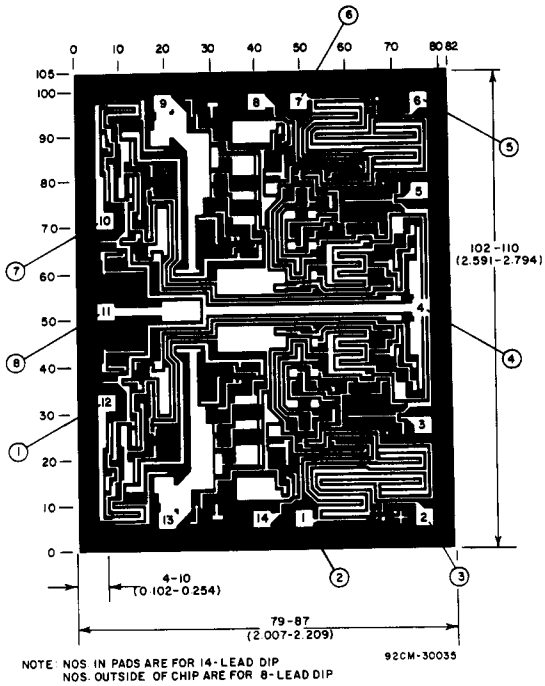


Fig. 32 – Differential light detector.

CA3240H Dimensions and Pad Layout



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).