FemtoClock® Crystal/LVCMOS-to-LVCMOS/LVTTL Frequency Synthesizer

840024I

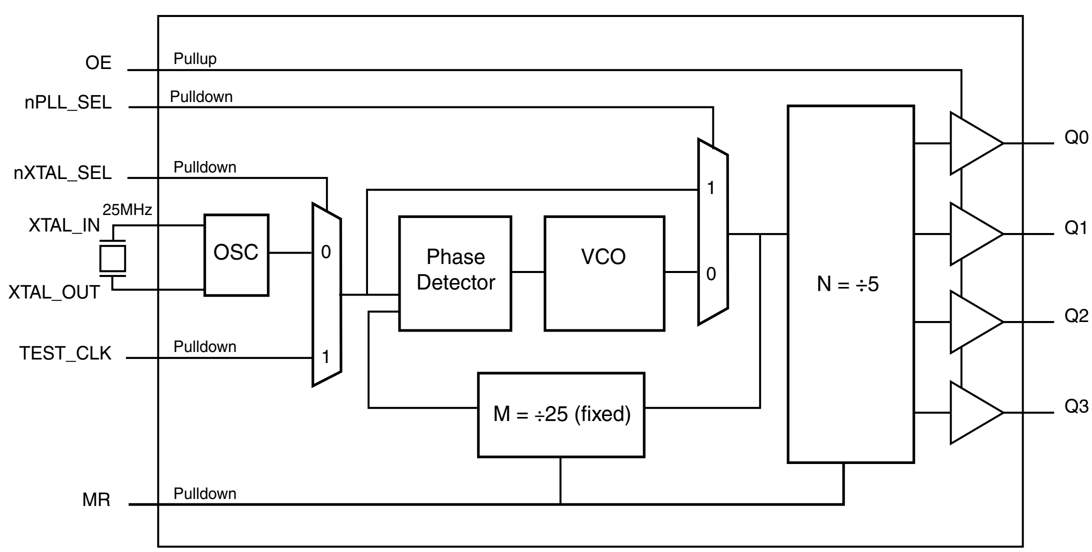
General Description

The 840024I is a four output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequency. The 840024I uses IDT's 3RD generation low phase noise VCO technology and can achieve 1ps or lower typical random RMS phase jitter, easily meeting Ethernet jitter requirements. The 840024I is packaged in a small 20-pin TSSOP package.

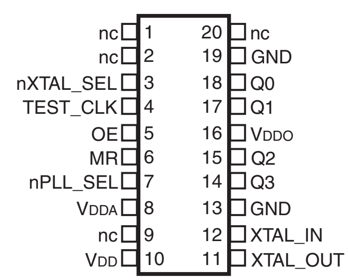
Features

- Four LVCMOS / LVTTL outputs
- Selectable crystal oscillator interface or LVCMOS / LVTTL single-ended clock input
- Supports the following output frequency: 125MHz
- RMS phase jitter @125MHz (1.875MHz - 20MHz): 0.6ps (typical)
- Power supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 9, 20	nc	Unused		No connect pins.
3	nXTAL_SEL	Input	Pulldown	PLL reference select control input. See Table 3A. LVCMOS/LVTTL interface levels.
4	TEST_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
5	OE	Input	Pullup	Output enable control pin. See Table 3B. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Master reset control pin. See Table 3C. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	PLL bypass control input. See Table 3D. LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
10	V_{DD}	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
13, 19	GND	Power		Power supply ground.
14, 15, 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. 17Ω output impedance. LVCMOS/LVTTL interface levels.
16	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		17		Ω
		V_{DDO} = 2.5V ± 5%		21		Ω

Function Tables

Table 3A. nXTAL_SEL PLL Reference Select Function Table

nXTAL_SEL	PLL Reference Input
0 (default)	XTAL Interface
1	TEST_CLK

Table 3B. Output Enable Function Table

OE	Output Operation
0	Q[0:3] are disabled in high-impedance state.
1 (default)	Q[0:3] are enabled.

Table 3C. Master Reset Function Table

MR	Reset Operation
0 (default)	Normal operation, internal dividers are enabled.
1	Internal dividers are reset, Q[0:3] are disabled in logic low state.

Table 3D. PLL Bypass Function Table

nPLL_SEL	PLL Operation
0 (default)	PLL is enabled
1	PLL is bypassed. The output frequency is equal to the selected reference frequency divided by the output divider of 5.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.14	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Core Supply Current				90	mA
I_{DDA}	Analog Supply Current				14	mA
I_{DDO}	Output Supply Current	No Load			8	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.14	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Core Supply Current				90	mA
I_{DDA}	Analog Supply Current				14	mA
I_{DDO}	Output Supply Current	No Load			8	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.14	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Core Supply Current				90	mA
I_{DDA}	Analog Supply Current				14	mA
I_{DDO}	Output Supply Current	No Load			8	mA

Table 4D. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
		TEST_CLK, MR, nXTAL_SEL, nPLL_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		TEST_CLK, MR, nXTAL_SEL, nPLL_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		V_{DDO} = 3.3V ± 5%; I_{OH} = -12mA	2.6			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5% or 2.5V ± 5%; I_{OL} = 12mA			0.5	V

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
*t*sk(o)	Output Skew; NOTE 1, 2			20	60	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz, Integration Range: 1.875MHz – 20MHz		0.604		ps
t_{LOCK}	PLL Lock Time			50	100	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	250	400	750	ps
odc	Output Duty Cycle		42	50	58	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with crystal input.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to phase noise plots.

Table 6B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
*t*sk(o)	Output Skew; NOTE 1, 2			20	60	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz, Integration Range: 1.875MHz – 20MHz		0.546		ps
t_{LOCK}	PLL Lock Time			50	100	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	250	400	750	ps
odc	Output Duty Cycle		46	50	54	%

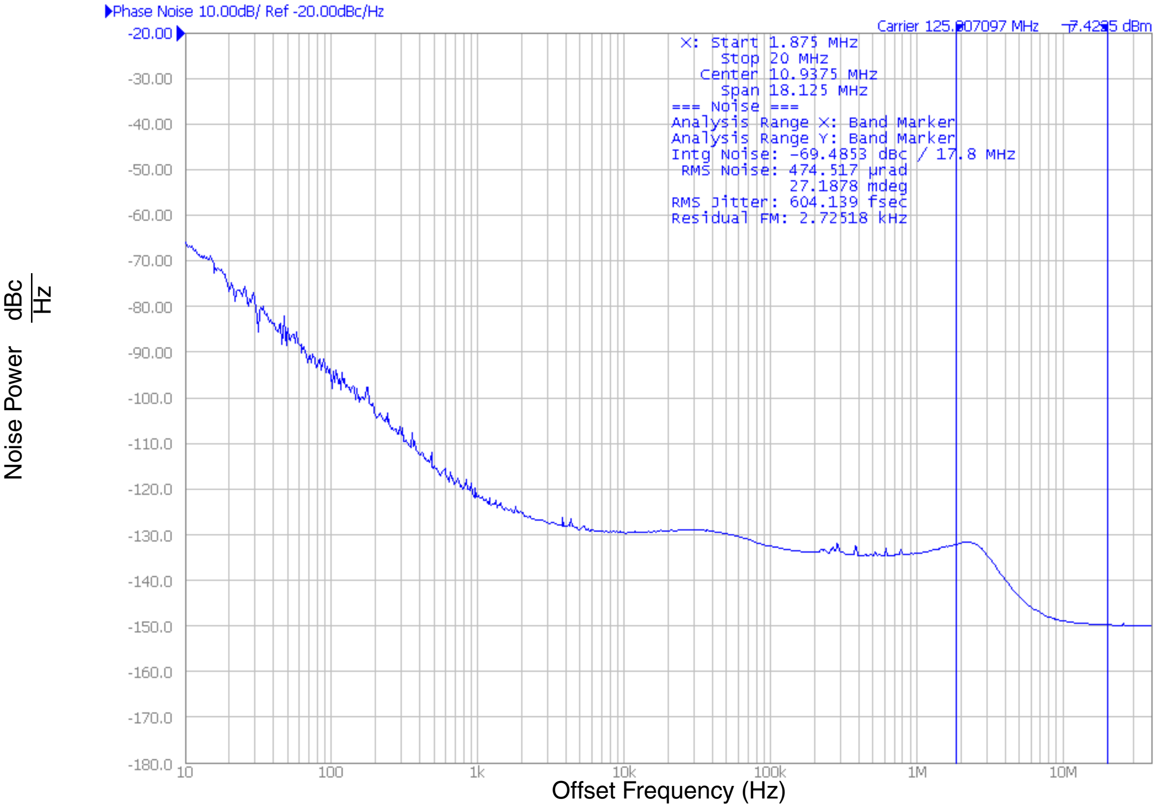
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with crystal input.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to phase noise plots.

Table 6C. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

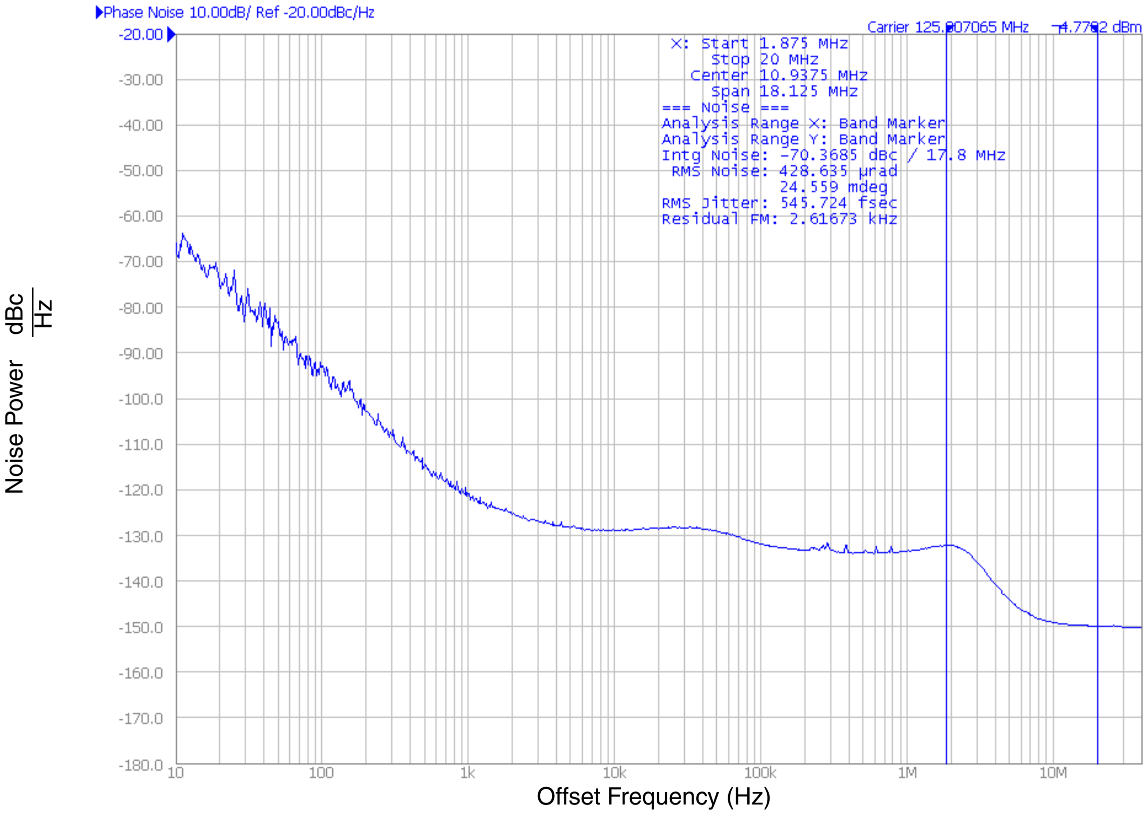
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
*t*sk(o)	Output Skew; NOTE 1, 2			20	60	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz, Integration Range: 1.875MHz – 20MHz		0.544		ps
t_{LOCK}	PLL Lock Time			50	100	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	250	400	750	ps
odc	Output Duty Cycle		42	50	58	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with crystal input.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to phase noise plots.

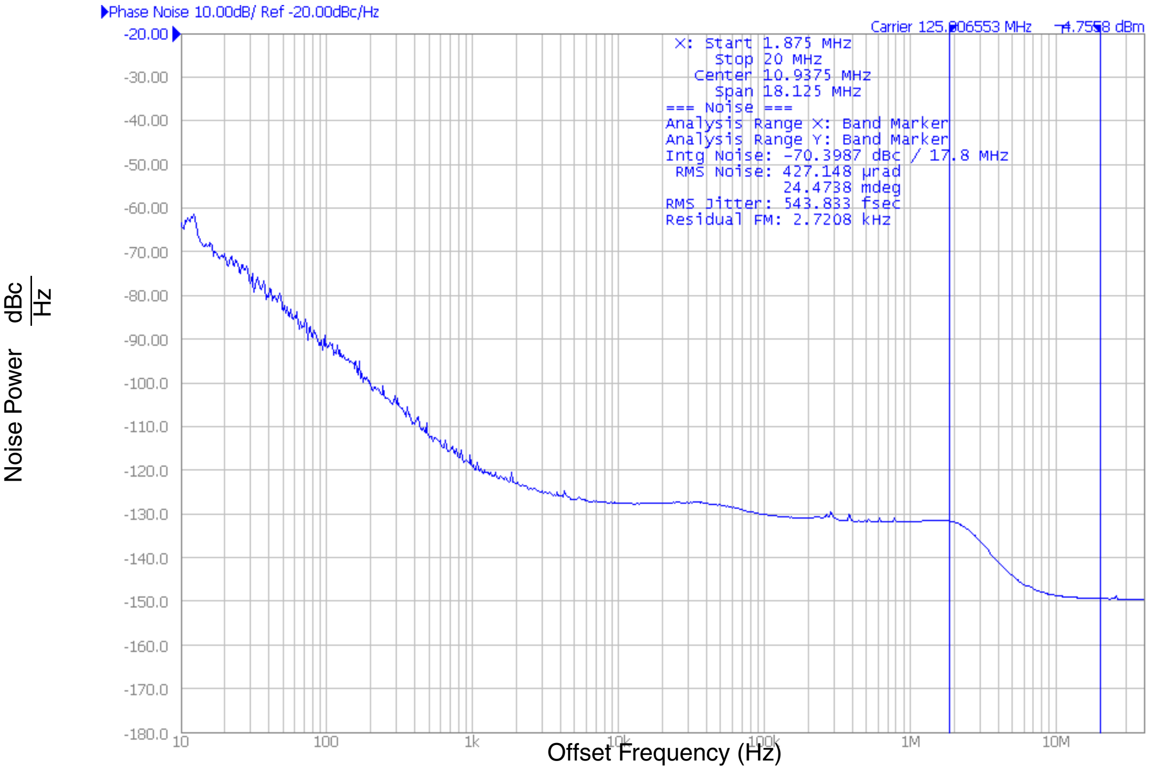
Typical Phase Noise at 125MHz (3.3V/3.3V)



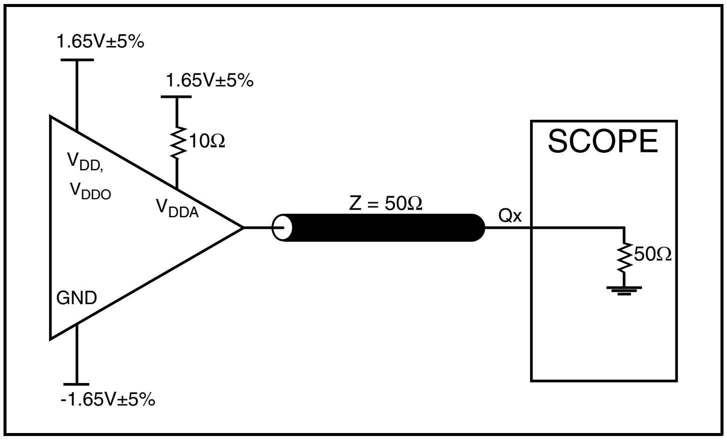
Typical Phase Noise at 125MHz (3.3V/2.5V)



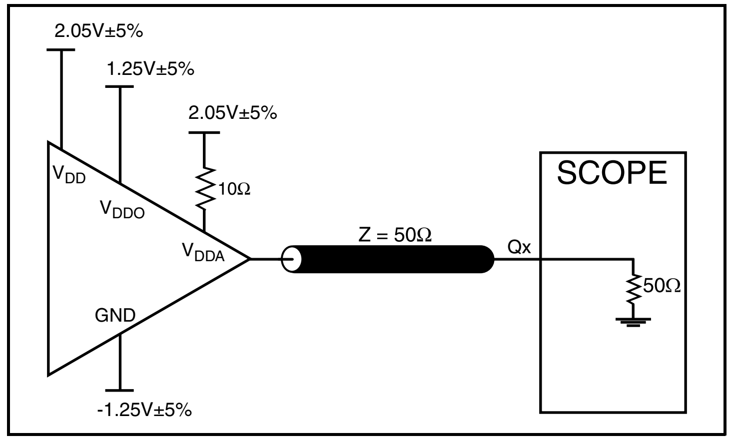
Typical Phase Noise at 125MHz (2.5V/2.5V)



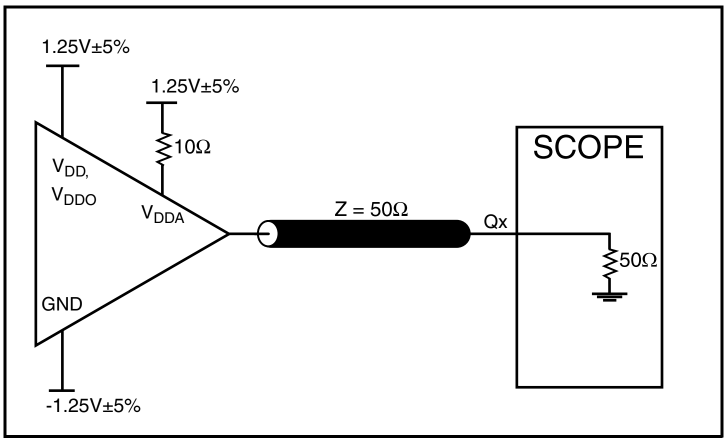
Parameter Measurement Information



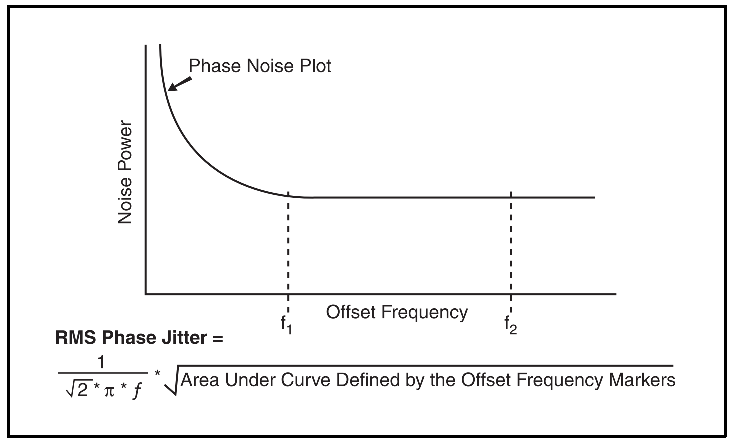
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



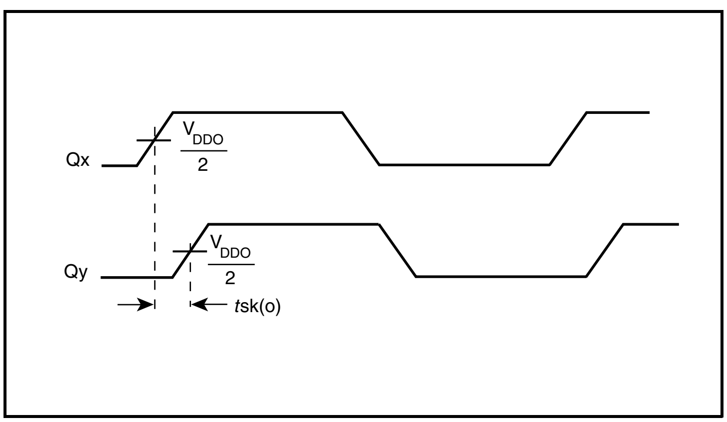
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



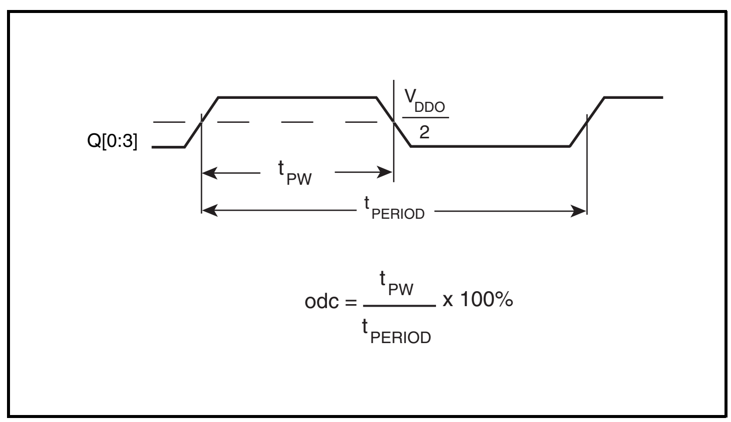
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



RMS Phase Jitter

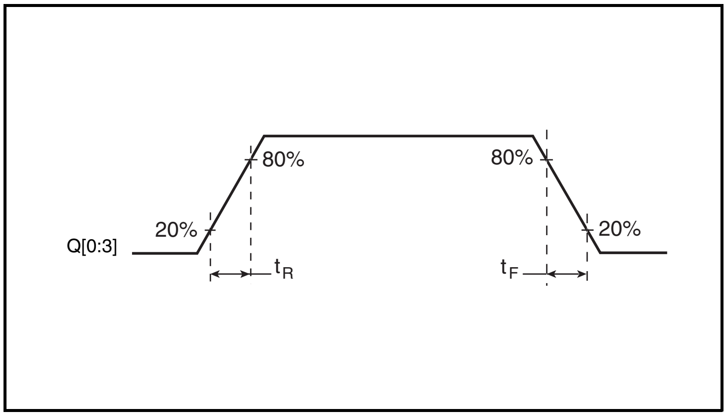


Output Skew



Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

TEST_CLK Input

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

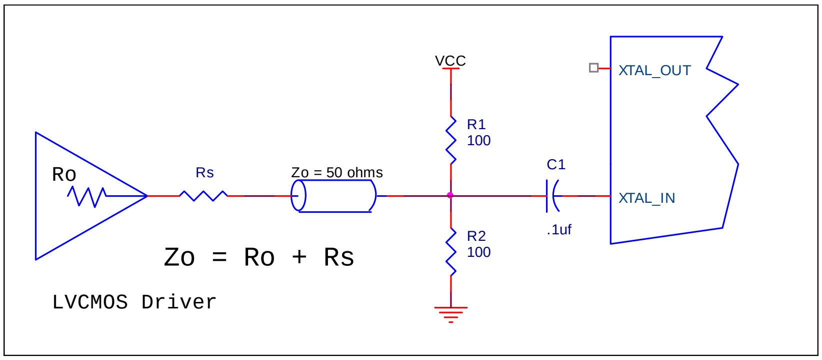


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

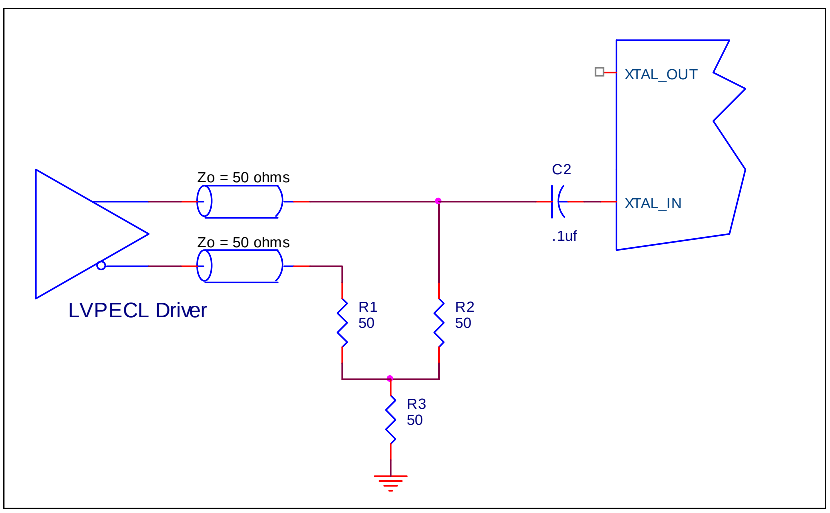


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Layout

Figure 2 shows an example of 840024I application schematic. In this example, the device is operated at $V_{DD} = V_{DDO} = 3.3V$. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will required adjusting C1 and C2.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 840024I provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

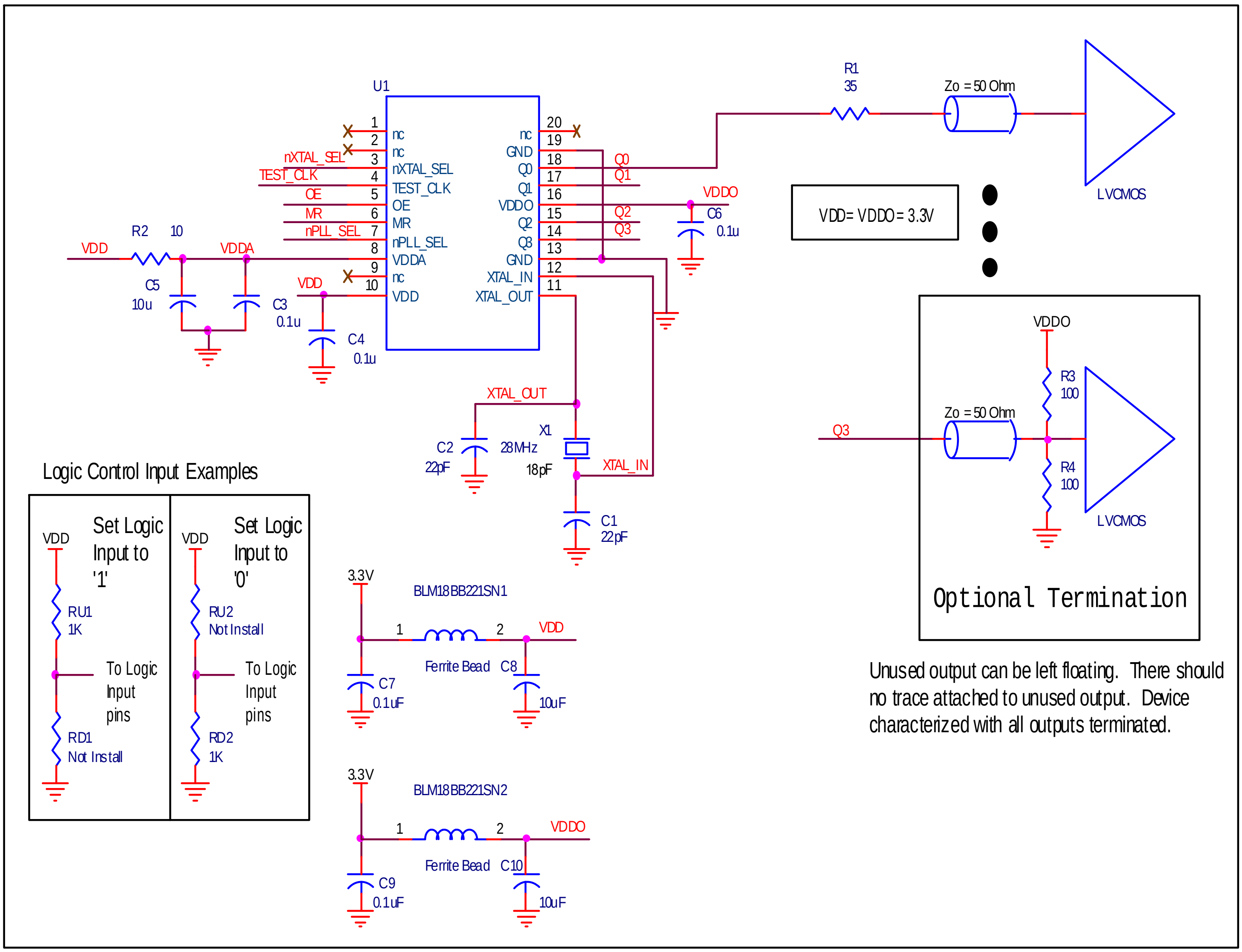


Figure 2. 840024I Application Schematic

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

Power Considerations

This section provides information on power dissipation and junction temperature for the 840024I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 840024I is the sum of the core power plus the analog power plus the output power dissipated into the load. The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX}$ = V_{DD_MAX} * (I_{DD} + I_{DDA} + I_{DDO}) = 3.465V *(90mA + 14mA + 8mA) = **388.1mW**

Dynamic Power Dissipation at 125MHz

Power (125MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 8pF * 125MHz * $(3.465V)^2$ = **12mW per output**

Total Power (125MHz) = 12mW * 4 = **48mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Power (125MHz)
  = 388.1mW + 48mW
  = 436.1mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.436W *86.7°C/W = 122.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Transistor Count

The transistor count for ICS40024I is: 3093

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

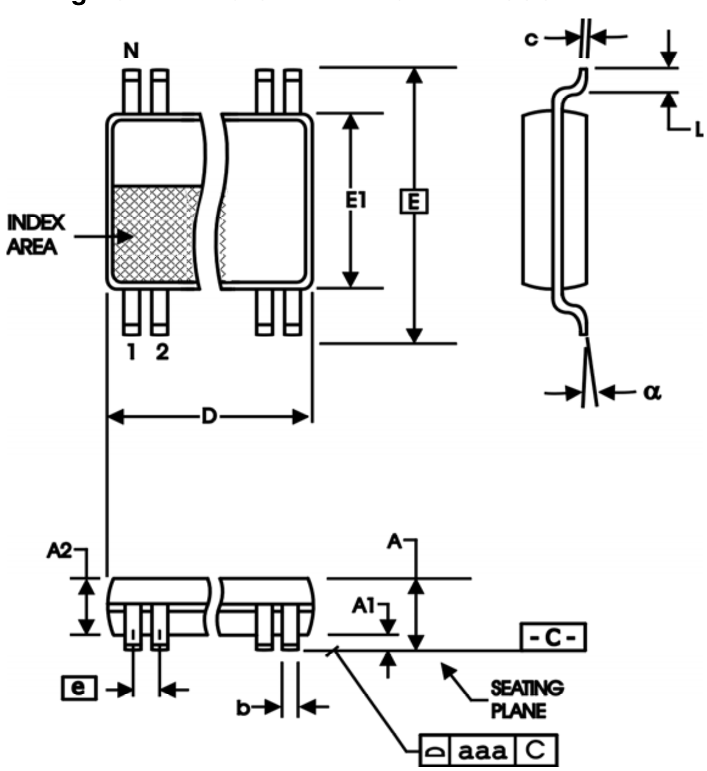


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840024BGILF	ICS840024BIL	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
840024BGILFT	ICS840024BIL	“Lead-Free” 20 Lead TSSOP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	Block Diagram - corrected nXTAL_SEL to select XTAL when LOW (0) and select TEST_CLK when HIGH (1).	8/30/2012
C	4A - 4C 6A - 6C	4 6	Output Supply Current, Test Conditions: Added 'No Load'. Added NOTE: Use XTAL input.	12/6/12
C	Features 4A - 4C 6A - 6C	1 4 6 13	Deleted 17Ω Output Impedance. RMS Phase Jitter from 0.604ps to 0.6ps I_{DDA} from 12mA to 14mA Deleted NOTE: Use XTAL input. Added NOTE: Characterized with crystal input. Updated Power Considerations for 14mA	1/11/13
C			Updated data sheet format.	4/3/15

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/