NEC

MOS INTEGRATED CIRCUIT

μPD43256B-X

256K-BIT CMOS STATIC RAM
32K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD43256B-X is a high speed, low power, and 262, 144 bits (32,768 words by 8 bits) CMOS static RAM. This device is an extended-operating-temperature version of the μPD43256B (X version, –25 to +85 °C). And A and B versions are wide voltage operations. Battery backup is available.

The μPD43256B-X is packed in 28-pin plastic TSOP (I).

Features

- 32,768 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Extended temperature (X version: T_A = –25 to +85 °C)
- Wide voltage range (A version: V_{CC} = 3.0 to 5.5 V, B version: V_{CC} = 2.7 to 5.5 V)
- 2 V data retention
- $\overline{OE}$ input for easy application

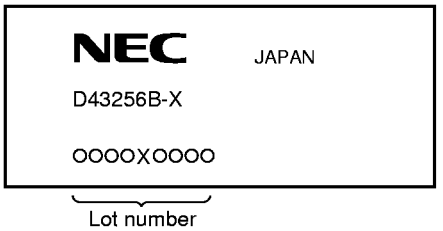
Part number	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Standby supply current μA (MAX.)	Data retention supply current[Note 1] μA (MAX.)
μPD43256B-X	70, 85, 100	4.5 to 5.5	–25 to +85	50	2
★ μPD43256B-AX	85[Note 2], 100, 120[Note 2]	3.0 to 5.5			
★ μPD43256B-BX	100, 120[Note 2], 150[Note 2]	2.7 to 5.5			

Notes 1. $T_A \leq 40$ °C, V_{CC} = 3 V

★ **2.** 100 ns (MAX.) (V_{CC} = 4.5 to 5.5 V)

★ Version X (DIP, SOP, TSOP (I))

This data sheet can be applied to the version X (DIP, SOP, TSOP (I)). Each version is identified with its lot number. Letter X in the fifth character position in a lot number signifies version X.



The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

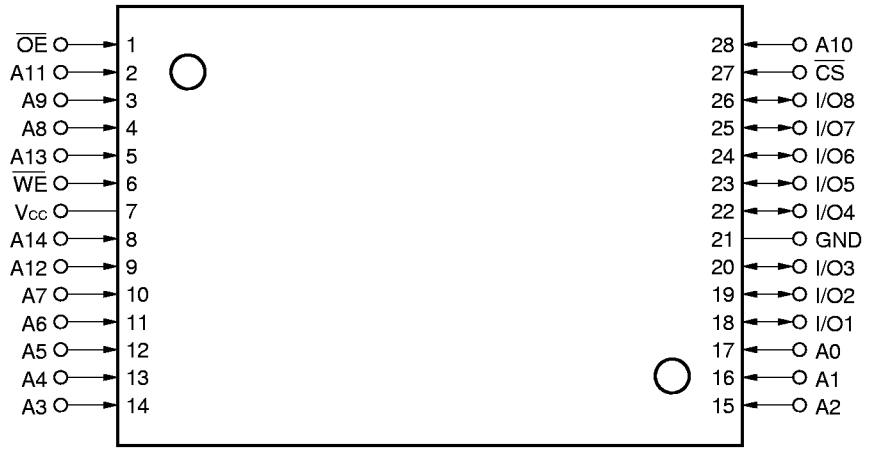
Ordering Information

	Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
	μPD43256BGW-70X-9JL	28-pin plastic TSOP (I) (8 × 13.4 mm) (Normal bent)	70	4.5 to 5.5	–25 to +85	
	μPD43256BGW-85X-9JL		85			
	μPD43256BGW-10X-9JL		100			
★	μPD43256BGW-A85X-9JL		85	3.0 to 5.5		A version
	μPD43256BGW-A10X-9JL		100			
	μPD43256BGW-A12X-9JL		120			
★	μPD43256BGW-B10X-9JL		100	2.7 to 5.5		B version
	μPD43256BGW-B12X-9JL		120			
	μPD43256BGW-B15X-9JL		150			
	μPD43256BGW-70X-9KL	28-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)	70	4.5 to 5.5		
	μPD43256BGW-85X-9KL		85			
	μPD43256BGW-10X-9KL		100			
★	μPD43256BGW-A85X-9KL		85	3.0 to 5.5		A version
	μPD43256BGW-A10X-9KL		100			
	μPD43256BGW-A12X-9KL		120			
★	μPD43256BGW-B10X-9KL		100	2.7 to 5.5		B version
	μPD43256BGW-B12X-9KL		120			
	μPD43256BGW-B15X-9KL		150			

Pin Configuration (Marking Side)

28-pin plastic TSOP (I) (8 × 13.4mm) (Normal bent)

[μPD43256BGW-X-9JL]

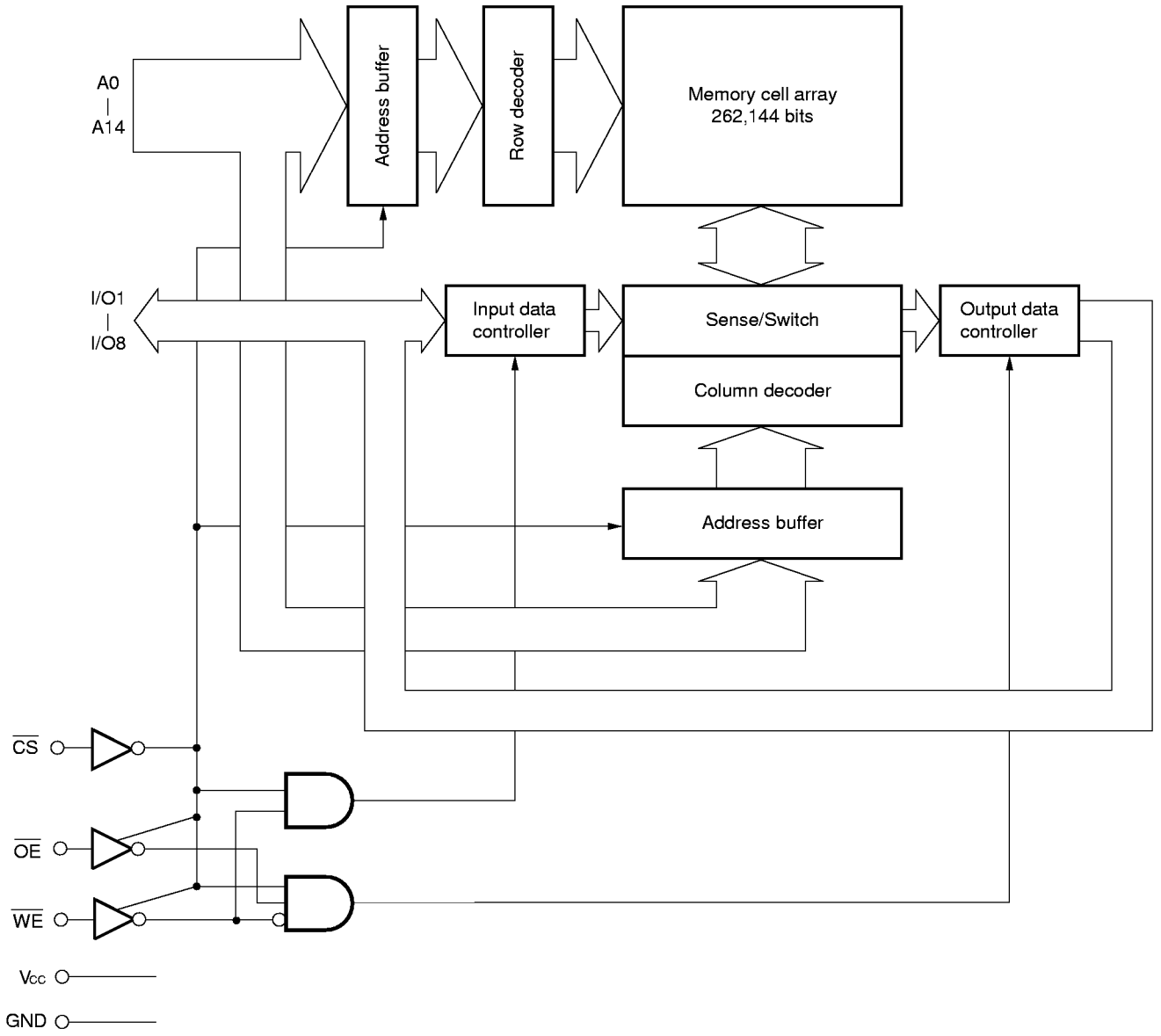


28-pin plastic TSOP (I) (8 × 13.4mm) (Reverse bent)

[μPD43256BGW-X-9KL]

A0 - A14 : Address Input
I/O1 - I/O8 : Data Input/Output
$\overline{CS}$: Chip Select Input
$\overline{WE}$: Write Enable Input
$\overline{OE}$: Output Enable Input
V_{CC} : Power Supply
GND : Ground

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
L	H	H	Output disable		I_{CCA}
L	×	L	Write	D_{IN}	
L	L	H	Read	D_{OUT}	

Remark ×: Don't care

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5[Note] to +7.0	V
Input/Output voltage	V_T	−0.5[Note] to V_{CC} + 0.5	V
Operating ambient temperature	T_A	−25 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note −3.0 V (MIN.) (Pulse width 50 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μPD43256B-X		μPD43256B-AX		μPD43256B-BX		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}	4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	V_{IH}	2.4	V_{CC} + 0.5	2.4	V_{CC} + 0.5	2.4	V_{CC} + 0.5	V
Low level input voltage	V_{IL}	−0.3[Note]	+0.6	−0.3[Note]	+0.4	−0.3[Note]	+0.4	V
Operating ambient temperature	T_A	−25	+85	−25	+85	−25	+85	°C

Note −3.0 V (MIN.) (Pulse width 50 ns)

★ **DC Characteristics (Recommended operating conditions unless otherwise noted) (1/2)**

Parameter	Symbol	Test condition		μPD43256B-X			Unit
				MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		−1.0		+1.0	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC} $\overline{OE}$ = V_{IH} or $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}		−1.0		+1.0	μA
Operating supply current	I_{CCA1}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Minimum cycle time	μPD43256B-70X			45	mA
			μPD43256B-85X			45	
			μPD43256B-10X			40	
	I_{CCA2}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA				15	
	I_{CCA3}	$\overline{CS}$ ≤ 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} − 0.2 V				15	
Standby supply current	I_{SB}	$\overline{CS}$ = V_{IH}				3	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2 V			1.0	50	μA
High level output voltage	V_{OH1}	I_{OH} = −1.0 mA		2.4			V
	V_{OH2}	I_{OH} = −0.1 mA		V_{CC} − 0.5			
Low level output voltage	V_{OL}	I_{OL} = +2.1 mA				0.4	V

Remarks 1. V_{IN}: Input voltage

2. These DC characteristics are in common regardless of package types.

DC Characteristics (Recommended operating conditions unless otherwise noted) (2/2)

Parameter	Symbol	Test conditions		μPD43256B-AX			μPD43256B-BX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		−1.0		+1.0	−1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC} $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}		−1.0		+1.0	−1.0		+1.0	μA
★ Operating supply current	I_{CCA1}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA Minimum cycle time	μPD43256B-A85X			45			–	mA
			μPD43256B-A10X			40			–	
			μPD43256B-A12X			40			–	
			μPD43256B-B10X			–			40	
			μPD43256B-B12X			–			40	
			μPD43256B-B15X			–			40	
			V_{CC} ≤ 3.3 V			–			25	
	I_{CCA2}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA				15			15	
			V_{CC} ≤ 3.3 V						10	
	I_{CCA3}	$\overline{CS}$ ≤ 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} − 0.2 V				15			15	
			V_{CC} ≤ 3.3 V			–			10	
Standby supply current	I_{SB}	$\overline{CS}$ = V_{IH}				3			3	mA
			V_{CC} ≤ 3.3 V			–			2	
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2 V			1.0	50		1.0	50	μA
			V_{CC} ≤ 3.3 V			–			25	
High level output voltage	V_{OH1}	I_{OH} = −1.0 mA, V_{CC} ≥ 4.5 V		2.4			2.4			V
		I_{OH} = −0.5 mA, V_{CC} < 4.5 V		2.4			2.4			
	V_{OH2}	I_{OH} = −0.02 mA		V_{CC} − 0.1			V_{CC} − 0.1			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} ≥ 4.5 V				0.4			0.4	V
		I_{OL} = 1.0 mA, V_{CC} < 4.5 V				0.4			0.4	
	V_{OL1}	I_{OL} = 0.02 mA				0.1			0.1	

Remarks 1. V_{IN}: Input voltage

2. These DC characteristics are in common regardless of package types.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			5	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF

Remarks 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

AC Characteristics (Recommended operating conditions unless otherwise noted)

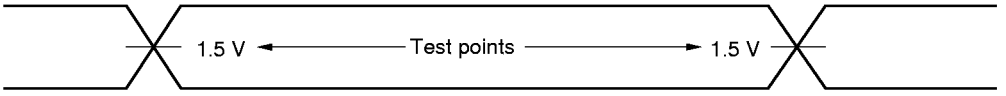
AC Test Conditions

Input waveform (Rise/fall time ≤ 5 ns)

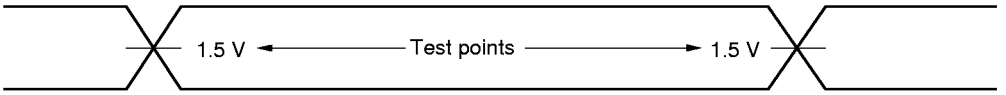
Input pulse levels

0.6 V to 2.4 V: μPD43256B-X

0.4 V to 2.4 V: μPD43256B-AX, 43256B-BX



Output waveform



Output load

μPD43256B-AX, 43256B-BX : 1TTL + 50 pF

μPD43256B-X : AC characteristics with notes should be measured with the output load shown in **Figure 1** and **Figure 2**.

Figure 1

(For t_{AA}, t_{ACS}, t_{OE}, t_{OH})

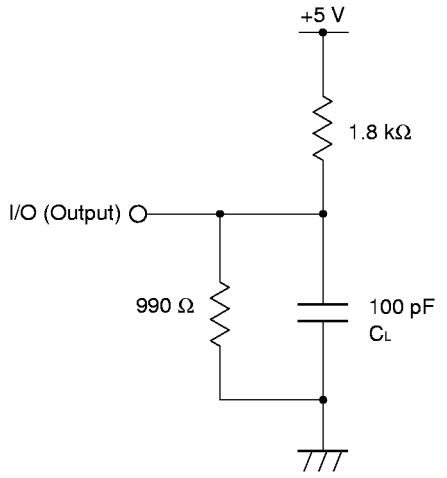
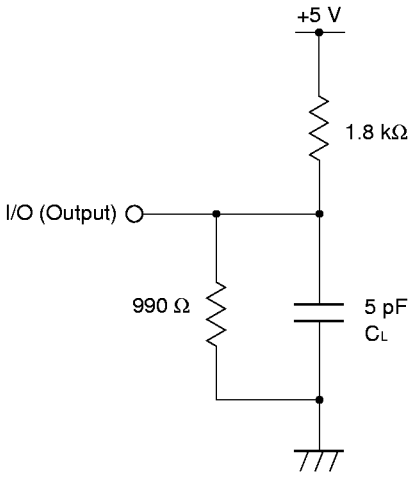


Figure 2

(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle (1/3)

Parameter	Symbol	$V_{CC} \geq 4.5$ V						Unit	Condition
		μPD43256B-70X		μPD43256B-85X		μPD43256B-10X μPD43256B-A85X/A10X/A12X μPD43256B-B10X/B12X/B15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note 1**
$\overline{CS}$ access time	t_{ACS}		70		85		100	ns	
$\overline{OE}$ access time	t_{OE}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	10		10		10		ns	**Note 2**
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		30		30		35	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		30		30		35	ns	

Notes 1. See the output load shown in **Figure 1** except for μPD43256B-AX, 43256B-BX.

2. See the output load shown in **Figure 2** except for μPD43256B-AX, 43256B-BX.

★ **Read Cycle (2/3)**

Parameter	Symbol	$V_{CC} \geq 3.0$ V						Unit	Condition
		μPD43256B-A85X		μPD43256B-A10X		μPD43256B-A12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85		100		120		ns	
Address access time	t_{AA}		85		100		120	ns	**Note**
$\overline{CS}$ access time	t_{ACS}		85		100		120	ns	
$\overline{OE}$ access time	t_{OE}		50		60		60	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	10		10		10		ns	
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		35		35		40	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		35		35		40	ns	

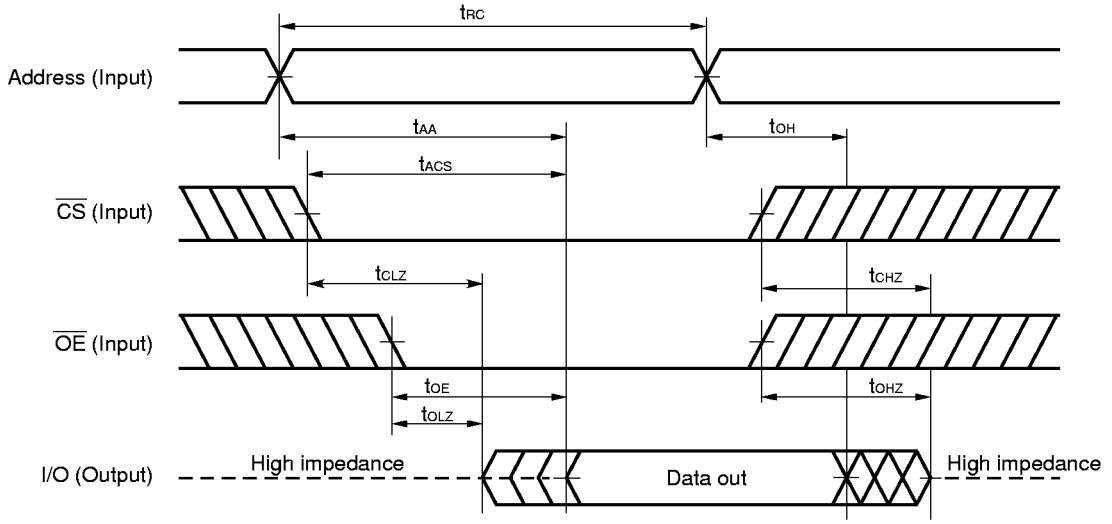
Note Loading condition is 1TTL + 50 pF.

★ **Read Cycle (3/3)**

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD43256B-B10X		μPD43256B-B12X		μPD43256B-B15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		150		ns	
Address access time	t_{AA}		100		120		150	ns	**Note**
$\overline{CS}$ access time	t_{ACS}		100		120		150	ns	
$\overline{OE}$ access time	t_{OE}		60		60		70	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	10		10		10		ns	
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		35		40		50	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		35		40		50	ns	

Note Loading condition is 1TTL + 50 pF.

Read Cycle Timing Chart



Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle (1/3)

Parameter	Symbol	$V_{CC} \geq 4.5$ V						Unit	Condition
		μPD43256B-70X		μPD43256B-85X		μPD43256B-10X μPD43256B-A85X/A10X/A12X μPD43256B-B10X/B12X/B15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
$\overline{CS}$ to end of write	t_{CW}	60		70		80		ns	
Address valid to end of write	t_{AW}	60		70		80		ns	
★ Write pulse width	t_{WP}	55		60		70		ns	
Data valid to end of write	t_{DW}	30		35		40		ns	
Data hold time	t_{DH}	5		5		5		ns	
Address setup time	t_{AS}	0		0		0		ns	
★ Write recovery time	t_{WR}	0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		30		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note See the output load shown in **Figure 2** except for μPD43256B-AX, 43256B-BX.

★ **Write Cycle (2/3)**

Parameter	Symbol	$V_{CC} \geq 3.0$ V						Unit	Condition
		μPD43256B-A85X		μPD43256B-A10X		μPD43256B-A12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85		100		120		ns	
$\overline{CS}$ to end of write	t_{CW}	70		70		90		ns	
Address valid to end of write	t_{AW}	70		70		90		ns	
Write pulse width	t_{WP}	60		60		80		ns	
Data valid to end of write	t_{DW}	60		60		70		ns	
Data hold time	t_{DH}	5		5		5		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		35		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

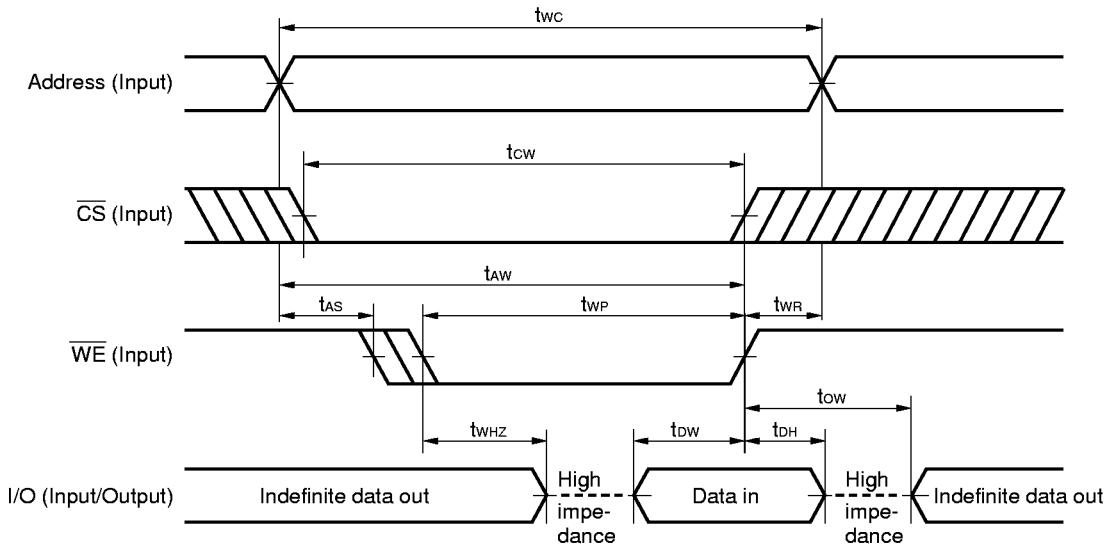
Note Loading condition is 1TTL + 50 pF.

★ **Write Cycle (3/3)**

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD43256B-B10X		μPD43256B-B12X		μPD43256B-B15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		150		ns	
$\overline{CS}$ to end of write	t_{CW}	70		90		100		ns	
Address valid to end of write	t_{AW}	70		90		100		ns	
Write pulse width	t_{WP}	60		80		90		ns	
Data valid to end of write	t_{DW}	60		70		80		ns	
Data hold time	t_{DH}	5		5		5		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		35		40		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note Loading condition is 1TTL + 50 pF.

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



Cautions 1. $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

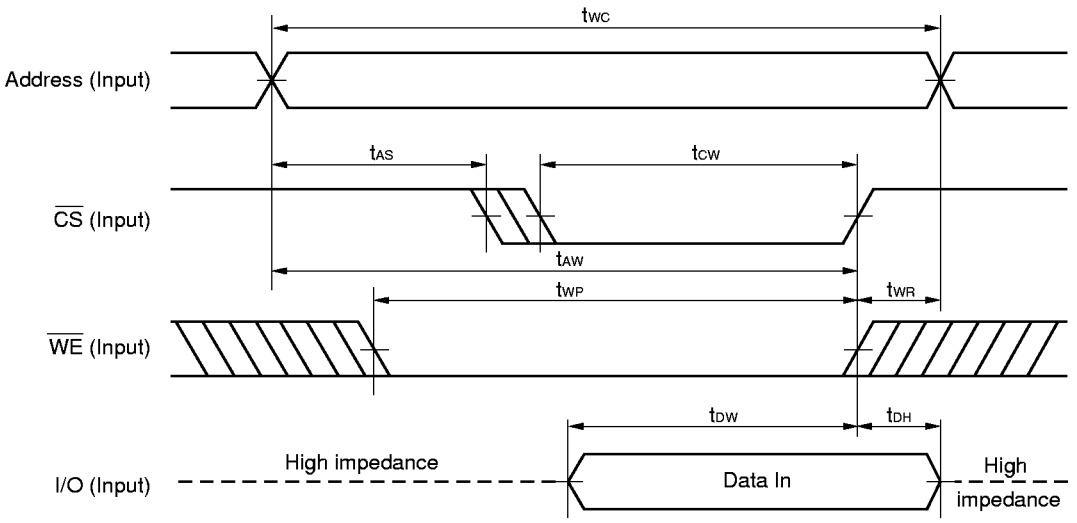
★ **2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.**

Remarks 1. Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

2. When $\overline{WE}$ is at low level, the I/O pins are always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.

3. If $\overline{CS}$ changes to low level at the same time or after the change of $\overline{WE}$ to low level, the I/O pins will remain high impedance state.

Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)



Cautions 1. $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

★ **2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.**

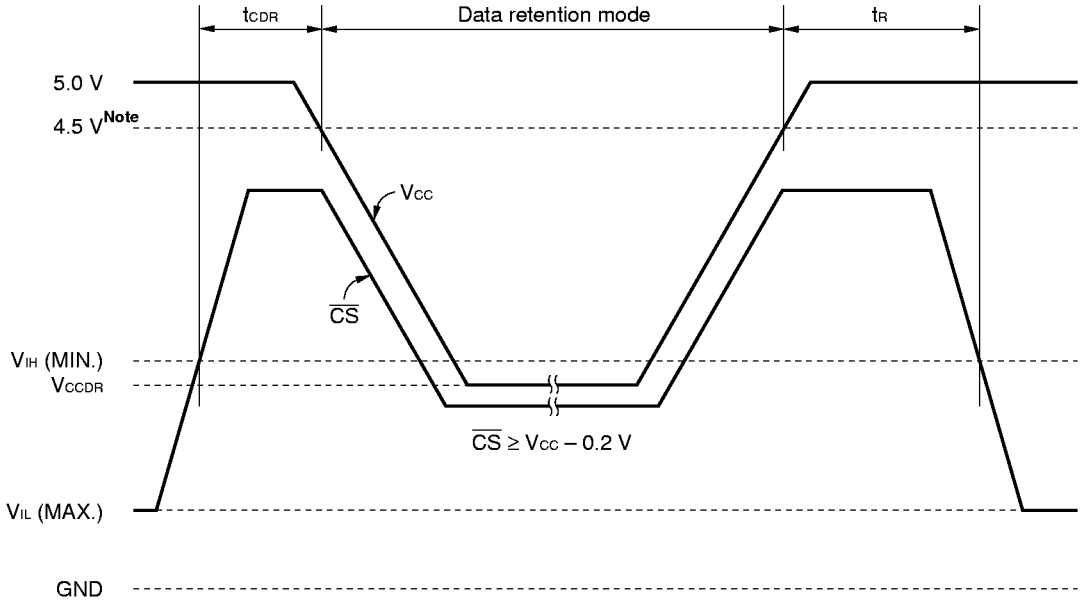
Remark Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR}	$\overline{CS} \geq V_{CC} - 0.2$ V	2.0		5.5	V
Data retention supply current	I_{CCDR}	V_{CC} = 3.0 V, $\overline{CS} \geq V_{CC} - 0.2$ V		0.5	20[Note]	μA
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 2 μA ($T_A \leq$ 40 °C), 7 μA ($T_A \leq$ 70 °C)

Data Retention Timing Chart

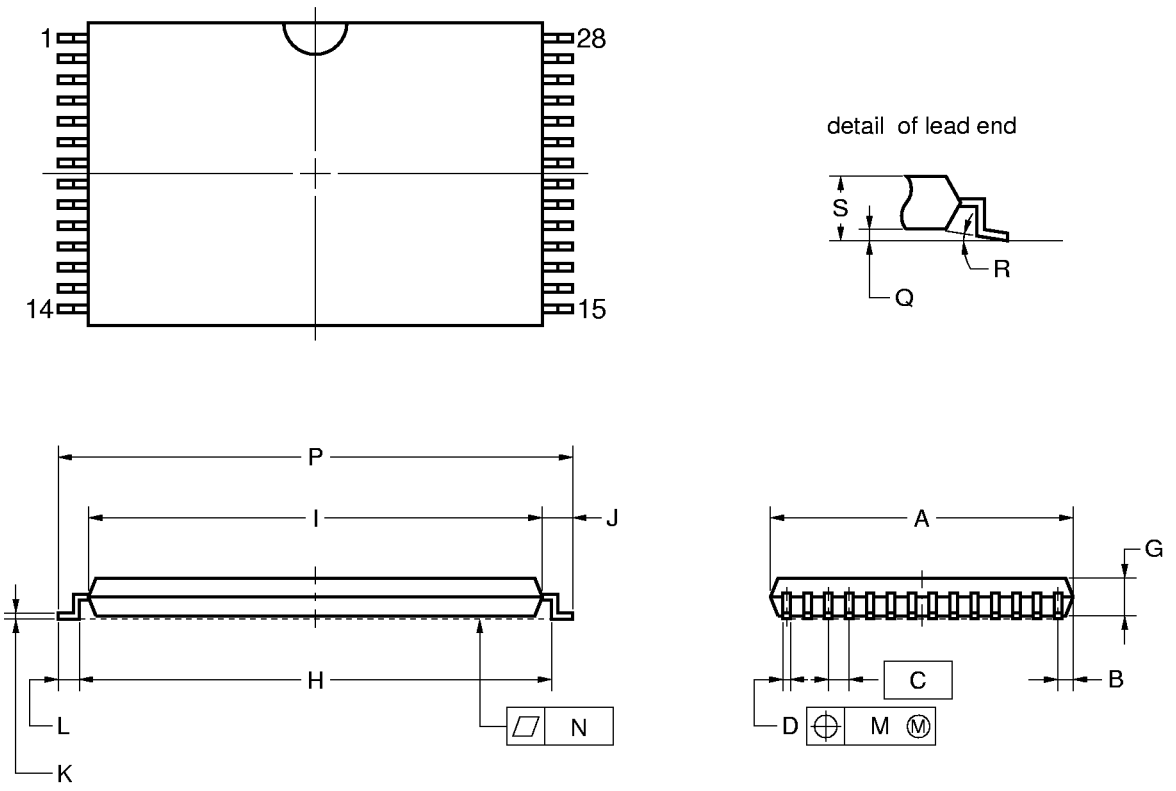


Note A Version: 3.0 V, B Version: 2.7 V

Remark The other pins (address, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance state.

Package Drawings

28PIN PLASTIC TSOP (I) (8×13.4)



NOTE

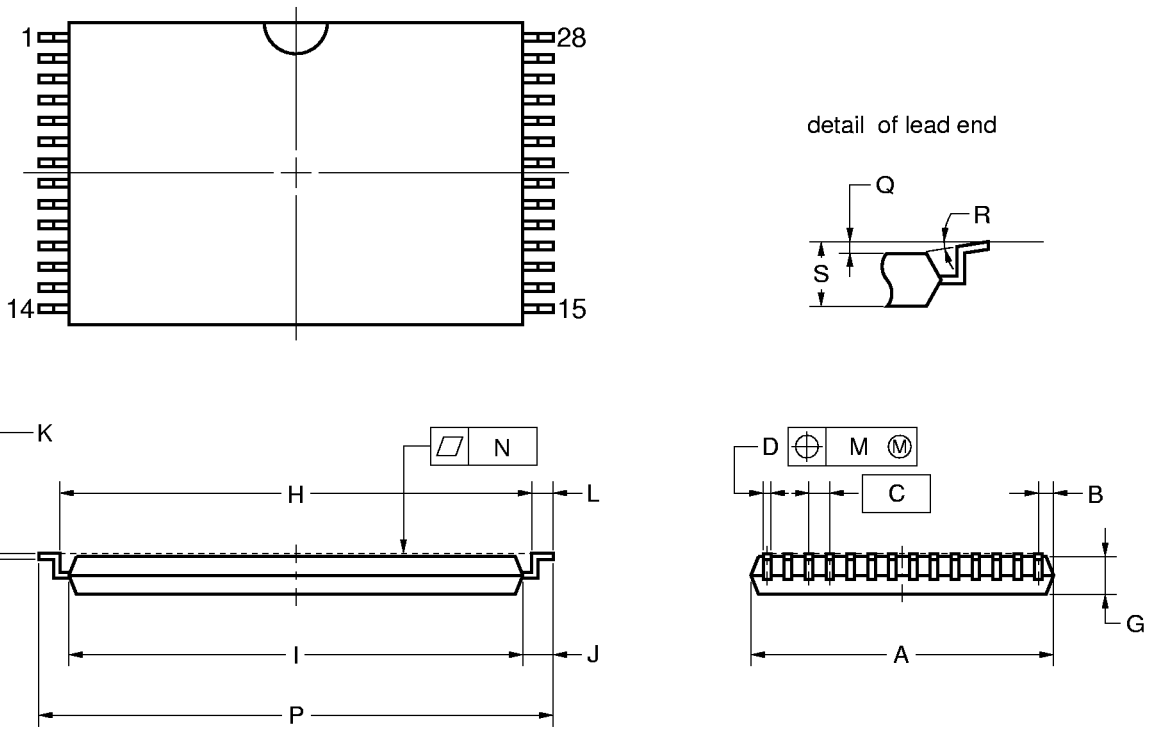
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.4mm MAX. <0.331 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.6 MAX.	0.024 MAX.
C	0.55 (T.P.)	0.022 (T.P.)
D	$0.22^{+0.08}_{-0.07}$	0.009±0.003
G	1.0	0.039
H	12.4±0.2	0.488±0.008
I	11.8±0.1	$0.465^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	13.4±0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1±0.05	0.004±0.002
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.2 MAX.	0.048 MAX.

P28GW-55-9JL-1

28PIN PLASTIC TSOP (I) (8×13.4)



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Q	0.1±0.05	0.004±0.002
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.2 MAX.	0.048 MAX.

P28GW-55-9KL-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD43256B-X.

Types of Surface Mount Device

μPD43256BGW-X-9JL : 28-pin Plastic TSOP (I) (8 × 13.4 mm) (Normal bent)
μPD43256BGW-X-9KL : 28-pin Plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)