BX Spread Spectrum Frequency Synthesizer for Pentium II®

Features

- Maximized EMI suppression using IC WORKS' Spread Spectrum Technology
- Single chip system frequency synthesizer for Intel BX chip set
- Two copies of CPU output
- Six copies of PCI output
- One 48MHz output for USB
- One 24MHz output for SIO
- Two buffered reference outputs
- One IOAPIC output
- Thirteen SDRAM outputs provide support for 3 DIMMs
- Supports frequencies up to 133MHz
- I^2C interface for programming
- Power management control inputs
- Smooth CPU frequency switching from 66.8–133MHz

Key Specifications

CPU Cycle-to-Cycle Jitter:	250ps
CPU to CPU Output Skew:	175ps
PCI to PCI Output Skew:	500ps
VDDQ3 =	3.3V±5%
VDDQ2 =	2.5V±5%
SDRAMIN to SDRAM0:12 Delay:	3.7nS typ.

Figure 1 Block Diagram

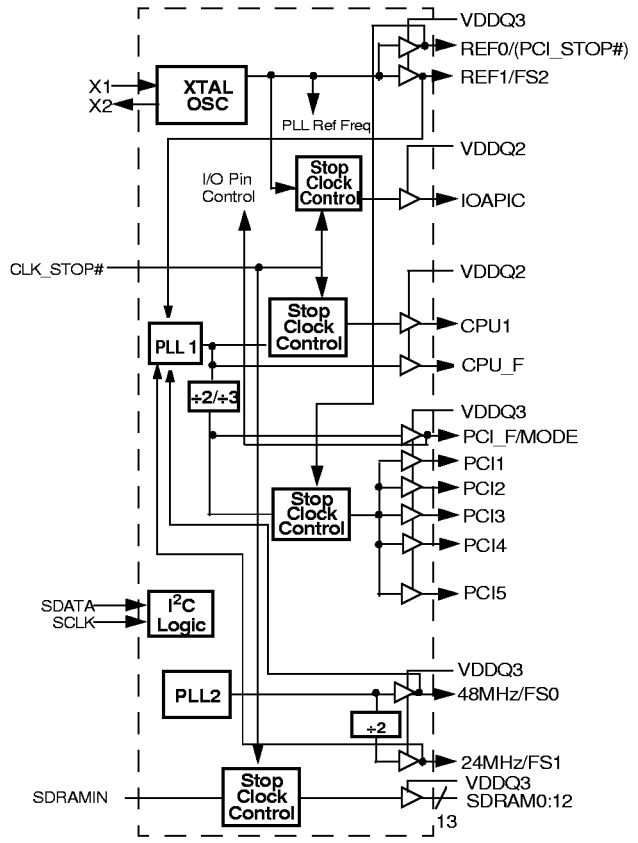


Table 1 Order Information

Part Number	Freq. Mask Code	Package
W138	-39	H = SSOP (300 mils)

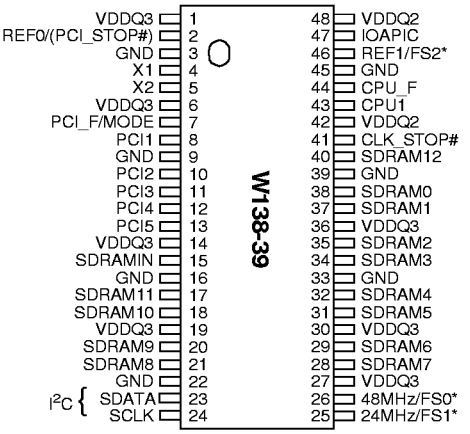
Table 2 Mode Input Table

Mode	Pin 3
0	PCI_STOP#
1	REF0

Table 3 Pin Selectable Frequency

Input Address			CPU Outputs	PCI Outputs
FS2	FS1	FS0	(MHz)	(MHz)
1	1	1	100	33.3 (CPU/3)
1	1	0	133.3	44.4 (CPU/3)
1	0	1	112	37.3 (CPU/3)
1	0	0	103	34.3 (CPU/3)
0	1	1	66.8	33.4 (CPU/2)
0	1	0	83.3	41.7 (CPU/2)
0	0	1	75	37.5 (CPU/2)
0	0	0	124	41.3 (CPU/3)

Figure 2 Pin Diagram



Note: Internal pull up resistors should not be relied upon for setting I/O pins high. Pin function with parentheses determined by MODE pin resistor strapping.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU_F	44	O	***Free-running CPU Clock:*** Output voltage swing is controlled by the voltage applied to VDDQ2. See Tables 3 and 7 for detailed frequency information.
CPU1	43	O	***CPU Clock Output 1:*** This CPU clock output is controlled by the CLK_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI1:5	8, 10, 11, 12, 13	O	***PCI Clock Outputs 1 through 5:*** These five PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F/MODE	7	I/O	***Fixed PCI Clock Output:*** Frequency is set by the FS0:1 inputs or through serial input interface, see Tables 3 and 7. This output is not affected by the PCI_STOP# input.
CLK_STOP#	41	I	***CLK_STOP# input:*** When brought low, affected clock outputs are stopped low after completing a full clock cycle (2-3 CPU clock latency). When brought high, affected clock outputs start, beginning with a full clock cycle (2-3 CPU clock latency).
IOAPIC	47	O	***IOAPIC Clock Output:*** Provides 14.318MHz fixed frequency. The output voltage swing is controlled by VDDQ2. This output is disabled when CLK_STOP# is set low.
48MHz/FS0	26	I/O	***48MHz Output:*** 48MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power-up FS0 input will be latched, which will set clock frequencies as described in Table 3.
24MHz/FS1	25	I/O	***24MHz Output:*** 24MHz is provided in normal operation. In standard systems, this output can be used as the clock input for a Super I/O chip.Upon power-up FS1 input will be latched, which will set clock frequencies as described in Table 3.
REF1/FS2	46	I/O	***I/O Dual Function REF0 and FS2 pin:*** Upon power-up, FS2 input will be latched which will set clock frequencies as described in Table 3. When an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins.
REF0/ (PCI_STOP#)	2	I/O	***Fixed 14.318MHz Output 0 or PCI_STOP# Pin:*** Function determined by MODE pin. The PCI_STOP# input enables the PCI 1:5 outputs when high and causes them to remain at logic 0 when low. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effects take place on the next PCI_F clock cycle. When an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins.
SDRAMIN	15	I	**Buffered Input Pin:** The signal provided to this input pin is buffered to 13 outputs (SDRAM0:12).
SDRAM0:12	38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17, 40	O	**Buffered Outputs:** These thirteen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3, and they are deactivated when CLK_STOP# input is set low.
SCLK	24	I	Clock pin for I^2C Circuitry.
SDATA	23	I/O	Data pin for I^2C Circuitry.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input.
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	1, 6, 14, 19, 27, 30, 36	P	***Power Connection:*** Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48MHz output, and 24MHz output. Connect to 3.3V supply
VDDQ2	42, 48	P	***Power Connection:*** Power supply for IOAPIC, CPU_F, and CPU1 output buffers. Connect to 2.5V.
GND	3, 9, 16, 22, 33, 39, 45	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Overview

The W138-39 was developed as a single chip device to meet the clocking needs of the Intel BX™ chipset. In addition to the typical outputs provided by standard 100 MHz BX™ FTG's, the W138-39 adds a thirteenth output buffer, supporting SDRAM DIMM modules in conjunction with the chipset.

IC WORKS proprietary spread spectrum frequency synthesis technique is a feature of the CPU and PCI outputs. When enabled, this feature reduces the peak EMI measurements of not only the output signals and their harmonics, but also of any other clock signals that are properly synchronized to them.

Functional Description

I/O Pin Operation

Pins 7, 25, 26, 46 are dual purpose I/O pins. Upon power up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power up, the logic state of each pin is latched and the pins become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10k ohm "strapping" resistor is connected between the I/O pin and ground or VDD. Connection to ground sets a latch to '0'; connection to VDD sets a latch to '1'. Figure 3 and Figure 7 show two suggested methods for strapping resistor connections.

Upon W138-39 power up, the first 2ms of operation is used for input logic selection. During this period, the four I/O pins(7, 25, 26, 46) are tristated, allowing the output strapping resistor on the I/O pins to pull the pin and their associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic '0' or '1' condition of the I/O pin is latched. Next the output buffer is enabled which converts the I/O pins into operating clock outputs. The 2ms timer is started when VDD reaches 2.0V. The input bits can only be re-set by turning VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is <40 ohms (nominal) which is minimally affected by the 10k ohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2ms input period, the specified output frequency is delivered on the pin, assuming that VDD has stabilized. If VDD has not yet reached full value, output frequency initially may be below target but will increase to target once VDD voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Figure 3 Input Logic Selection Through Resistor Load Option

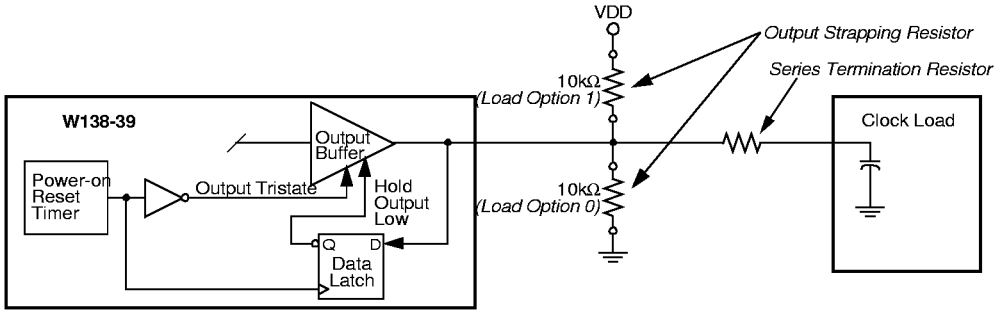
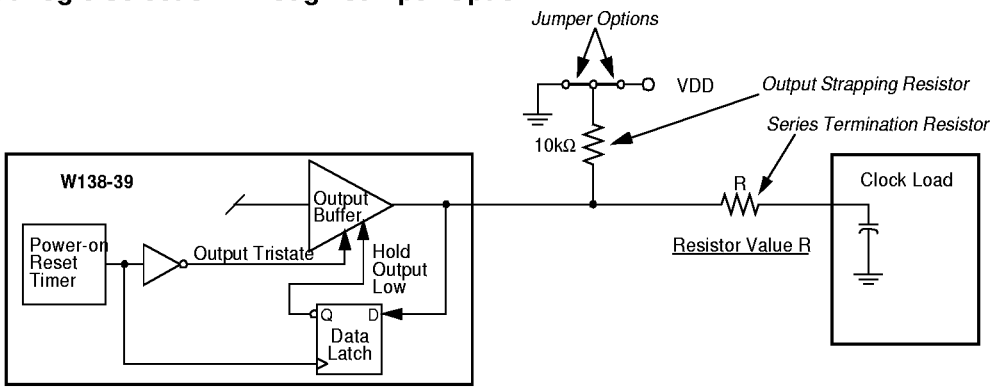


Figure 4 Input Logic Selection Through Jumper Option



Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in Figure 5.

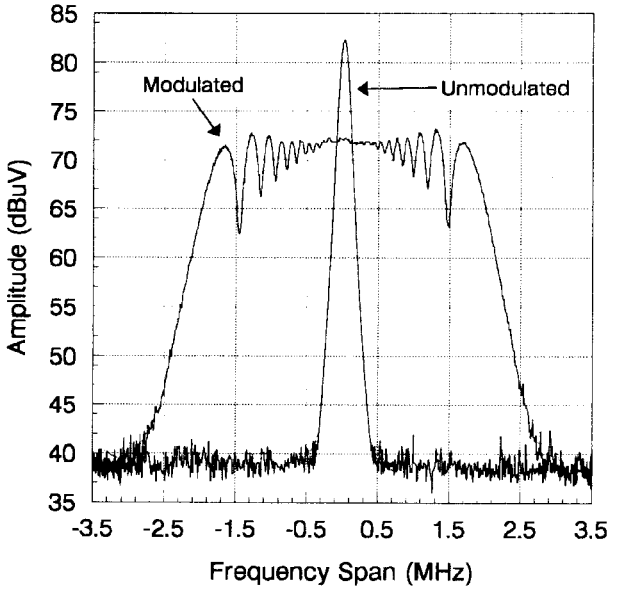
As shown in Figure 5, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and*F* is the frequency in MHz where the reduction is measured.

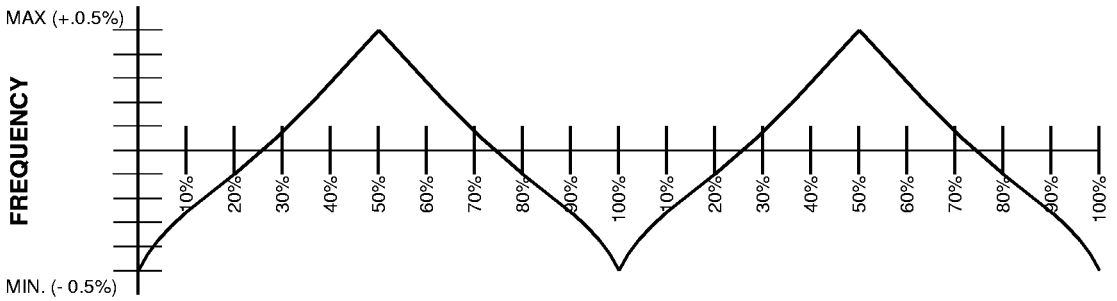
The output clock is modulated with a waveform depicted in Figure 6. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is± 0.5% of the center frequency. Figure 6 details the IC WORKS spreading pattern. IC WORKS does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Figure 5 Clock Harmonic with and without SSCG Modulation Frequency Domain Representation



Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1-0 in data byte 0 of the I²C data stream. Refer to Table 8 for more details.

Figure 6 Typical Modulation Profile



Serial Data Interface

The W138-39 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W138-39 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 4 summarizes the control functions of the serial data interface.

Table 4 Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
Output Tristate	Puts clock output into a high impedance state.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Operation

Data is written to the W138-39 in eleven bytes of eight bits each. Bytes are written in the order shown in Table 5.

Table 5 Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W138-39 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W138-39 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Dont' Care	Unused by the W138-39, therefore bit values are ignored (dont' care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Dont' Care	Unused by the W138-39, therefore bit values are ignored (dont' care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 6	The data bits in Data Bytes 0-7 set internal W138-39 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 6, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		
11	Data Byte 7		

Writing Data Bytes

Each bit in Data Bytes 0-7 control a particular device function except for the "reserved" bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. Table 6 gives the bit formats for registers located in Data Bytes 0-7.

Table 7 details additional frequency selections that are available through the serial data interface.

Table 8 details the select functions for Byte 0, bits 1 and 0.

Table 6 Data Bytes 0-7 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL_2	See Table 7		0
5	--	--	SEL_1	See Table 7		0
4	--	--	SEL_0	See Table 7		0
3	--	--	Hardware/Software Frequency Select	Hardware	Software	0
2	--	--	(Reserved)	--	--	0
1-0	--	--	**Bit 1 / Bit 0 / Function (See Table 8 for function details)** 0 0 Normal Operation 0 1 (Reserved) 1 0 Spread Spectrum On 1 1 All Outputs Tristated			00
Data Byte 1						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	40	SDRAM12	Clock Output Disable	Low	Active	1
2	--	--	(Reserved)	--	--	0
1	43	CPU1	Clock Output Disable	Low	Active	1
0	44	CPU_F	Clock Output Disable	Low	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	7	PCI_F	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	13	PCI5	Clock Output Disable	Low	Active	1
3	12	PCI4	Clock Output Disable	Low	Active	1
2	11	PCI3	Clock Output Disable	Low	Active	1
1	10	PCI2	Clock Output Disable	Low	Active	1
0	8	PCI1	Clock Output Disable	Low	Active	1
Data Byte 3						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	26	48MHz	Clock Output Disable	Low	Active	1
4	25	24MHz	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0

Table 6 Data Bytes 0-7 Serial Configuration Map (cont.)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
2	21, 20, 18, 17	SDRAM8:11	Clock Output Disable	Low	Active	1
1	32, 31, 29, 28	SDRAM4:7	Clock Output Disable	Low	Active	1
0	38, 37, 35, 34	SDRAM0:3	Clock Output Disable	Low	Active	1
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 5						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	47	IOAPIC	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	46	REF1	Clock Output Disable	Low	Active	1
0	2	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 7						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 7 Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions			Output Frequency	
Data Byte 0, Bit 3 = 1				
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
1	1	1	100. 2	33.4
1	1	0	133.3	44.4
1	0	1	112	37.3
1	0	0	103	34.3
0	1	1	66.8	33.4
0	1	0	83.3	41.65
0	0	1	75	37.5
0	0	0	124	41.3

Table 8 Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditions				
	Data Byte 0		CPU_F, CPU1	PCI_F, PCI1:5	REF0:1, IOAPIC	48MHZ	24MHZ
	Bit 1	Bit 0					
Normal Operation	0	0	Note 1	Note 1	14.318MHz	48MHz	24MHz
Spread Spectrum	1	0	±0.5%	±0.5%	14.318MHz	48MHz	24MHz
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note 1. CPU and PCI frequency selections are listed in Table 3 and Table 7.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

DC Electrical Characteristics:

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
Supply Current							
I_{DD}	3.3V Supply Current			260		mA	CPU_F: CPU1 = 100MHz Outputs Loaded (Note 1)
I_{DD}	2.5V Supply Current			25		mA	CPU_F: CPU1 = 100MHz Outputs Loaded (Note 1)
Logic Inputs							
V_{IL}	Input Low Voltage		GND -.3		0.8	V	
V_{IH}	Input High Voltage		2.0		VDD +.3	V	
I_{IL}	Input Low Current (Note 2)				-25	µA	
I_{IH}	Input High Current (Note 2)				10	µA	
I_{IL}	Input Low Current (SEL100/66#)				-5	µA	
I_{IH}	Input High Current (SEL100/66#)				+5	µA	
Clock Outputs							
V_{OL}	Output Low Voltage				50	mV	I_{OL} = 1mA
V_{OH}	Output High Voltage		3.1			V	I_{OH} = 1mA
V_{OH}	Output High Voltage	CPU_F:1, IOPIC	2.2			V	I_{OH} = –1mA
I_{OL}	Output Low Current:	CPU_F, CPU1	27	57	97	mA	V_{OL} = 1.25V
		PCI_F, PCI1:5	20.5	53	139	mA	V_{OL} = 1.5V
		IOAPIC	40	85	140	mA	V_{OL} = 1.25V
		REF0:1	25	37	76	mA	V_{OL} = 1.5V
		48MHz	25	37	76	mA	V_{OL} = 1.5V
		24MHz	25	37	76	mA	V_{OL} = 1.5V
I_{OH}	Output High Current	CPU_F, CPU1	25	55	97	mA	V_{OH} = 1.25V

DC Electrical Characteristics: (cont.)

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

Symbol	Parameter		Min	Typ	Max	Unit	Test Condition
I_{OH}	Output High Current	PCI_F, PCI1:5	31	55	139	mA	V_{OH} = 1.5V
		IOAPIC	40	87	155	mA	V_{OH} = 1.25V
		REF0:1	27	44	94	mA	V_{OH} = 1.5V
		48MHz	27	44	94	mA	V_{OH} = 1.5V
		24MHz	25	37	76	mA	V_{OH} = 1.5V
Crystal Oscillator							
V_{TH}	X1 Input threshold Voltage (Note 3)			1.65		V	VDDQ3 = 3.3V
C_{LOAD}	Load Capacitance, Imposed on External Crystal (Note 4)			14		pF	
$C_{IN,X1}$	X1 Input Capacitance (Note 5)			28		pF	Pin X2 unconnected
Pin Capacitance/Inductance							
C_{IN}	Input Pin Capacitance				5	pF	Except X1 and X2
C_{OUT}	Output Pin Capacitance				6	pF	
L_{IN}	Input Pin Inductance				7	nH	

Notes:
1. All clock outputs loaded with 6" 60 ohm traces with 22pF capacitors.
2. W138-39 logic inputs have internal pull-up devices (pull-ups not full CMOS level).
3. X1 input threshold voltage (typical) is VDD/2.
4. The W138-39 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics:

T_A = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU_F, CPU1 (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.6MHz			CPU = 100MHz			Unit	Test Condition/Comments
		Min	Typ	Max	Min	Typ	Max		
t_P	Period	15		15.5	10		10.5	ns	Measured on rising edge at 1.25.
t_H	High Time	5.2			3.0			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5.0			2.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			200			200	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			175			175	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		20			20		ohm	Average value during switching transition. Used for determining series termination value

PCI Clock Outputs, PCI_F and PCI1:5 (Lump Capacitance Test Load = 30pF)

Symbol	Parameter	CPU = 66.6/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
t_H	High Time	12.0			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			500	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Skew	1.5		4.0	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.
f_{ST}	Frequency Stabilization from Power-up (cold start)				ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		30		ohm	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU = 66.6/100MHz			Unit	Test Condition/Comments
		Min	Typ	Max		
f	Frequency, Actual		14.31818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF) (cont.)

Symbol	Parameter	CPU = 66.6/100MHz Min	Typ	Max	Unit	Test Condition/Comments
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		15		ohm	Average value during switching transition. Used for determining series termination value.

REF0:1 Clock Output (Lump Capacitance Test Load = 20pF)

Symbol	Parameter	CPU =66.6/100MHz Min	Typ	Max	Unit	Test Condition/Comments
f	Frequency, Actual		14.318		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		40		ohm	Average value during switching transition. Used for determining series termination value.

48MHz Clock Output (Lump Capacitance Test Load = 20pF=66.6/100MHz

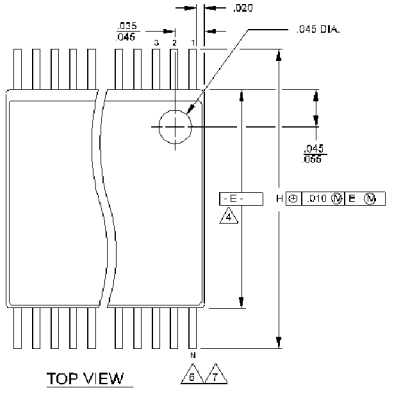
Symbol	Parameter	CPU = 66.6/100MHz Min	Typ	Max	Unit	Test Condition/Comments
f	Frequency, Actual		48.008		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
m/n	PLL Ratio		57/17			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		40		ohm	Average value during switching transition. Used for determining series termination value.

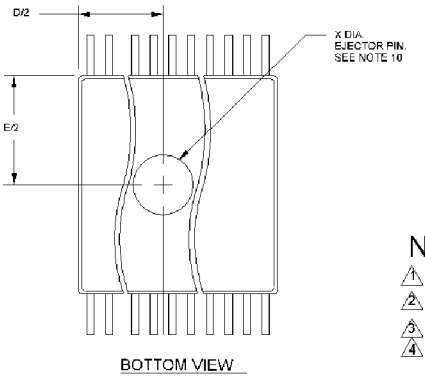
24MHz Clock Output (Lump Capacitance Test Load = 20pF=66.6/100MHz

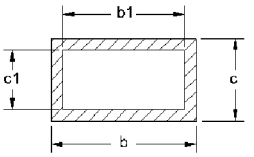
Symbol	Parameter	CPU = 66.6/100MHz Min	Typ	Max	Unit	Test Condition/Comments
f	Frequency, Actual		24.004		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 24MHz		+167		ppm	(24.004 – 24)/24
m/n	PLL Ratio		57/34			(14.31818MHz x 57/34 = 24.004MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up. Short cycles exist prior to frequency stabilization.
Z_o	AC Output Impedance		40		ohm	Average value during switching transition. Used for determining series termination value.

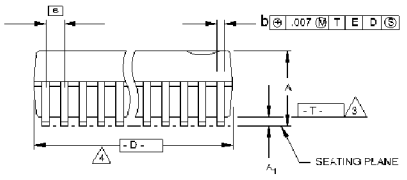
Mechanical Package Outlines

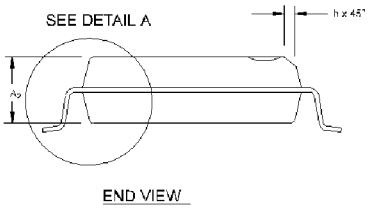
Figure 7 56-Pin Shrink Small Outline Package (SSOP, 300 mils)

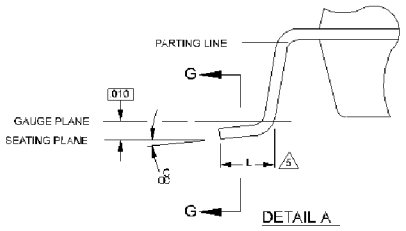












NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .005 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: .296
Lead Pitch: .025
Body Length: .625
Body Height: .102

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS