Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (16K x 1-BIT)

IDT 6167SA
IDT 6167LA

T-46-23-05

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
  - IDT6167SA
    Active: 200mW (typ.)
    Standby:100µW (typ.)
  - IDT6167LA
    Active: 150mW (typ.)
    Standby:10µW (typ.)
- Battery backup operation—2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and plastic DIP, 20-pin Flatpack or CERPACK, 20-pin SOIC and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-84132 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

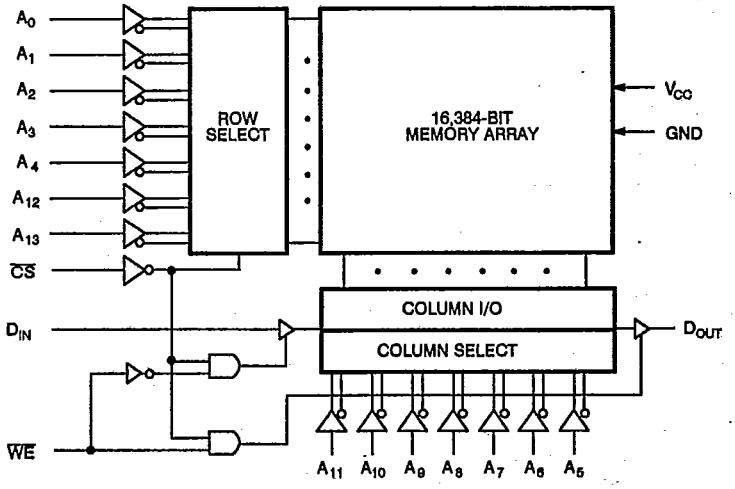
Access times as fast as 12ns are available with maximum power consumption of only 660mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, plastic 20-pin SOIC, 20-pin flatpack or CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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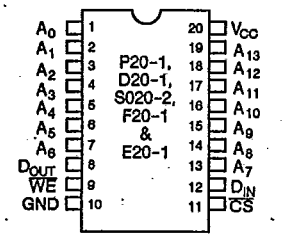
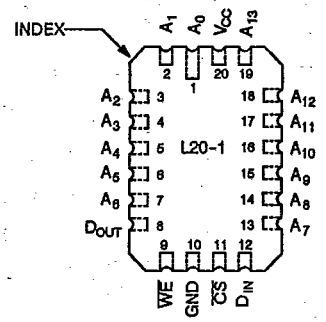
PIN CONFIGURATIONS

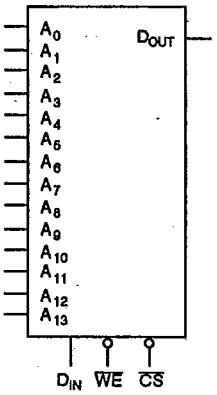


DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{13}	Address Inputs	D_{IN}	$DATA_{IN}$
$\overline{CS}$	Chip Select	D_{OUT}	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and funotional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT6167SA MIN.	IDT6167SA TYP.(1)	IDT6167SA MAX.	IDT6167LA MIN.	IDT6167LA TYP.(1)	IDT6167LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1) V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	6167SA12(4) COM'L.	6167SA12(4) MIL.	6167SA15 6167LA15 COM'L.	6167SA15 6167LA15 MIL.	6167SA20/25 6167LA20/25 COM'L.	6167SA20/25 6167LA20/25 MIL.	6167SA35 6167LA35 COM'L.	6167SA35 6167LA35 MIL.	6167SA45(5) 6167LA45(5) COM'L.	6167SA45(5) 6167LA45(5) MIL.	6167SA55(5) 6167LA55(5) COM'L.	6167SA55(5) 6167LA55(5) MIL.	6167SA70(5) 6167LA70(5) COM'L.	6167SA70(5) 6167LA70(5) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	–	90	90	90	90	90	90	–	90	–	90	–	90	mA
		LA	–	–	55	60	55	60	55	60	–	60	–	60	–	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL} Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	140	–	120	130	100	110/100	100	100	–	100	–	100	–	100	mA
		LA	–	–	100	110	80/70	85/75	65	70	–	65	–	60	–	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	SA	50	–	50	50	35	35	35	35	–	35	–	35	–	35	mA
		LA	–	–	35	35	30/25	30/25	20	20	–	20	–	20	–	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC} f = 0(3)	SA	10	–	5	10	5	10	5	10	–	10	–	10	–	10	mA
		LA	–	–	0.9	2	0.05	2/0.9	0.05	0.9	–	0.9	–	0.9	–	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices
3. f = f_{MAX} (All inputs cycling at f = $1/t_{RC}$). f = 0 means no address control lines change.
4. 0°C to +70°C temperature range only.
5. -55°C to +125°C temperature range only.

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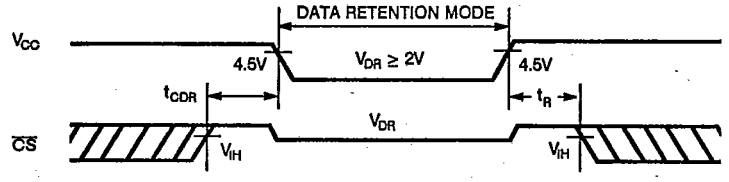
DATA RETENTION CHARACTERISTICS

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC}@ 2.0V	TYP.(1) V_{CC}@ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	0.5	1.0	200	300	µA
			COM'L.	–	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

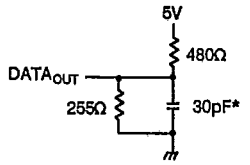


Figure 1. Output Load

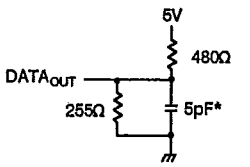


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6167SA12[1] MIN.	6167SA12[1] MAX.	6167SA15 6167LA15 MIN.	6167SA15 6167LA15 MAX.	6167SA20/25 6167LA20/25 MIN.	6167SA20/25 6167LA20/25 MAX.	6167SA35/45[2] 6167LA35/45[2] MIN.	6167SA35/45[2] 6167LA35/45[2] MAX.	6167SA55[2]/70[2] 6167LA55[2]/70[2] MIN.	6167SA55[2]/70[2] 6167LA55[2]/70[2] MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	12	–	15	–	20/25	–	35/45	–	55/70	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20/25	–	35/45	–	55/70	ns
t_{ACS}	Chip Select Access Time	–	12	–	15	–	20/25	–	35/45	–	55/70	ns
t_{OH}	Output Hold from Address Change	3	–	3	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Deselect to Output in Low Z[3]	3	–	3	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Select to Output in High Z[3]	–	8	–	10	–	10	–	15/30	–	40	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	12	–	15	–	20/25	–	35	–	55/70	ns

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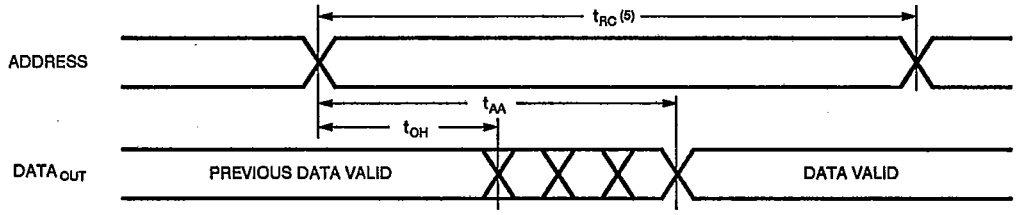
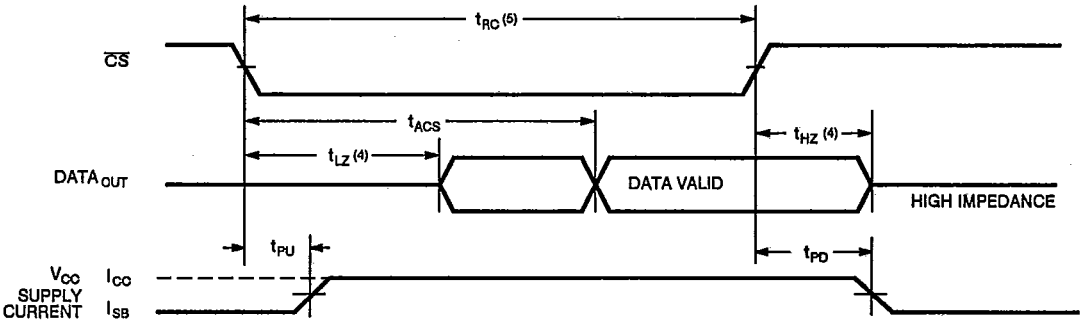
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



NOTES:
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6167SA12[1]		6167SA15 6167LA15		6167SA20/25 6167LA20/25		6167SA35/45[2] 6167LA35/45[2]		6167SA55[2]/70[2] 6167LA55[2]/70[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	12	–	15	–	20/20	–	30/45	–	55/70	–	ns
t_{CW}	Chip Select to End of Write	12	–	15	–	15/20	–	30/40	–	45/55	–	ns
t_{AW}	Address Valid to End of Write	12	–	15	–	15/20	–	30/40	–	45/55	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	15/20	–	30	–	35/40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	10	–	10	–	12/15	–	17/20	–	25/30	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enable to Output in High Z[3]	–	6	–	7	–	8	–	15/30	–	40	ns
t_{OW}	Output Active from End of Write[3]	0	–	0	–	0	–	0	–	0	–	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
3. This parameter guaranteed but not tested.

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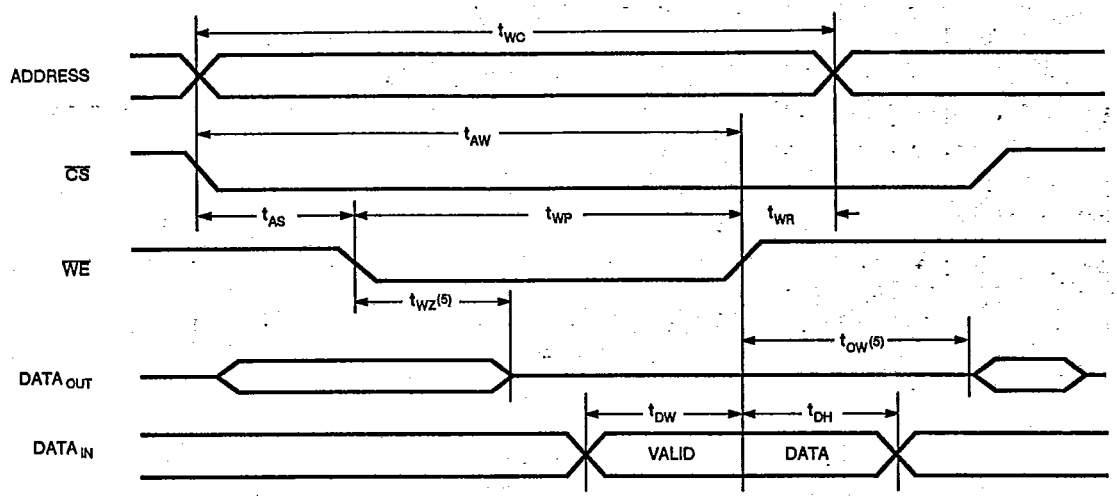
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3)



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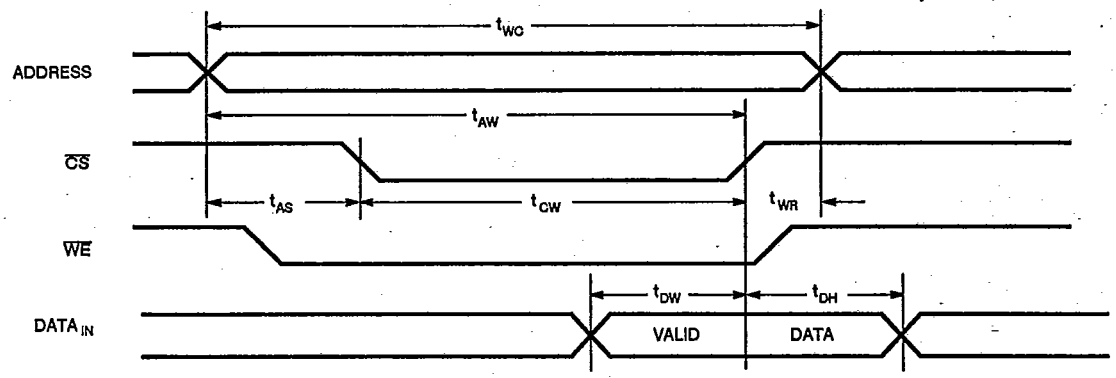
TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 4)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

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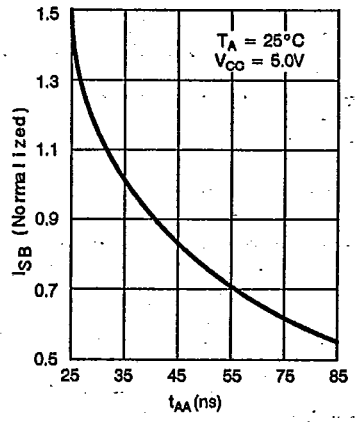
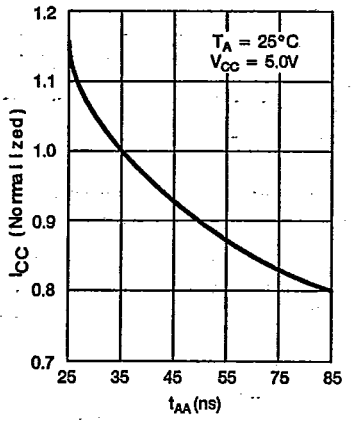
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

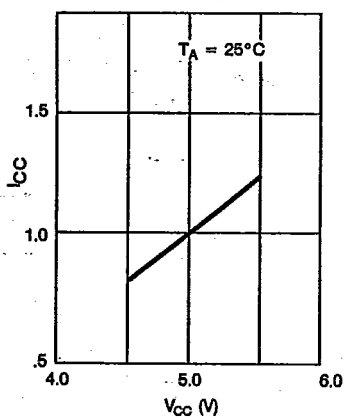
I_{SB} vs. t_{AA} (35ns Device)



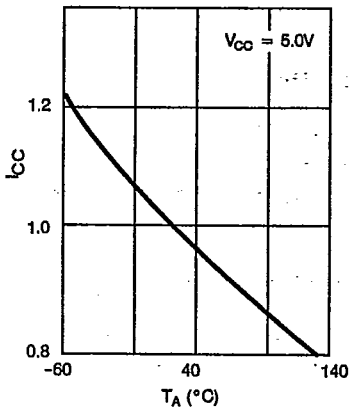
I_{CC} vs. t_{AA} (35ns Device)



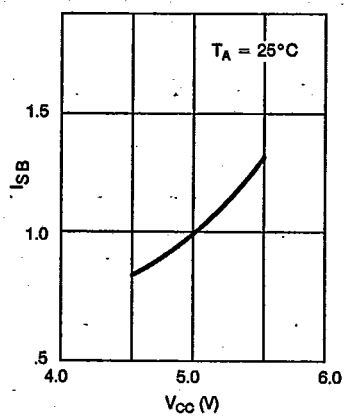
I_{CC} vs. Supply Voltage



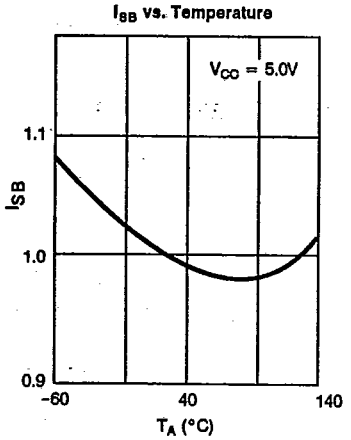
I_{CC} vs. Temperature



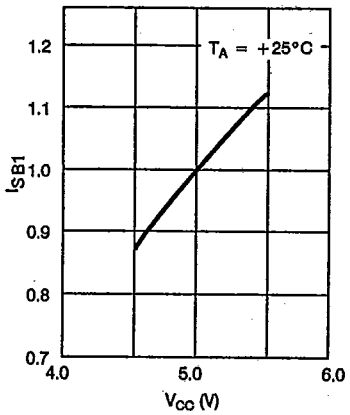
I_{SB} vs. Supply Voltage



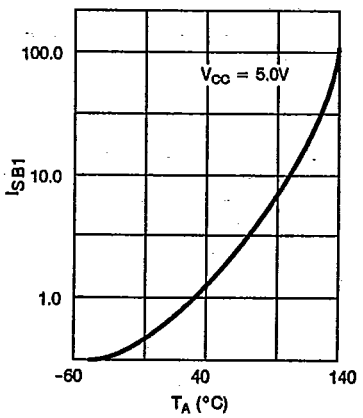
I_{SB} vs. Temperature



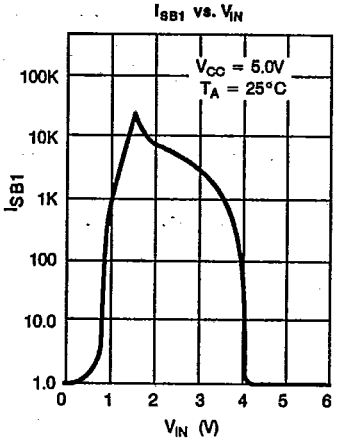
I_{SB1} vs. Supply Voltage



I_{SB1} vs. Temperature



I_{SB1} vs. V_{IN}



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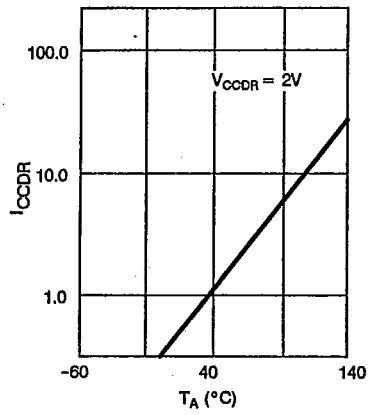
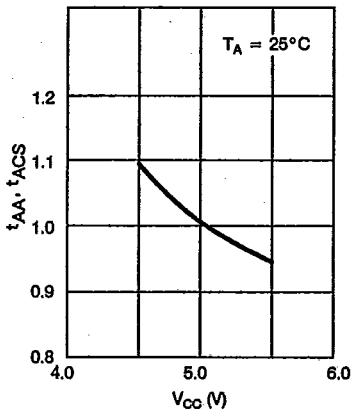
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

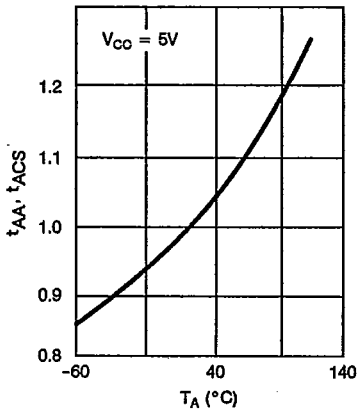
I_{CCDR} vs. Temperature



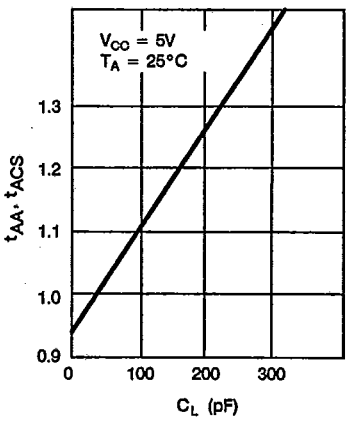
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization and is not production tested.

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ORDERING INFORMATION