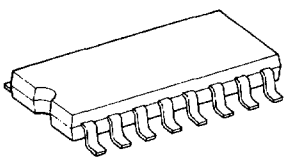
TC74LVQ174F/FN/FS

HEX D-TYPE FLIP FLOP WITH CLEAR

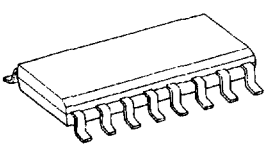
The TC74LVQ174 is a high speed CMOS HEX D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.
When the $\overline{CLR}$ input is held low, the Q output are in the low logic level independent of the other inputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74LVQ174F



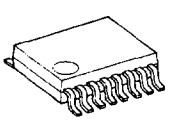
SOP16-P-300

TC74LVQ174FN



SOL16-P-150

TC74LVQ174FS



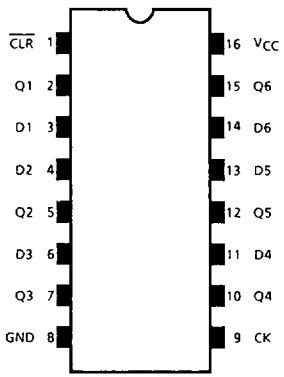
SSOP16-P-225B

Weight SOP16-P-300 : 0.18g (Typ.)
SOL16-P-150 : 0.13g (Typ.)
SSOP16-P-225B : 0.07g (Typ.)

FEATURES

- High speed : f_{MAX} = 165MHz (Typ.) (V_{CC} = 3.3V)
- Low power dissipation : I_{CC} = 4μA (Max.) (Ta = 25°C)
- Input voltage level : V_{IL} = 0.8V (Max.) (V_{CC} = 3V)
  V_{IH} = 2.0V (Min.) (V_{CC} = 3V)
- Symmetrical output impedance
  : $|I_{OH}| = I_{OL}$ = 12mA (Min.)
- Balanced propagation delays
  : $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74HC174

PIN ASSIGNMENT



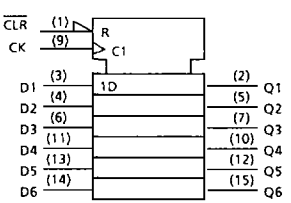
(TOP VIEW)

TRUTH TABLE

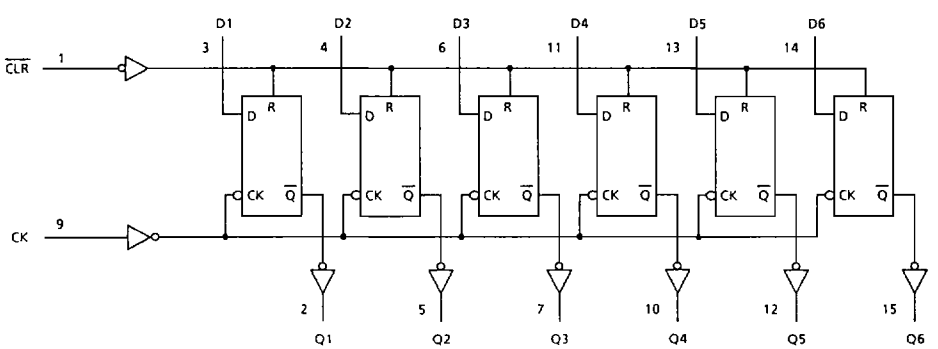
INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±150	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10s	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			3.0	2.0	—	—	2.0	—	V
	"L" Level	V_{IL}			3.0	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	V
				I_{OH} = −12mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current		I_{IN}	V_{IN} = V_{CC} or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.7	9.0	10.0	ns
			3.3 ± 0.3	7.0	7.0	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		2.7	9.0	10.0	ns
			3.3 ± 0.3	7.0	7.0	
Minimum Set-up Time	t_s		2.7	9.0	10.0	ns
			3.3 ± 0.3	7.0	7.0	
Minimum Hold Time	t_h		2.7	1.0	1.0	ns
			3.3 ± 0.3	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.7	7.5	8.5	ns
			3.3 ± 0.3	6.0	6.0	

AC characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40~85°C MIN.	MAX.	UNIT
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		2.7	—	8.2	16.2	1.0	19.0	ns
			3.3 ± 0.3	—	6.8	11.5	1.0	13.0	
Propagation Delay Time ($\overline{CLR}$-Q)	t_{pHL}		2.7	—	7.9	16.2	1.0	18.0	ns
			3.3 ± 0.3	—	6.6	11.5	1.0	12.5	
Maximum Clock Frequency	f_{MAX}		2.7	55	120	—	50	—	MHz
			3.3 ± 0.3	80	145	—	70	—	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	36	—	—	—	pF

(Note 1) *Parameter guaranteed by design.*
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of flip flop operate can be gained by the following equation :

$$C_{PD} \text{ (total)} = 25 + 11 \cdot n$$

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V