National Semiconductor

F100351
Low Power Hex D Flip-Flop

General Description

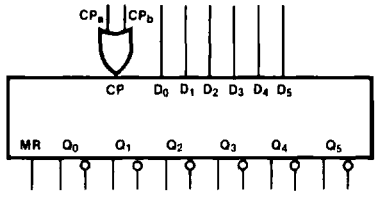
The F100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

- 40% power reduction of the F100151
- 2000V ESD protection
- Pin/function compatible with F100151
- Voltage compensated operating range: −4.2V to −5.7V

Ordering Code: See Section 8

Logic Symbol



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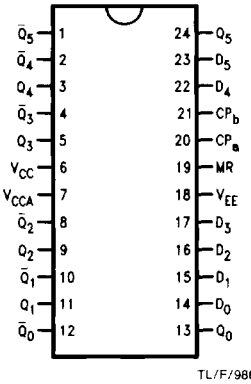
Pin Names	Description
D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



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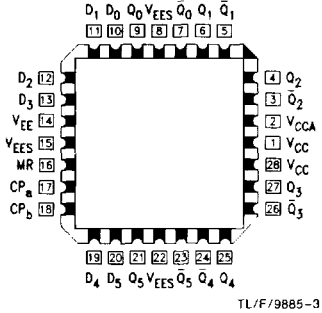
28-Pin PCC



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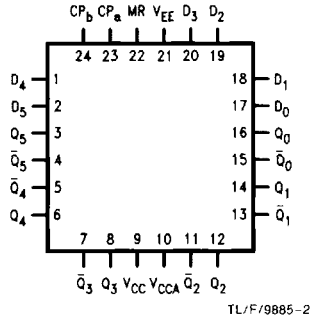
24-Pin Quad Cerpak



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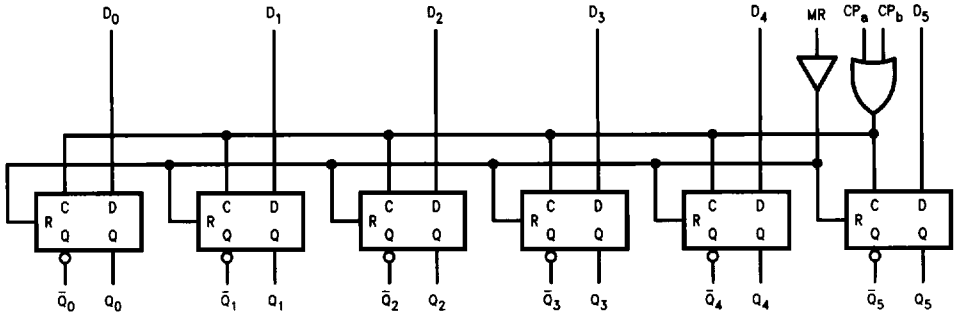
Logic Diagram



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Truth Tables (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	⌐	L	L	L
H	⌐	L	L	H
L	L	⌐	L	L
H	L	⌐	L	H
X	H	⌐	L	$Q_n(t)$
X	⌐	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before CP positive transition
t + 1 = Time after CP positive transition
⌐ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Military	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current MR D_0–D_5 CP_a, CP_b			 350 240 350	 μA	 V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−129		−62	mA	Inputs Open	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.0	0.90	2.10	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.30	1.10	2.30	1.20	2.40	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	*Figures 1* and *3*

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_s	Setup Time D_0–D_5 MR (Release Time)	0.40 1.60		0.40 1.60		0.40 1.60		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0–D_5	1.00		1.00		1.00		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	1.80	0.80	1.80	0.90	1.90	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.10	1.10	2.10	1.20	2.20	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_0–D_5 MR (Release Time)	0.30 1.50		0.30 1.50		0.30 1.50		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0–D_5	0.90		0.90		0.90		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*
$t_{S,\,G\text{-}G}$	Skew, Gate-to-Gate		TBD		TBD		TBD	ps	(PCC only) (Note 1)

Note 1: Gate-to-gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			

Military Version—Preliminary (Continued)

DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	1, 2, 3
I_{IH}	Input HIGH Current MR D_0–D_5 CP_a, CP_b		300 250 520	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	1, 2, 3
	MR D_0–D_5 CP_a, CP_b		450 350 750	μA	−55°C		
I_{EE}	Power Supply Current	−146	−96	mA	−55°C to +125°C	Inputs Open	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.20	0.80	2.20	0.90	2.40	ns	*Figures 1* and *3*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.90	1.30	3.00	1.20	3.10	ns	*Figures 1* and *4*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	*Figures 1* and *3*	4
t_s	Setup Time D_0–D_5	0.70		0.70		0.70		ns	*Figure 5*	
	MR (Release Time)	2.30		2.30		2.60			*Figure 4*	
t_h	Hold Time D_0–D_5	0.70		0.70		0.70		ns	*Figure 5*	
t_{pw}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*	

Military Version—Preliminary (Continued)

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.00	0.90	2.20	ns	*Figures 1* and *3*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.70	1.30	2.80	1.20	2.90	ns	*Figures 1* and *4*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*	
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.60 2.20		 0.60 2.20		 0.60 2.50		ns	*Figure 5* *Figure 4*	4
t_h	Hold Time D_0–D_5	0.60		0.60		0.60		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*	

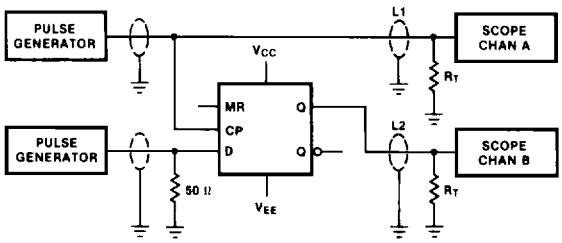
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C Temperature, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

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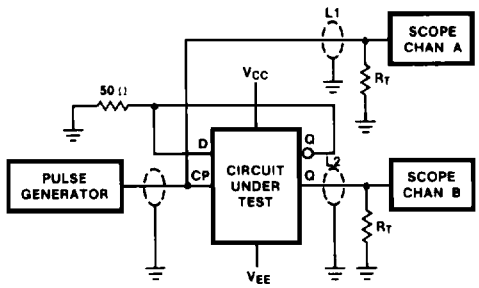
FIGURE 1. AC Test Circuit



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

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FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms

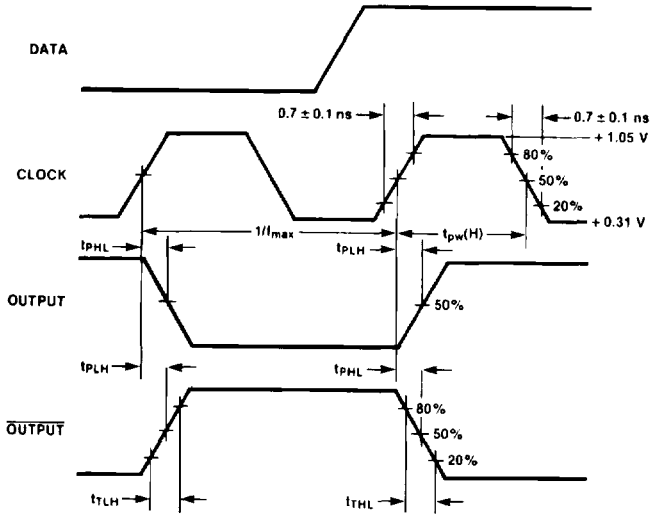

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FIGURE 3. Propagation Delay (Clock) and Transition Times

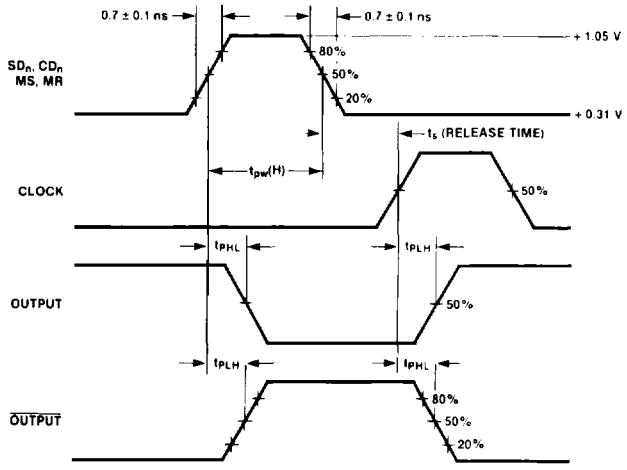

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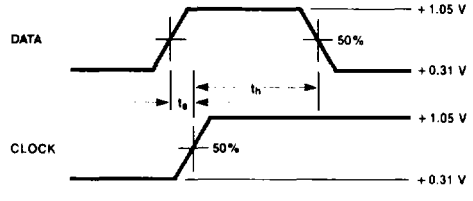
FIGURE 4. Propagation Delay (Reset)



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Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time