

**DESCRIPTION**

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A common clear input resets all flip-flops upon application of a logic "1" level.

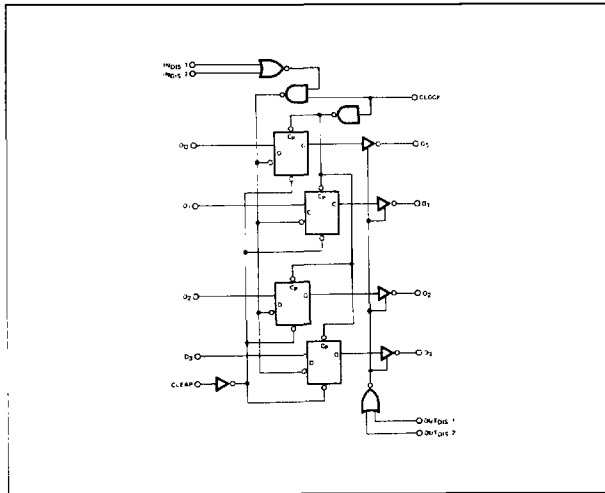
Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

**TRUTH TABLE**

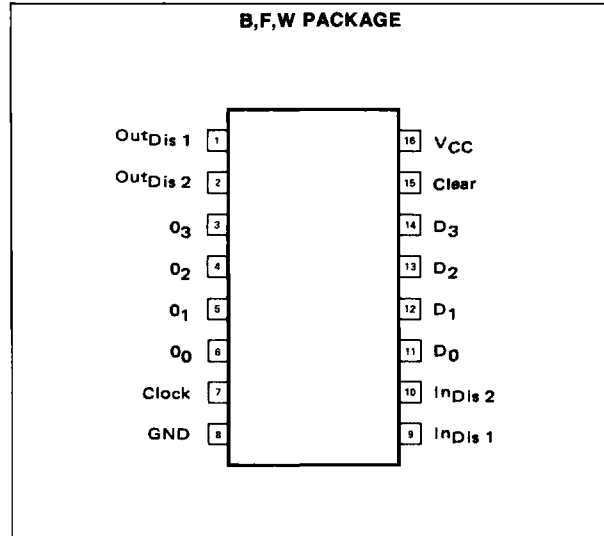
D <sub>n</sub>	INDIS	OUTDIS	O <sub>n+1</sub>
0	0	0	0
1	0	0	1
X	1	0	O <sub>n</sub>
X	X	1	High Z

O<sub>n</sub> refers to the output state before a clock pulse.  
O<sub>n</sub> + 1 refers to the output state after a clock pulse.

**LOGIC DIAGRAM**



**PIN CONFIGURATION**



T<sub>A</sub> = 25° C and V<sub>CC</sub> = 5.0V

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Propagation Delay (t <sub>on</sub> , t <sub>off</sub> )				
Clock to Output				
C <sub>L</sub> = 30pf		18	25	ns
C <sub>L</sub> = 300pf		24	35	ns
Disable to Output				
High Z to Logic 0, t <sub>pZL</sub>		20	30	ns
State (C <sub>L</sub> = 300pf)				
Logic 0 to High Z, t <sub>pLZ</sub>		20	30	ns
High Z (C <sub>L</sub> = 300pf)				
Clear to Output				
C <sub>L</sub> = 30pf		15	22	ns
C <sub>L</sub> = 300pf		21	30	ns
Set Up Time, t <sub>setup</sub>				
Data	+5	-1		ns
Input Disable		-6	0	ns
Hold Time, t <sub>hold</sub>				
Data		-1	+5	ns
Reset Pulse Width	15			ns
Clock Frequency	35	50		MHz
Clock Pulse Width				
Positive		8	12	ns
Negative		8	12	ns

1. Measured to 1.5V level of output waveform.
2. Measured to 10% level of output waveform.
3. Refer to AC Test Circuits.

**INTERFACE**

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY  $t_{on}$ ,  $t_{off}$  (CLOCK TO OUTPUT)  
DATA SETUP TIME,  $t_{setup}$

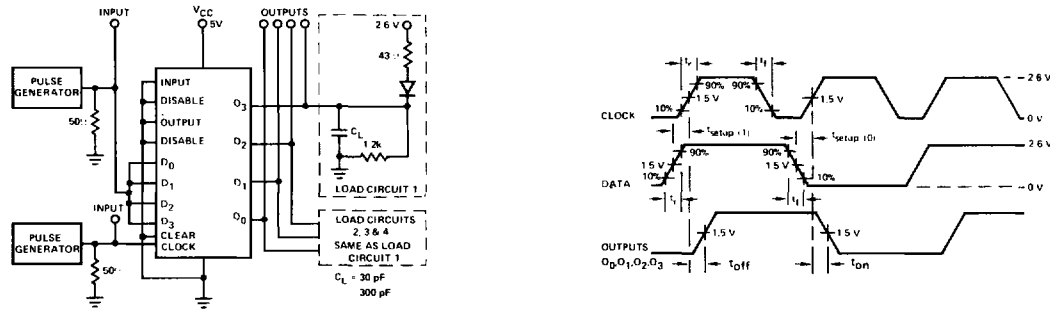


FIGURE 1

PROPAGATION DELAY (CLEAR TO OUTPUT)

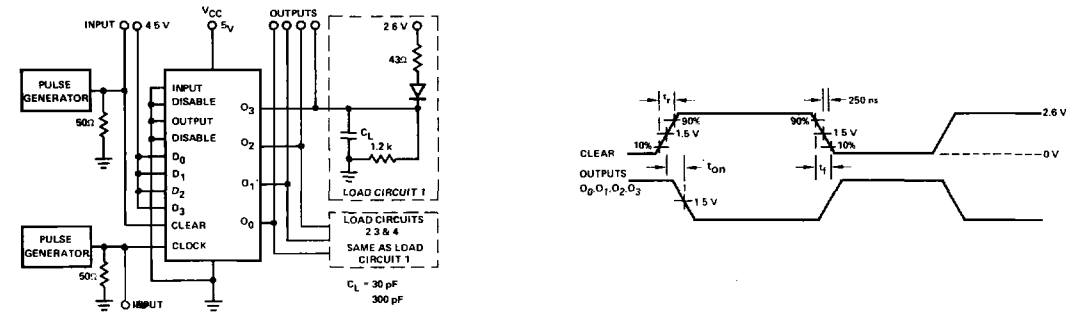


FIGURE 2

PROPAGATION DELAY (DATA HOLD TIME)

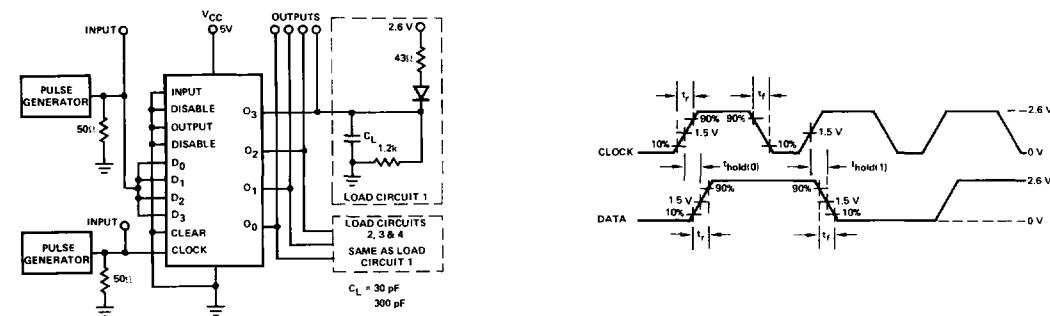
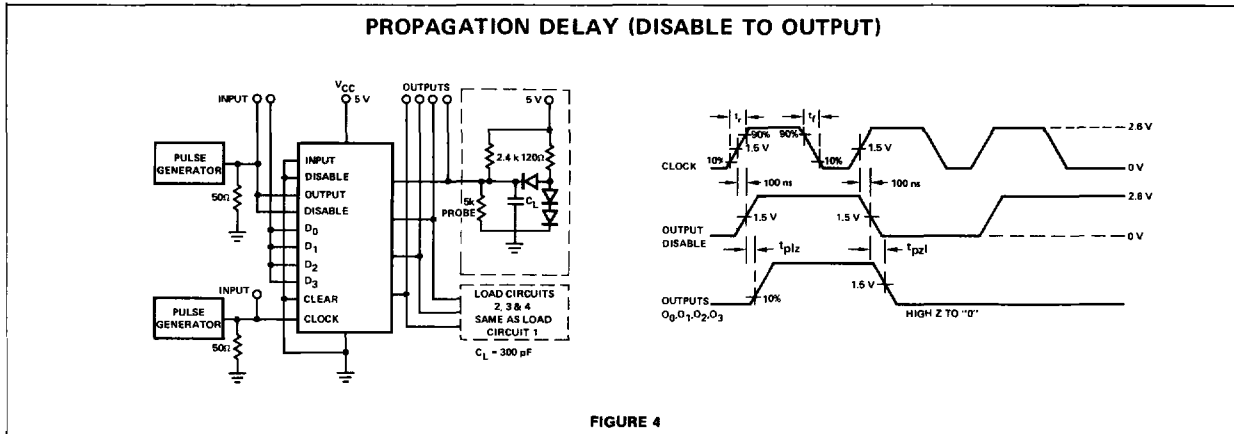
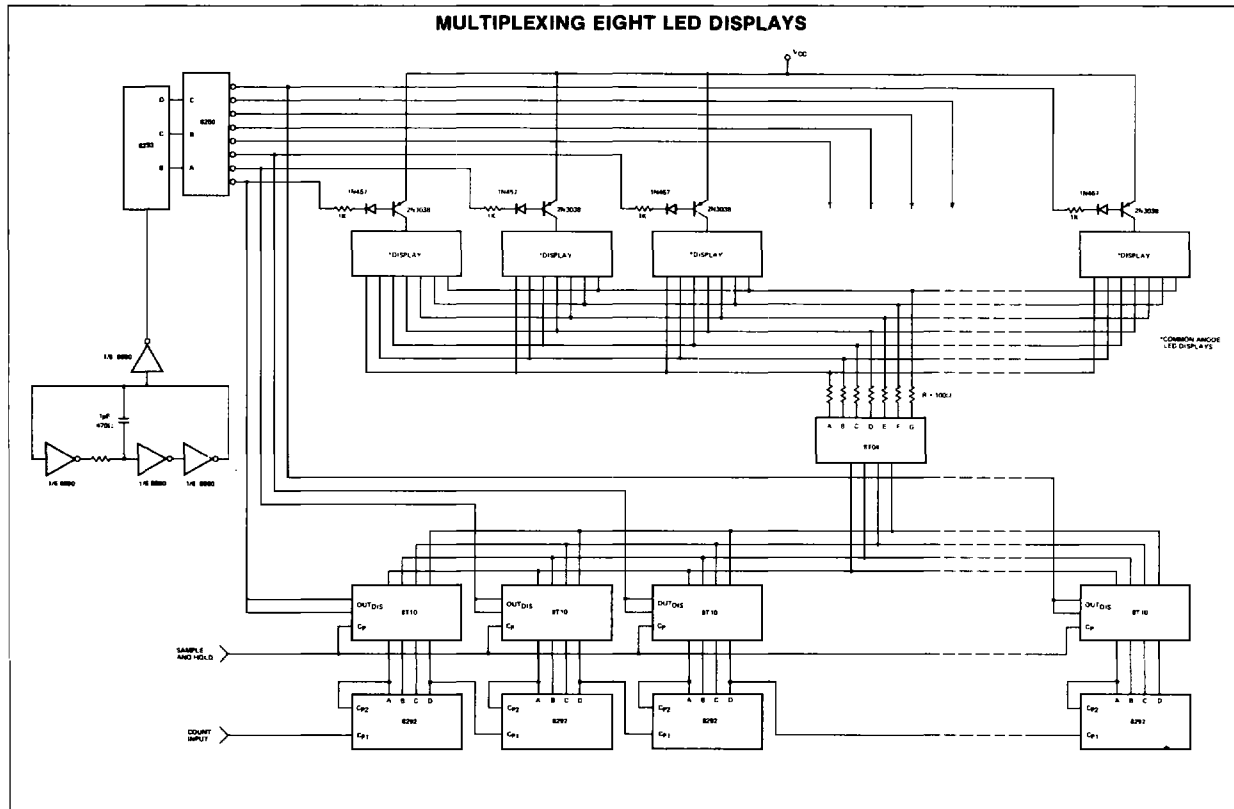


FIGURE 3

AC TEST FIGURES AND WAVEFORMS (Cont'd)



TYPICAL APPLICATIONS



**INTERFACE**

TYPICAL APPLICATIONS

