



CYPRESS

PRELIMINARY

CY7C1354V25
CY7C1356V25

256Kx36/512Kx18 Pipelined SRAM with NoBL™ Architecture

Features

- Pin compatible and functionally equivalent to ZBT™
- Supports 200-MHz bus operations with zero wait states
 - Data is transferred on every clock
- Internally self-timed output buffer control to eliminate the need to use asynchronous OE
- Fully Registered (inputs and outputs) for pipelined operation
- Byte Write capability
- Common I/O architecture
- Single 2.5V power supply
- Fast clock-to-output times
 - 3.2 ns (for 200-MHz device)
 - 3.5 ns (for 166-MHz device)
 - 4.2 ns (for 133-MHz device)
 - 5.0 ns (for 100-MHz device)
- Clock Enable (\overline{CEN}) pin to suspend operation
- Synchronous self-timed writes
- Available in 100 TQFP & 119 BGA Packages
- Burst Capability—linear or interleaved burst order

tively designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1354V25/CY7C1356V25 is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write/Read transitions. The CY7C1354V25/CY7C1356V25 is pin compatible and functionally equivalent to ZBT devices.

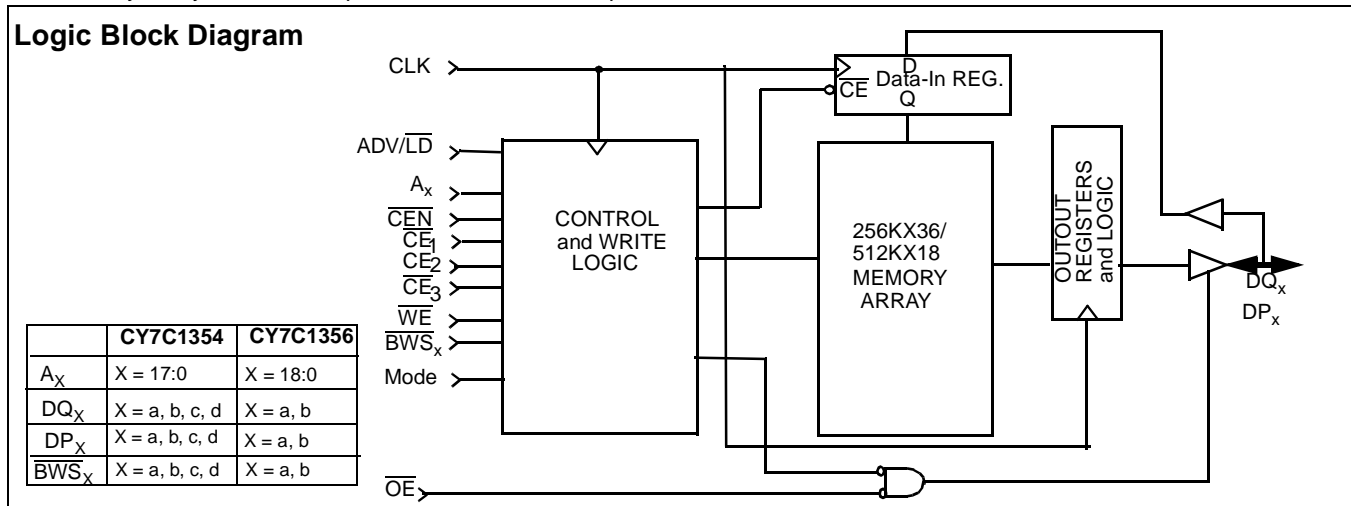
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (\overline{CEN}) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 3.2 ns (200-MHz device).

Write operations are controlled by the Byte Write Selects (\overline{BWSa} - \overline{BWSd} for CY7C1354V25 and \overline{BWSa} - \overline{BWSb} for CY7C1356V25) and a Write Enable (\overline{WE}) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, $\overline{CE_2}$, $\overline{CE_3}$) and an asynchronous Output Enable (\overline{OE}) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

Functional Description

The CY7C1354V25 and CY7C1356V25 are 2.5V, 256K by 36 and 512K by 18 Synchronous-Pipelined Burst SRAMs respec-

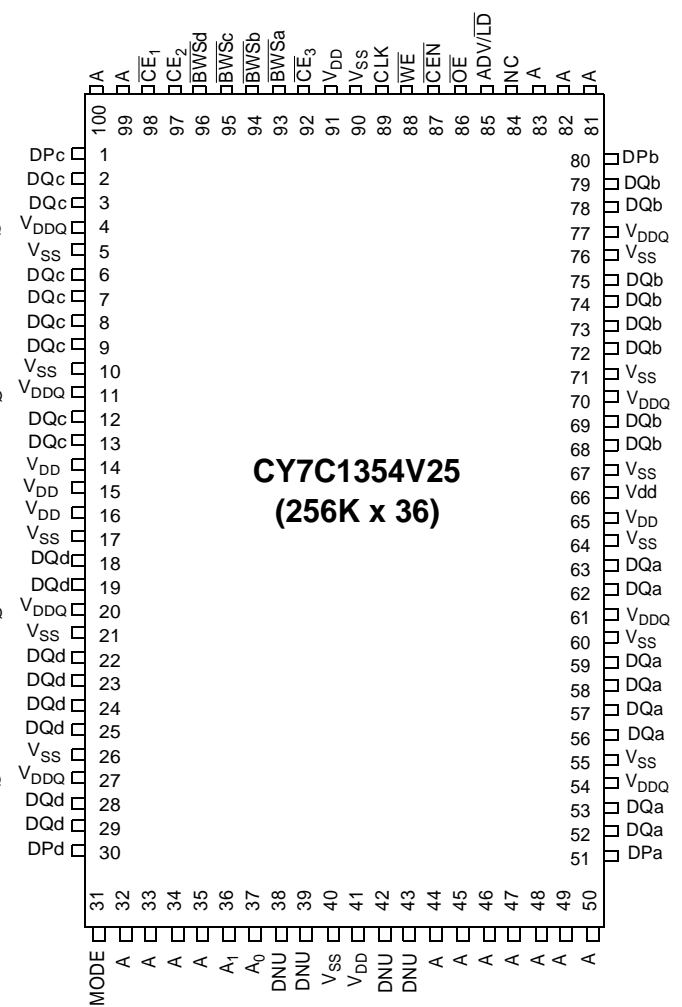
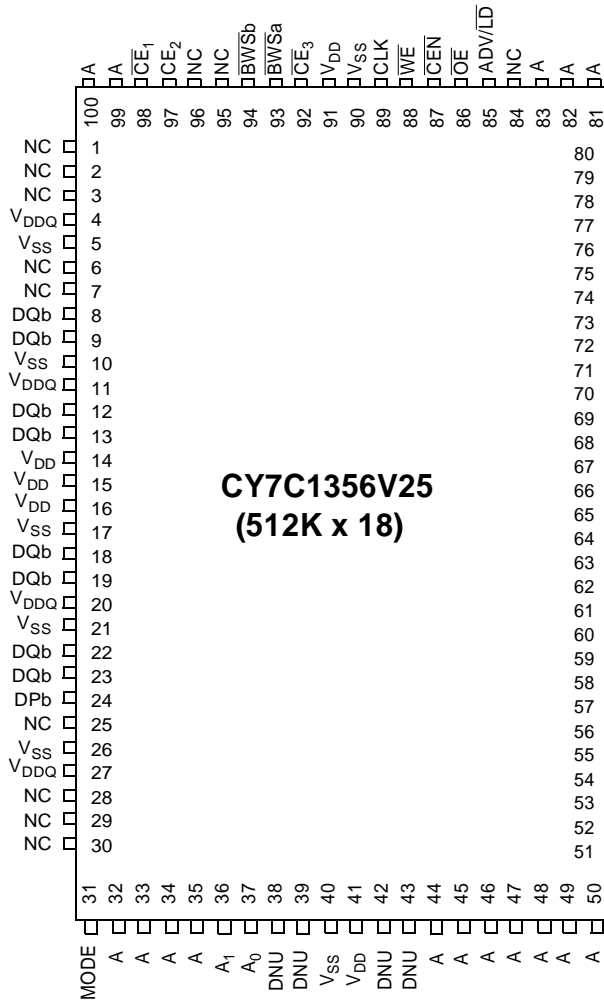


Selection Guide

| | | 7C1354V25-200 7C1356V25-200 | 7C1354V25-166 7C1356V25-166 | 7C1354V25-133 7C1356V25-133 | 7C1354V25-100 7C1356V25-100 |
|-----------------------------------|-------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Maximum Access Time (ns) | | 3.2 | 3.5 | 4.0 | 5.0 |
| Maximum Operating Current (mA) | Com'l | 475 | 450 | 370 | 300 |
| Maximum CMOS Standby Current (mA) | Com'l | 10 | 10 | 10 | 10 |

Shaded areas contain advance information.

No Bus Latency and NoBL are trademarks of Cypress Semiconductor Corporation. ZBT is a trademark of Integrated Device Technology.

Pin Configurations
100-Pin TQFP Packages


Pin Configurations (continued)
119-Ball Bump BGA
CY7C1356 - 7 x 17 BGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| A | V _{DDQ} | A | A | NC | A | A | V _{DDQ} |
| B | NC | CE ₂ | A | ADV/LD | A | CE ₃ | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQb | NC | V _{SS} | NC | V _{SS} | DQa | NC |
| E | NC | DQb | V _{SS} | CE1 | V _{SS} | NC | DQa |
| F | V _{DDQ} | NC | V _{SS} | OE | V _{SS} | DQa | V _{DDQ} |
| G | NC | DQb | BWSb | A | V _{SS} | NC | DQa |
| H | DQb | NC | V _{SS} | WE | V _{SS} | DQa | NC |
| J | V _{DDQ} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DDQ} |
| K | NC | DQb | V _{SS} | CLK | V _{SS} | NC | DQa |
| L | DQb | NC | V _{SS} | NC | BWSa | DQa | NC |
| M | V _{DDQ} | DQb | V _{SS} | CEN | V _{SS} | NC | V _{DDQ} |
| N | DQb | NC | V _{SS} | A1 | V _{SS} | DQa | NC |
| P | NC | DPb | V _{SS} | A0 | V _{SS} | NC | DPa |
| R | NC | A | MODE | V _{DD} | V _{SS} | A | NC |
| T | NC | A | A | NC | A | A | NC |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

CY7C1354 - 7 x 17 BGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| A | V _{DDQ} | A | A | NC | A | A | V _{DDQ} |
| B | NC | CE ₂ | A | ADV/LD | A | CE ₃ | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQc | DPc | V _{SS} | NC | V _{SS} | DPb | DQb |
| E | DQc | DQc | V _{SS} | CE1 | V _{SS} | DQb | DQb |
| F | V _{DDQ} | DQc | V _{SS} | OE | V _{SS} | DQb | V _{DDQ} |
| G | DQc | DQc | BWSc | A | BWSb | DQb | DQb |
| H | DQc | DQc | V _{SS} | WE | V _{SS} | DQb | DQb |
| J | V _{DDQ} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DDQ} |
| K | DQd | DQd | V _{SS} | CLK | V _{SS} | DQa | DQa |
| L | DQd | DQd | BWSc | NC | BWSa | DQa | DQa |
| M | V _{DDQ} | DQd | V _{SS} | CEN | V _{SS} | DQa | V _{DDQ} |
| N | DQd | DQd | V _{SS} | A1 | V _{SS} | DQa | DQa |
| P | DQd | DPd | V _{SS} | A0 | V _{SS} | DQa | DPa |
| R | NC | A | MODE | V _{DD} | V _{SS} | A | NC |
| T | NC | NC | A | A | A | NC | NC |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

Pin Definitions (100-Pin TQFP)

| x18 Pin Location | x36 Pin Location | Name | I/O Type | Description |
|--|---|--|------------------------|---|
| 37, 36, 32–35, 44–50, 80–83, 99, 100 | 37, 36, 32–35, 44–50, 81–83, 99, 100 | A0 A1 A | Input- Synchronous | Address Inputs used to select one of the 266,144 address locations. Sampled at the rising edge of the CLK. |
| 93, 94 | 93, 94, 95, 96 | \overline{BWSa} \overline{BWSb} \overline{BWSc} \overline{BWSd} | Input- Synchronous | Byte Write Select Inputs, active LOW. Qualified with \overline{WE} to conduct writes to the SRAM. Sampled on the rising edge of CLK. \overline{BWSa} controls DQa and DPa, \overline{BWSb} controls DQb and DPb, \overline{BWSc} controls DQc and DPc, \overline{BWSd} controls DQd and DPd. |
| 88 | 88 | \overline{WE} | Input- Synchronous | Write Enable Input, active LOW. Sampled on the rising edge of CLK if \overline{CEN} is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| 85 | 85 | $\overline{ADV/LD}$ | Input- Synchronous | Advance/Load Input used to advance the on-chip address counter or load a new address. When HIGH (and \overline{CEN} is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, $\overline{ADV/LD}$ should be driven LOW in order to load a new address. |
| 89 | 89 | CLK | Input-Clock | Clock Input. Used to capture all synchronous inputs to the device. CLK is qualified with \overline{CEN} . CLK is only recognized if \overline{CEN} is active LOW. |
| 98 | 98 | \overline{CE}_1 | Input- Synchronous | Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select/deselect the device. |
| 97 | 97 | \overline{CE}_2 | Input- Synchronous | Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device. |
| 92 | 92 | \overline{CE}_3 | Input- Synchronous | Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device. |
| 86 | 86 | \overline{OE} | Input- Asynchronous | Output Enable, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. \overline{OE} is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected. |
| 87 | 87 | \overline{CEN} | Input- Synchronous | Clock Enable Input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting \overline{CEN} does not deselect the device, \overline{CEN} can be used to extend the previous cycle when required. |
| (a)58, 59, 62, 63, 68, 69, 72–74 (b)8, 9, 12, 13, 18, 19, 22–24 | (a)52, 53, 56–59, 62, 63, (b)68, 69, 72–75, 78, 79 (c)2, 3, 6–9, 12, 13, (d)18, 19, 22–25, 28, 29 | DQa DQb DQc DQd | I/O- Synchronous | Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} and the internal control logic. When \overline{OE} is asserted LOW, the pins can behave as outputs. When HIGH, DQa–DQd are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} . |

Pin Definitions (100-Pin TQFP) (continued)

| x18 Pin Location | x36 Pin Location | Name | I/O Type | Description |
|---|---|--------------------------|---------------------|--|
| 74, 24 | 51, 80, 1, 30 | DPa DPb DPc DPd | I/O- Synchronous | Bidirectional Data Parity I/O lines. Functionally, these signals are identical to $\overline{DQ}_{[31:0]}$. During write sequences, DPa is controlled by \overline{BWSa} , DPb is controlled by \overline{BWSb} , DPc is controlled by \overline{BWSc} , and DPd is controlled by \overline{BWSd} . |
| 31 | 31 | MODE | Input Strap Pin | Mode Input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order. |
| 14–16, 41, 65, 66, 91 | 14–16, 41, 65, 66, 91 | V _{DD} | Power Supply | Power supply inputs to the core of the device. |
| 4, 11, 20, 27, 54, 61, 70, 77 | 4, 11, 20, 27, 54, 61, 70, 77 | V _{DDQ} | I/O Power Supply | Power supply for the I/O circuitry. |
| 5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90 | 5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90 | V _{SS} | Ground | Ground for the device. Should be connected to ground of the system. |
| NC | NC | NC | - | No connects. Reserved for address expansion to 512K depths. |
| 38, 39, 42, 43 | 38, 39, 42, 43 | DNU | - | Do Not Use pins. These pins should be left floating or tied to V _{SS} . |

Pin Definitions (119 BGA)

| x18 Pin Location | x36 Pin Location | Name | I/O Type | Description |
|--|--|--|--------------------|---|
| P4, N4, A2, A3, A5, A6, B3, B5, C2, C3, C5, C6, G4, R2, R6, T2, T3, T5, T6 | P4, N4, A2, A3, A5, A6, B3, B5, C2, C3, C5, C6, R2, R6, G4, T3, T4, T5 | A0 A1 A | Input-Synchronous | Address Inputs used to select one of the 266,144 address locations. Sampled at the rising edge of the CLK. |
| L5, G3 | L5, G5, G3, L3 | \overline{BWSa} \overline{BWSb} \overline{BWSc} \overline{BWSd} | Input-Synchronous | Byte Write Select Inputs, active LOW. Qualified with \overline{WE} to conduct writes to the SRAM. Sampled on the rising edge of CLK. \overline{BWSa} controls DQa and DPa, \overline{BWSb} controls DQb and DPb, \overline{BWSc} controls DQc and DPc, \overline{BWSd} controls DQd and DPd. |
| H4 | H4 | \overline{WE} | Input-Synchronous | Write Enable Input, active LOW. Sampled on the rising edge of CLK if \overline{CEN} is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| B4 | B4 | $\overline{ADV/LD}$ | Input-Synchronous | Advance/Load Input used to advance the on-chip address counter or load a new address. When HIGH (and \overline{CEN} is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, $\overline{ADV/LD}$ should be driven LOW in order to load a new address. |
| K4 | K4 | CLK | Input-Clock | Clock Input. Used to capture all synchronous inputs to the device. CLK is qualified with \overline{CEN} . CLK is only recognized if \overline{CEN} is active LOW. |
| E4 | E4 | \overline{CE}_1 | Input-Synchronous | Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select/deselect the device. |
| B2 | B2 | \overline{CE}_2 | Input-Synchronous | Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device. |
| B6 | B6 | \overline{CE}_3 | Input-Synchronous | Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device. |
| F4 | F4 | \overline{OE} | Input-Asynchronous | Output Enable, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. \overline{OE} is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected. |
| M4 | M4 | \overline{CEN} | Input-Synchronous | Clock Enable Input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting \overline{CEN} does not deselect the device, \overline{CEN} can be used to extend the previous cycle when required. |

Pin Definitions (119 BGA) (continued)

| x18 Pin Location | x36 Pin Location | Name | I/O Type | Description |
|--|--|---------------------------------|---------------------|---|
| (a)P7, N6, L6, K7, H6, G7, F6, E7 (b)N1, M2, L1, K2, H1, G2, E2, D1 | (a)P7, N7, N6, M6, L7, L6, K7, K6 (b)D7, E7, E6, F6, G7, G6, H7, H6 (c)D1, E1, E2, F2, G1, G2, H1, H2 (d)P1, N1, N2, M2, L1, L2, K1, K2 | DQa DQb DQc DQd | I/O- Synchronous | Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} and the internal control logic. When \overline{OE} is asserted LOW, the pins can behave as outputs. When HIGH, DQa–DQd are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} . |
| D6, P2 | P6, D6, D2, P2 | DPa DPb DPc DPd | I/O- Synchronous | Bidirectional Data Parity I/O lines. Functionally, these signals are identical to $DQ_{[31:0]}$. During write sequences, DPa is controlled by \overline{BWSa} , DPb is controlled by \overline{BWSb} , DPc is controlled by \overline{BWSc} , and DPd is controlled by \overline{BWSd} . |
| R3 | R3 | MODE | Input Strap pin | Mode Input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order. |
| C4, J2, J4, J6, R4 | C4, J2, J4, J6, R4 | V _{DD} | Power Supply | Power supply inputs to the core of the device. |
| A1, A7, F1, F7, J1, J7, M1, M7, U1, U7 | A1, A7, F1, F7, J1, J7, M1, M7, U1, U7 | V _{DDQ} | I/O Power Supply | Power supply for the I/O circuitry. |
| D3, D5, E3, E5, F3, F5, H3, H5, K3, K5, M3, M5, N3, N5, P3, P5, R5 | D3, D5, E3, E5, F3, F5, H3, H5, K3, K5, M3, M5, N3, N5, P3, P5, R5 | V _{SS} | Ground | Ground for the device. Should be connected to ground of the system. |
| T7 | T7 | ZZ | - | |
| U5 | U5 | TDO | - | |
| U3 | U3 | TDI | - | |
| U2 | U2 | TMS | - | |
| U4 | U4 | TCK | - | |
| A4, T6, T2 | A4, T4, T1 | NC, 16M, NC, 32M, NC, 64M | - | No connects. Reserved for address expansion to 512K depths. |
| B1, B7, C1, C7, D2, D4, D7, E1, E6, F2, G1, G5, G6, H2, H7, J3, J5, K1, K6, L2, L3, L4, M6, N2, N7, P1, P6, R1, R7 | B7, C7, D4, J3, J5, L4, R1, R7, T1 | NC | - | No connects. |

Introduction

Functional Overview

The CY7C1354V25/1356V25 are synchronous-pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal (\overline{CEN}). If \overline{CEN} is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with \overline{CEN} . All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.2 ns (200-MHz device).

Accesses can be initiated by asserting all three Chip Enables (\overline{CE}_1 , CE_2 , \overline{CE}_3) active at the rising edge of the clock. If Clock Enable (\overline{CEN}) is active LOW and $\overline{ADV}/\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the Write Enable (\overline{WE}). $\overline{BWS}_{[d:a]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable (\overline{WE}). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables (\overline{CE}_1 , CE_2 , \overline{CE}_3) and an asynchronous Output Enable (\overline{OE}) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. $\overline{ADV}/\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CEN} is asserted LOW, (2) \overline{CE}_1 , CE_2 , and \overline{CE}_3 are ALL asserted active, (3) the write enable input signal \overline{WE} is deasserted HIGH, and (4) $\overline{ADV}/\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.2 ns (200-MHz device) provided \overline{OE} is active LOW. After the first clock of the read access the output buffers are controlled by \overline{OE} and the internal control logic. \overline{OE} must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

Burst Read Accesses

The CY7C1354V25/1356V25 have on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. $\overline{ADV}/\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst se-

quence, and will wrap-around when incremented sufficiently. A HIGH input on $\overline{ADV}/\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or \overline{WE} . \overline{WE} is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) \overline{CEN} is asserted LOW, (2) \overline{CE}_1 , CE_2 , and \overline{CE}_3 are ALL asserted active, and (3) the write signal \overline{WE} is asserted LOW. The address presented to A_0 - A_{16} is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the \overline{OE} input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}/DP_{a,b}$ for CY7C1354V25 and $DQ_{a,b}/DP_{a,b}$ for CY7C1356V25). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DP ($DQ_{a,b,c,d}/DP_{a,b}$ for CY7C1354V25 & $DQ_{a,b}/DP_{a,b}$ for CY7C1356V25) (or a subset for byte write operations, see Write Cycle Description Table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by \overline{BWS} ($\overline{BWS}_{a,b,c,d}$ for CY7C1354V25 & $\overline{BWS}_{a,b}$ for CY7C1356V25) signals. The CY7C1354V25/56V25 provides byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input (\overline{WE}) with the selected Byte Write Select (\overline{BWS}) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1354V25/56V25 is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable (\overline{OE}) can be deasserted HIGH before presenting data to the DQ and DP ($DQ_{a,b,c,d}/DP_{a,b}$ for CY7C1354V25 & $DQ_{a,b}/DP_{a,b}$ for CY7C1356V25) inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DP ($DQ_{a,b,c,d}/DP_{a,b}$ for CY7C1354V25 & $DQ_{a,b}/DP_{a,b}$ for CY7C1356V25) are automatically three-stated during the data portion of a write cycle, regardless of the state of \overline{OE} .

Burst Write Accesses

The CY7C1354V25/56V25 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. $\overline{ADV}/\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When $\overline{ADV}/\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables (\overline{CE}_1 , CE_2 , and \overline{CE}_3) and \overline{WE} inputs are ignored and the burst counter is incremented. The correct \overline{BWS} ($\overline{BWS}_{a,b,c,d}$ for CY7C1354V25 & $\overline{BWS}_{a,b}$ for CY7C1356V25) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Cycle Description Truth Table^[1, 2, 3, 4, 5, 6]

| Operation | Address Used | \overline{CE} | \overline{CEN} | $\overline{ADV/LD}$ | \overline{WE} | \overline{BWS}_x | CLK | Comments |
|-----------------------|--------------|-----------------|------------------|---------------------|-----------------|--------------------|-----|---|
| Deselected | External | 1 | 0 | L | X | X | L-H | I/Os three-state following next recognized clock. |
| Suspend | - | X | 1 | X | X | X | L-H | Clock ignored, all operations suspended. |
| Begin Read | External | 0 | 0 | 0 | 1 | X | L-H | Address latched. |
| Begin Write | External | 0 | 0 | 0 | 0 | Valid | L-H | Address latched, data presented two valid clocks later. |
| Burst Read Operation | Internal | X | 0 | 1 | X | X | L-H | Burst Read operation. Previous access was a Read operation. Addresses incremented internally in conjunction with the state of Mode. |
| Burst Write Operation | Internal | X | 0 | 1 | X | Valid | L-H | Burst Write operation. Previous access was a Write operation. Addresses incremented internally in conjunction with the state of MODE. Bytes written are determined by $BWS_{[d:a]}$. |

Interleaved Burst Sequence

| First Address | Second Address | Third Address | Fourth Address |
|---------------|----------------|---------------|----------------|
| A[1:0] | A[1:0] | A[1:0] | A[1:0] |
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

Linear Burst Sequence

| First Address | Second Address | Third Address | Fourth Address |
|---------------|----------------|---------------|----------------|
| A[1:0] | A[1:0] | A[1:0] | A[1:0] |
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

Notes:

- X="Don't Care", 1=Logic HIGH, 0=Logic LOW, \overline{CE} stands for ALL Chip Enables active. $\overline{BWS}_x = 0$ signifies at least one Byte Write Select is active, $\overline{BWS}_x = \text{Valid}$ signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
- Write is defined by \overline{WE} and \overline{BWS}_x . See Write Cycle Description table for details.
- The DQ and DP pins are controlled by the current cycle and the \overline{OE} signal.
- $\overline{CEN}=1$ inserts wait states.
- Device will power-up deselected and the I/Os in a three-state condition, regardless of \overline{OE} .
- \overline{OE} assumed LOW.

Write Cycle Description^[1]

| Function (CY7C1354V25) | \overline{WE} | \overline{BWS}_d | \overline{BWS}_c | \overline{BWS}_b | \overline{BWS}_a |
|------------------------------|-----------------|--------------------|--------------------|--------------------|--------------------|
| Read | 1 | X | X | X | X |
| Write - No bytes written | 0 | 1 | 1 | 1 | 1 |
| Write Byte 0 - (DQa and DPa) | 0 | 1 | 1 | 1 | 0 |
| Write Byte 1 - (DQb and DPb) | 0 | 1 | 1 | 0 | 1 |
| Write Bytes 1, 0 | 0 | 1 | 1 | 0 | 0 |
| Write Byte 2 - (DQc and DPc) | 0 | 1 | 0 | 1 | 1 |
| Write Bytes 2, 0 | 0 | 1 | 0 | 1 | 0 |
| Write Bytes 2, 1 | 0 | 1 | 0 | 0 | 1 |
| Write Bytes 2, 1, 0 | 0 | 1 | 0 | 0 | 0 |
| Write Byte 3 - (DQd and DPd) | 0 | 0 | 1 | 1 | 1 |
| Write Bytes 3, 0 | 0 | 0 | 1 | 1 | 0 |
| Write Bytes 3, 1 | 0 | 0 | 1 | 0 | 1 |
| Write Bytes 3, 1, 0 | 0 | 0 | 1 | 0 | 0 |
| Write Bytes 3, 2 | 0 | 0 | 0 | 1 | 1 |
| Write Bytes 3, 2, 0 | 0 | 0 | 0 | 1 | 0 |
| Write Bytes 3, 2, 1 | 0 | 0 | 0 | 0 | 1 |
| Write All Bytes | 0 | 0 | 0 | 0 | 0 |

| Function (CY7C1356V25) | \overline{WE} | \overline{BWS}_b | \overline{BWS}_a |
|---|-----------------|--------------------|--------------------|
| Read | 1 | x | x |
| Write - No Bytes Written | 0 | 1 | 1 |
| Write Byte 0 - (DQ _a and DP _a) | 0 | 1 | 0 |
| Write Byte 1 - (DQ _b and DP _b) | 0 | 0 | 1 |
| Write Both Bytes | 0 | 0 | 0 |

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1354/56 incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAP Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP) - Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the

instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a xx-bit-long register, and the x18 configuration has a yy-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the Input or Output buffers. The

SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE / PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does not recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE / PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE / PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE / PRELOAD

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant.

When the SAMPLE / PRELOAD instructions are loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (TCS and TCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE / PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

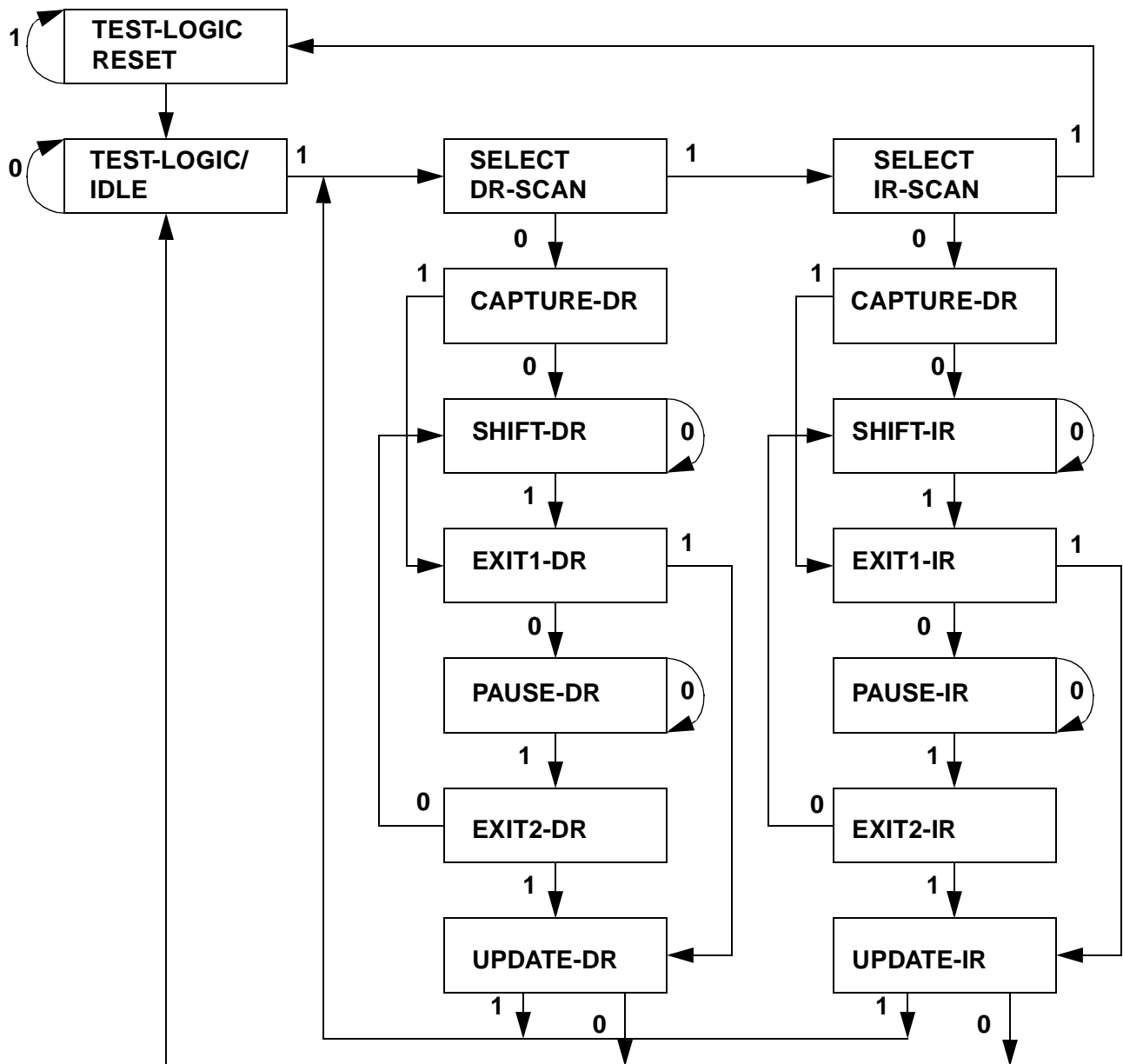
Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE / PRELOAD instruction will have the same effect as the Pause-DR command.

Bypass

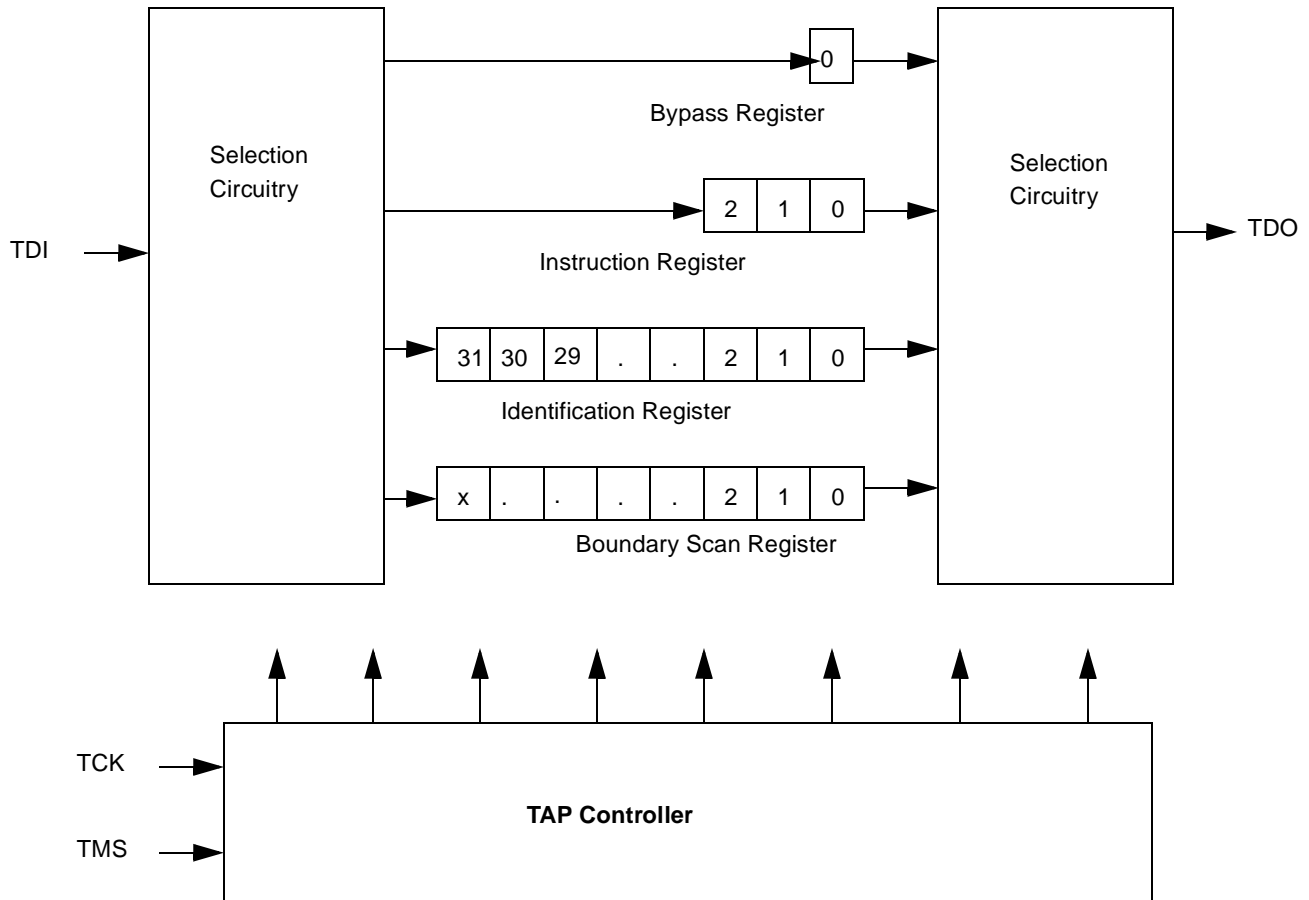
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram


Note: The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram

TAP Electrical Characteristics Over the Operating Range^[7, 8]

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|------------------|---------------------|---|------|----------------------|------|
| V _{OH1} | Output HIGH Voltage | I _{OH} = -2.0 mA | 1.7 | | V |
| V _{OH2} | Output HIGH Voltage | I _{OH} = -100 μA | 2.1 | | V |
| V _{OL1} | Output LOW Voltage | I _{OL} = 2.0 mA | | 0.7 | V |
| V _{OL2} | Output LOW Voltage | I _{OL} = 100 μA | | 0.2 | V |
| V _{IH} | Input HIGH Voltage | | 1.7 | V _{DD} +0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.7 | V |
| I _X | Input Load Current | GND ≤ V _I ≤ V _{DDQ} | -5 | 5 | μA |

Notes:

7. All Voltage referenced to Ground

8. Overshoot: V_{IH(AC)} ≤ V_{DD}+1.5V for t_{≤t_{TCYC}/2}, Undershoot: V_{IL(AC)} ≤ 0.5V for t_{≤t_{TCYC}/2}, Power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

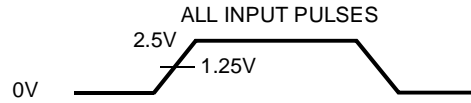
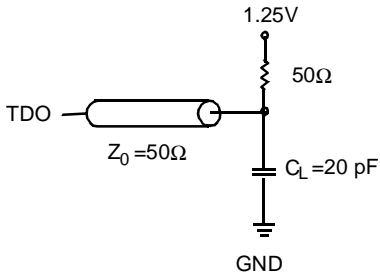
TAP AC Switching Characteristics Over the Operating Range^[9, 10]

| Parameter | Description | Min. | Max | Unit |
|---------------------|-------------------------------|------|-----|------|
| t _{TCYC} | TCK Clock Cycle Time | 100 | | ns |
| t _{TF} | TCK Clock Frequency | | 10 | MHz |
| t _{TH} | TCK Clock HIGH | 40 | | ns |
| t _{TL} | TCK Clock LOW | 40 | | ns |
| Set-up Times | | | | |
| t _{TMSS} | TMS Set-up to TCK Clock Rise | 10 | | ns |
| t _{TDIS} | TDI Set-up to TCK Clock Rise | 10 | | ns |
| t _{CS} | Capture Set-up to TCK Rise | 10 | | ns |
| Hold Times | | | | |
| t _{TMSH} | TMS Hold after TCK Clock Rise | 10 | | ns |
| t _{TDIH} | TDI Hold after Clock Rise | 10 | | ns |
| t _{CH} | Capture Hold after clock rise | 10 | | ns |
| Output Times | | | | |
| t _{TDOV} | TCK Clock LOW to TDO Valid | | 20 | ns |
| t _{TDOX} | TCK Clock LOW to TDO Invalid | 0 | | ns |

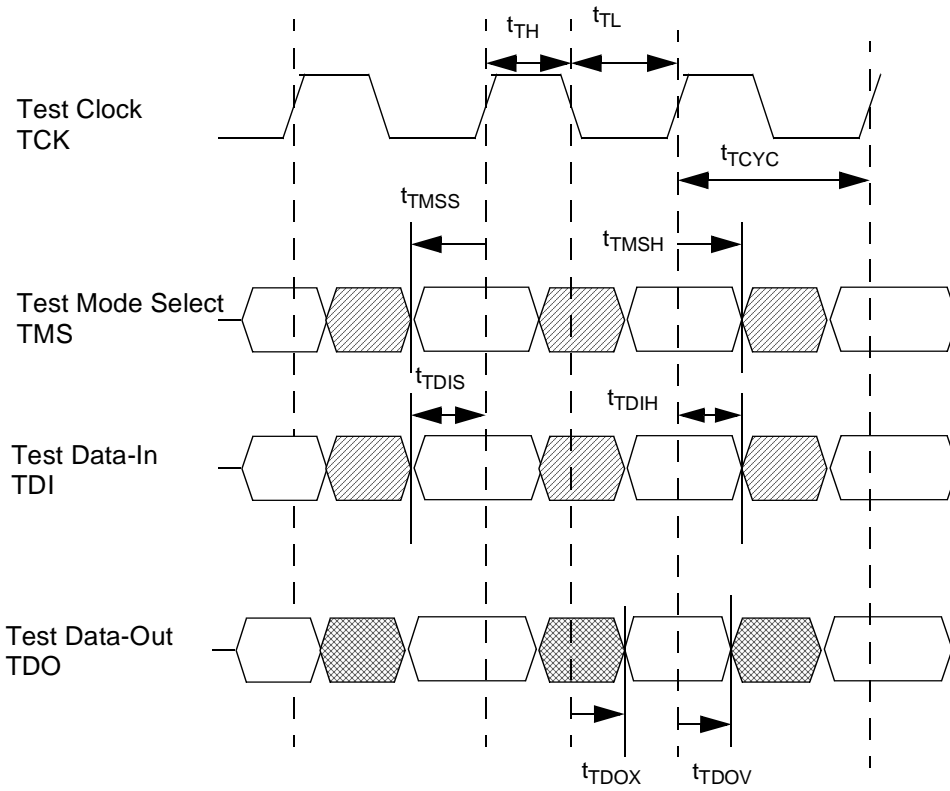
Notes:

9. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
 10. Test conditions are specified using the load in TAP AC test conditions. Tr/Tf = 1 ns.

TAP Timing and Test Conditions



(a)



Identification Register Definitions

| Instruction Field | Value | Description |
|------------------------------|-------|--|
| Revision Number (31:28) | TBD | Reserved for version number. |
| Device Depth (27:23) | TBD | Defines depth of SRAM. |
| Device Width (22:18) | TBD | Defines with of the SRAM. |
| Cypress Device ID (17:12) | TBD | Reserved for future use. |
| Cypress JEDEC ID (11:1) | TBD | Allows unique identification of SRAM vendor. |
| ID Register Presence (0) | TBD | Indicate the presence of an ID register. |

Scan Register sizes

| Register Name | Bit Size |
|---------------|----------|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | TBD |

Identification Codes

| Instruction | Code | Description |
|----------------|------|--|
| EXTEST | 000 | Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation. |
| SAMPLE Z | 010 | Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operation. |

Boundary Scan Order

| Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID |
|-------|-------------|---------|-------|-------------|---------|
| 1 | TBD | TBD | 36 | TBD | TBD |
| 2 | TBD | TBD | 37 | TBD | TBD |
| 3 | TBD | TBD | 38 | TBD | TBD |
| 4 | TBD | TBD | 39 | TBD | TBD |
| 5 | TBD | TBD | 40 | TBD | TBD |
| 6 | TBD | TBD | 41 | TBD | TBD |
| 7 | TBD | TBD | 42 | TBD | TBD |
| 8 | TBD | TBD | 43 | TBD | TBD |
| 9 | TBD | TBD | 44 | TBD | TBD |
| 10 | TBD | TBD | 45 | TBD | TBD |
| 11 | TBD | TBD | 46 | TBD | TBD |
| 12 | TBD | TBD | 47 | TBD | TBD |
| 13 | TBD | TBD | 48 | TBD | TBD |
| 14 | TBD | TBD | 49 | TBD | TBD |
| 15 | TBD | TBD | 50 | TBD | TBD |
| 16 | TBD | TBD | 51 | TBD | TBD |
| 17 | TBD | TBD | 52 | TBD | TBD |
| 18 | TBD | TBD | 53 | TBD | TBD |
| 19 | TBD | TBD | 54 | TBD | TBD |
| 20 | TBD | TBD | 55 | TBD | TBD |
| 21 | TBD | TBD | 56 | TBD | TBD |
| 22 | TBD | TBD | 57 | TBD | TBD |
| 23 | TBD | TBD | 58 | TBD | TBD |
| 24 | TBD | TBD | 59 | TBD | TBD |
| 25 | TBD | TBD | 60 | TBD | TBD |
| 26 | TBD | TBD | 61 | TBD | TBD |
| 27 | TBD | TBD | 62 | TBD | TBD |
| 28 | TBD | TBD | 63 | TBD | TBD |
| 29 | TBD | TBD | 64 | TBD | TBD |
| 30 | TBD | TBD | 65 | TBD | TBD |
| 31 | TBD | TBD | 66 | TBD | TBD |
| 32 | TBD | TBD | 67 | TBD | TBD |
| 33 | TBD | TBD | 68 | TBD | TBD |
| 34 | TBD | TBD | 69 | TBD | TBD |
| 35 | TBD | TBD | 70 | TBD | TBD |

Boundary Scan Order

| Bit # | Signal Name | Bump ID | Bit # | Signal Name | Bump ID |
|-------|-------------|---------|-------|-------------|---------|
| 71 | TBD | TBD | | TBD | TBD |
| 72 | TBD | TBD | | TBD | TBD |
| 73 | TBD | TBD | | TBD | TBD |
| 74 | TBD | TBD | | TBD | TBD |
| 75 | TBD | TBD | | TBD | TBD |
| 76 | TBD | TBD | | TBD | TBD |
| 77 | TBD | TBD | | TBD | TBD |
| 78 | TBD | TBD | | TBD | TBD |
| 79 | TBD | TBD | | TBD | TBD |
| 80 | TBD | TBD | | TBD | TBD |
| 81 | TBD | TBD | | TBD | TBD |
| 82 | TBD | TBD | | TBD | TBD |
| 83 | TBD | TBD | | TBD | TBD |
| 84 | TBD | TBD | | TBD | TBD |
| 85 | TBD | TBD | | TBD | TBD |
| 86 | TBD | TBD | | TBD | TBD |
| 87 | TBD | TBD | | TBD | TBD |
| 88 | TBD | TBD | | TBD | TBD |
| 89 | TBD | TBD | | TBD | TBD |
| 90 | TBD | TBD | | TBD | TBD |
| 91 | TBD | TBD | | TBD | TBD |
| 92 | TBD | TBD | | TBD | TBD |
| 93 | TBD | TBD | | TBD | TBD |
| 94 | TBD | TBD | | TBD | TBD |
| 95 | TBD | TBD | | TBD | TBD |
| 96 | TBD | TBD | | TBD | TBD |
| 97 | TBD | TBD | | TBD | TBD |
| 98 | TBD | TBD | | TBD | TBD |
| 99 | TBD | TBD | | TBD | TBD |



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- Supply Voltage on V_{DD} Relative to GND -0.5V to +3.6V
- DC Voltage Applied to Outputs in High Z State^[12] -0.5V to V_{DDQ} + 0.5V
- DC Input Voltage^[12] -0.5V to V_{DDQ} + 0.5V

- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature ^[11] | V _{DD} /V _{DDQ} |
|-------|-------------------------------------|-----------------------------------|
| Com'l | 0°C to +70°C | 2.5V ± 5% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit | |
|------------------|---|--|-----------------------|------------------------|------|----|
| V _{DD} | Power Supply Voltage | | 2.375 | 2.625 | V | |
| V _{DDQ} | I/O Supply Voltage | | 2.375 | 2.625 | V | |
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1.0 mA ^[13] | 2.0 | | V | |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 1.0 mA ^[13] | | 0.2 | V | |
| V _{IH} | Input HIGH Voltage | | 1.7 | V _{DD} + 0.3V | V | |
| V _{IL} | Input LOW Voltage ^[12] | | -0.3 | 0.7 | V | |
| I _X | Input Load Current | GND ≤ V _I ≤ V _{DDQ} | -5 | 5 | μA | |
| | Input Current of MODE | | -30 | 30 | μA | |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{DDQ} , Output Disabled | -5 | 5 | μA | |
| I _{DD} | V _{DD} Operating Supply | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{CYC} | 5-ns cycle, 200 MHz | | 475 | mA |
| | | | 6-ns cycle, 166 MHz | | 450 | mA |
| | | | 7.5-ns cycle, 133 MHz | | 320 | mA |
| | | | 10-ns cycle, 100 MHz | | 300 | mA |
| I _{SB1} | Automatic CE Power-Down Current—TTL Inputs | Max. V _{DD} , Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} = 1/t _{CYC} | 5-ns cycle, 200 MHz | | 90 | mA |
| | | | 6-ns cycle, 166 MHz | | 80 | mA |
| | | | 7.5-ns cycle, 133 MHz | | 70 | mA |
| | | | 10-ns cycle, 100 MHz | | 65 | mA |
| I _{SB2} | Automatic CE Power-Down Current—CMOS Inputs | Max. V _{DD} , Device Deselected, V _{IN} ≤ 0.3V or V _{IN} ≥ V _{DDQ} - 0.3V, f = 0 | | 10 | mA | |
| I _{SB3} | Automatic CE Power-Down Current—CMOS Inputs | Max. V _{DD} , Device Deselected, or V _{IN} ≤ 0.3V or V _{IN} ≥ V _{DDQ} - 0.3V, f = f _{MAX} = 1/t _{CYC} | 5-ns cycle, 200 MHz | | 45 | mA |
| | | | 6-ns cycle, 166 MHz | | 40 | mA |
| | | | 7.5-ns cycle, 133 MHz | | 35 | mA |
| | | | 10-ns cycle, 100 MHz | | 30 | mA |
| I _{SB4} | Automatic CE Power-Down Current—TTL Inputs | Max. V _{DD} , Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = 0 | | 25 | mA | |

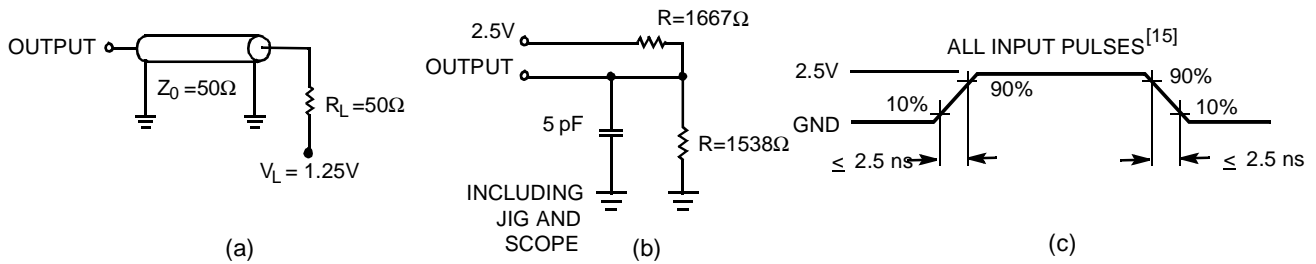
Shaded areas contain advance information.

Notes:

- 11. T_A is the case temperature.
- 12. Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
- 13. The load used for V_{OH} and V_{OL} testing is shown in figure (b) of the A/C test conditions.

Capacitance^[14]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|--------------------------|---|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = V_{DDQ} = 2.5\text{V}$ | 4 | pF |
| C_{CLK} | Clock Input Capacitance | | 4 | pF |
| $C_{I/O}$ | Input/Output Capacitance | | 4 | pF |

AC Test Loads and Waveforms

Thermal Resistance

| Description | Test Conditions | Symbol | TQFP Typ. | Units | Notes |
|--|---|----------|-----------|--------------------|-------|
| Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board | Q_{JA} | TBD | $^\circ\text{C/W}$ | 14 |
| Thermal Resistance (Junction to Case) | | Q_{JC} | TBD | $^\circ\text{C/W}$ | 14 |

Notes:

14. Tested initially and after any design or process change that may affect these parameters.
 15. Input waveform should have a slew rate of 1 V/ns.

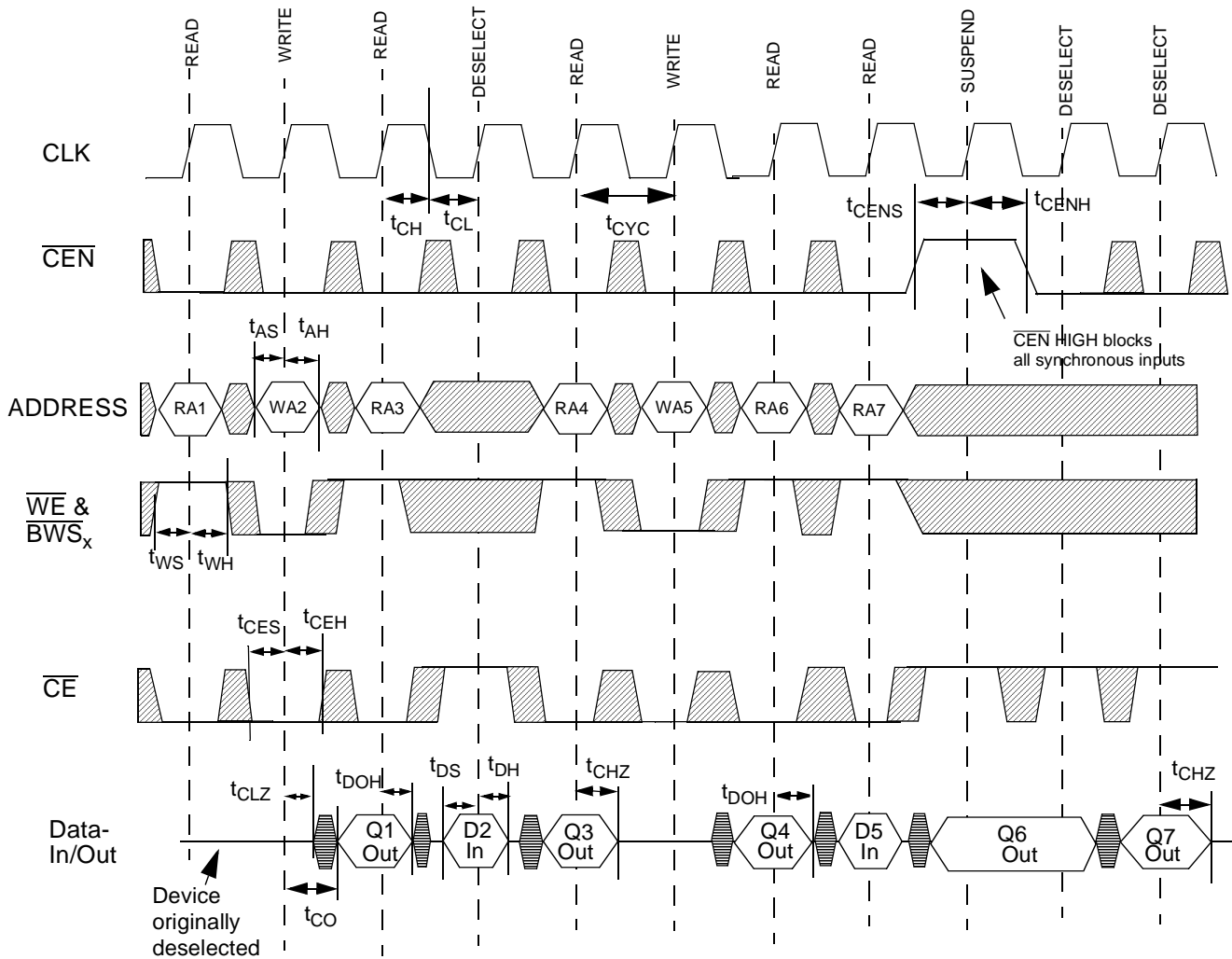
Switching Characteristics Over the Operating Range^[16]

| Parameter | Description | -200 | | -166 | | -133 | | -100 | | Unit |
|---------------------|---|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock | | | | | | | | | | |
| t _{CYC} | Clock Cycle Time | 5 | | 6 | | 7.5 | | 10.0 | | ns |
| F _{MAX} | Maximum Operating Frequency | | 200 | | 166 | | 133 | | 100 | MHz |
| t _{CH} | Clock HIGH | 1.4 | | 1.7 | | 2.0 | | 4.0 | | ns |
| t _{CL} | Clock LOW | 1.4 | | 1.7 | | 2.0 | | 4.0 | | ns |
| Output Times | | | | | | | | | | |
| t _{CDV} | Data Output Valid After CLK Rise | | 3.2 | | 3.5 | | 4.2 | | 5.0 | ns |
| t _{EOV} | \overline{OE} LOW to Output Valid ^[14, 17, 19] | | 3.2 | | 3.5 | | 4.2 | | 5.0 | ns |
| t _{DOH} | Data Output Hold After CLK Rise | 1.5 | | 1.5 | | 1.5 | | 1.5 | | ns |
| t _{CHZ} | Clock to High-Z ^[14, 16, 17, 18, 19] | 1.5 | 3.2 | 1.5 | 3.5 | 1.5 | 3.5 | 1.5 | 3.5 | ns |
| t _{CLZ} | Clock to Low-Z ^[14, 16, 17, 18, 19] | 1.5 | | 1.5 | | 1.5 | | 1.5 | | ns |
| t _{EOHZ} | \overline{OE} HIGH to Output High-Z ^[16, 17, 19] | | 3.0 | | 3.3 | | 4.0 | | 4.8 | ns |
| t _{EOLZ} | \overline{OE} LOW to Output Low-Z ^[16, 17, 19] | 0 | | 0 | | 0 | | 0 | | ns |
| Set-Up Times | | | | | | | | | | |
| t _{AS} | Address Set-Up Before CLK Rise | 1.5 | | 1.5 | | 2.0 | | 2.0 | | ns |
| t _{DS} | Data Input Set-Up Before CLK Rise | 1.5 | | 1.5 | | 2.0 | | 2.0 | | ns |
| t _{CENS} | \overline{CEN} Set-Up Before CLK Rise | 1.5 | | 1.5 | | 2.0 | | 2.0 | | ns |
| t _{WES} | \overline{WE} , \overline{BWS}_x Set-Up Before CLK Rise | 1.5 | | 1.5 | | 2.0 | | 2.0 | | ns |
| t _{ALS} | $\overline{ADV}/\overline{LD}$ Set-Up Before CLK Rise | 1.5 | | 1.5 | | 2.0 | | 2.0 | | ns |
| t _{CES} | Chip Select Set-Up | 1.5 | | 1.5 | | 2.0 | | 2.0 | | ns |
| Hold Times | | | | | | | | | | |
| t _{AH} | Address Hold After CLK Rise | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{DH} | Data Input Hold After CLK Rise | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{CENH} | \overline{CEN} Hold After CLK Rise | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{WEH} | \overline{WE} , \overline{BWS}_x Hold After CLK Rise | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{ALH} | $\overline{ADV}/\overline{LD}$ Hold after CLK Rise | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{CEH} | Chip Select Hold After CLK Rise | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |


Shaded areas contain advance information.

Notes:

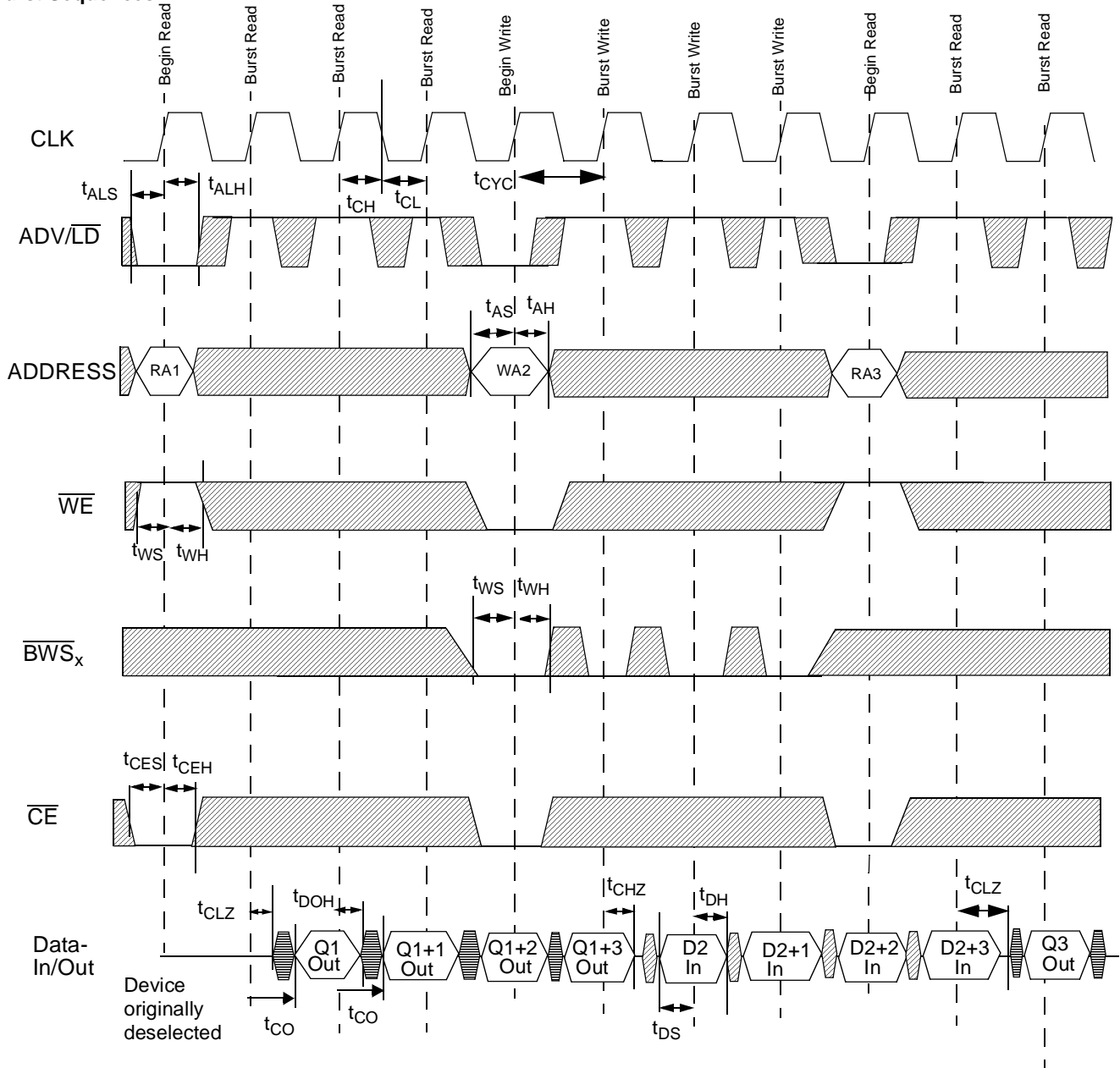
16. AC test conditions assume signal transition time of 2 ns or less, timing reference levels, input pulse levels and output loading shown in part (a) of AC Test Load.
17. t_{CHZ}, t_{CLZ}, t_{EOV}, t_{EOLZ}, and t_{EOHZ} are specified with A/C test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
19. This parameter is sampled and not 100% tested.

Switching Waveforms
READ/WRITE/DESELECT Sequence


The combination of \overline{WE} & \overline{BWS}_x ($x=a, b, c, d$ for CY7C1354V25 & $x=a, b$ for CY7C1356V25) define a write cycle (see Write Cycle Definition table) \overline{CE} is the combination of \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 . All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAX stands for Read Address X, WAX Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{ADV}/\overline{LD}$ held LOW. \overline{OE} held LOW.

 = DON'T CARE  = UNDEFINED

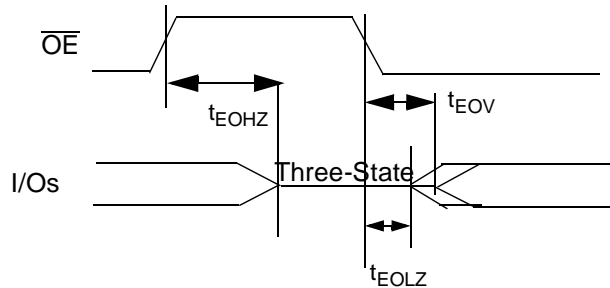
Switching Waveforms (continued)

Burst Sequences


The combination of \overline{WE} & $\overline{BWS}_x(x=a, b, c, d)$ define a write cycle (see Write Cycle Definition table). \overline{CE} is the combination of \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 . All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RA_x stands for Read Address X, WA_x stands for Write Address X, D_x stands for Data-in for location X, Q_x stands for Data-out for location X. \overline{CEN} held LOW. During burst writes, byte writes can be conducted by asserting the appropriate \overline{BWS}_x input signals. Burst order determined by the state of the MODE input. \overline{CEN} held LOW. \overline{OE} held LOW.

▨ = DON'T CARE ▩ = UNDEFINED

Switching Waveforms (continued)

 $\overline{\text{OE}}$ Timing

Ordering Information

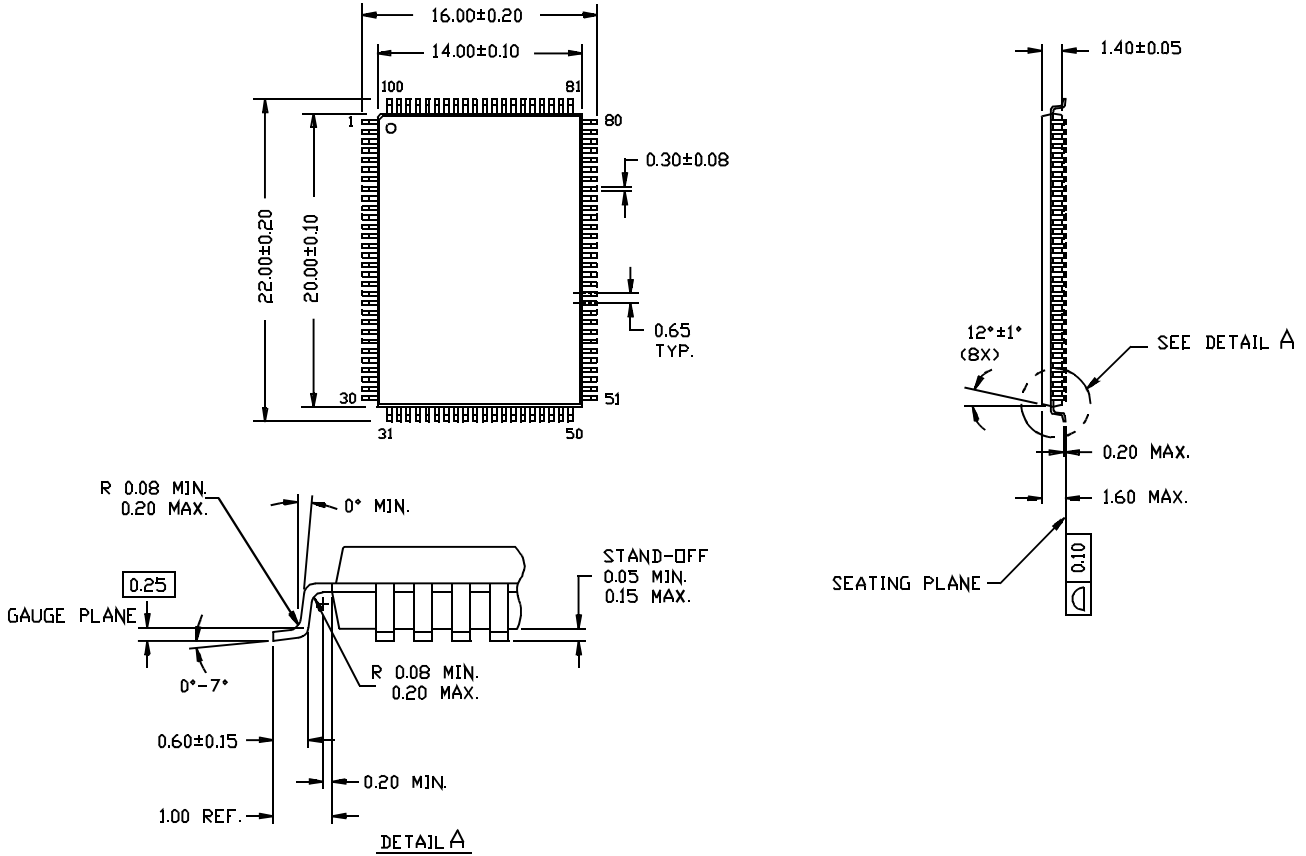
| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------|---|--------------|---|-----------------|
| 200 | CY7C1354V25-200AC/ CY7C1356V25-200AC | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1354V25-200BAC/ CY7C1356V25-200BAC | TBD | 7 x 17 BGA | |
| 166 | CY7C1354V25-166AC/ CY7C1356V25-166AC | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | |
| | CY7C1354V25-166BAC/ CY7C1356V25-166BAC | TBD | 7 x 17 BGA | |
| 133 | CY7C1354V25-133AC/ CY7C1356V25-133AC | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | |
| | CY7C1354V25-133BAC/ CY7C1356V25-133BAC | TBD | 7 x 17 BGA | |
| 100 | CY7C1354V25-100AC/ CY7C1356V25-100AC | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | |
| | CY7C1354V25-100BAC/ CY7C1356V25-100BAC | TBD | 7 x 17 BGA | |

Shaded areas contain advance information.

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.



51-85050-A