Document Title

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

Revision History

Rev. No.	History	Draft Date	Remark
Rev. 0.0	- Preliminary specification release	Oct. 2002	Preliminary
Rev. 0.1	- Update DC CHARACTERISTICS x36 : I_{DD6} : TBD -> 300, I_{DD65} -> 290, I_{DD7} -> 280. x18 : I_{DD6} : TBD -> 290, I_{DD65} -> 280, I_{DD7} -> 270.	Jan. 2003	Preliminary
Rev. 0.2	- Change simbol in DC CHARACTERISTICS I_{DD6}, I_{DD65}, I_{DD7} -> I_{DD65}, I_{DD70}, I_{DD75}	Feb. 2003	Preliminary
Rev. 1.0	- Final Version	Jun. 2003	Final
Rev. 1.1	- Add Single ended differential clock on clock comment.	Jun. 2003	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or cortact Headquarters.

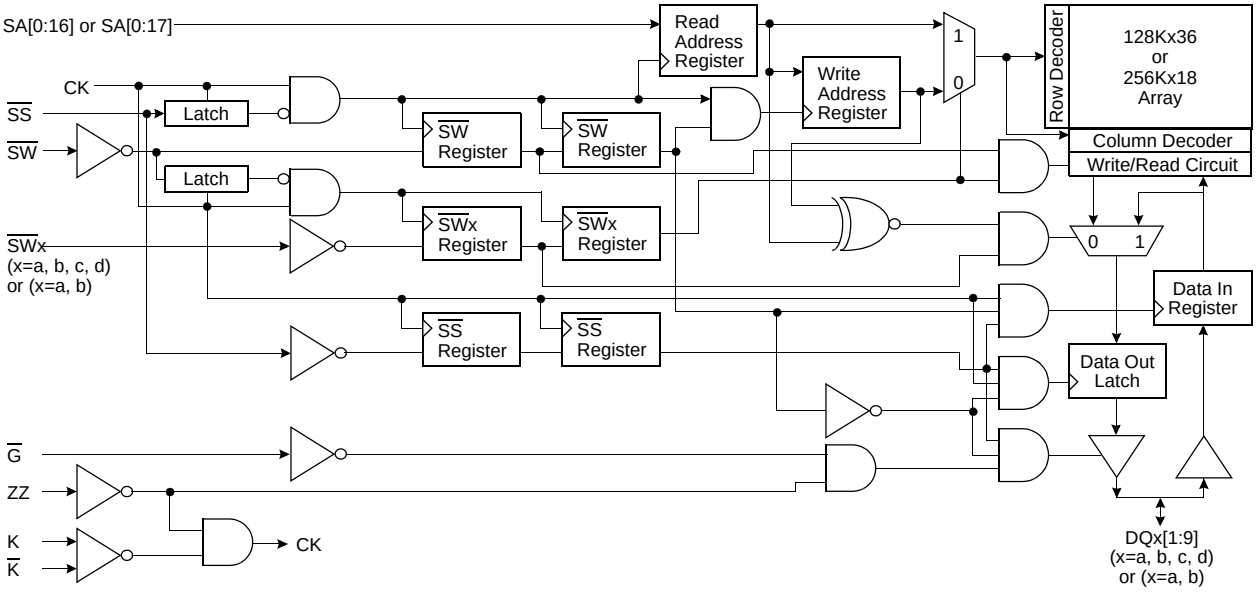
128Kx36 & 256Kx18 Synchronous Pipelined SRAM

FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V V_{DD}, 2.5/3.3V V_{DDQ}.
- LVTTL 2.5/3.3V Input and Output Levels.
- Differential, PECL clock / Single ended or differential LVTTL clock Inputs
- Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mmx22mm).

Organization	Part Number	Cycle Time	Access Time
128Kx36	K7P403623B-H65	6	6.5
	K7P403623B-H70	6.5	7.0
	K7P403623B-H75	7	7.5
256Kx18	K7P401823B-H65	6	6.5
	K7P401823B-H70	6.5	7.0
	K7P401823B-H75	7	7.5

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks(PECL or LVTTL Level)	V_{DDQ}	Output Power Supply
SAn	Synchronous Address Input	M_1, M_2	Read Protocol Mode Pins (M_1=V_{DD}, M_2=V_{SS})
DQn	Bi-directional Data Bus	$\overline{G}$	Asynchronous Output Enable
$\overline{SW}$	Synchronous Global Write Enable	$\overline{SS}$	Synchronous Select
$\overline{SW}$a	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\overline{SW}$b	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\overline{SW}$c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\overline{SW}$d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	V_{SS}	GND
V_{DD}	Core Power Supply	NC	No Connection

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7P403623B(128Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQc_8	DQc_9	V_{SS}	NC*	V_{SS}	DQb_9	DQb_8
E	DQc_6	DQc_7	V_{SS}	$\overline{SS}$	V_{SS}	DQb_7	DQb_6
F	V_{DDQ}	DQc_5	V_{SS}	$\overline{G}$	V_{SS}	DQb_5	V_{DDQ}
G	DQc_3	DQc_4	$\overline{SW}c$	NC*	$\overline{SW}b$	DQb_4	DQb_3
H	DQc_1	DQc_2	V_{SS}	NC*	V_{SS}	DQb_2	DQb_1
J	V_{DDQ}	V_{DD}	NC***	V_{DD}	NC***	V_{DD}	V_{DDQ}
K	DQd_1	DQd_2	V_{SS}	K	V_{SS}	DQa_2	DQa_1
L	DQd_3	DQd_4	$\overline{SW}d$	$\overline{K}$	$\overline{SW}a$	DQa_4	DQa_3
M	V_{DDQ}	DQd_5	V_{SS}	$\overline{SW}$	V_{SS}	DQa_5	V_{DDQ}
N	DQd_6	DQd_7	V_{SS}	SA_{16}	V_{SS}	DQa_7	DQa_6
P	DQd_8	DQd_9	V_{SS}	SA_0	V_{SS}	DQa_9	DQa_8
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	NC	SA_{14}	SA_1	SA_3	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC**	V_{DDQ}

NOTE : 1. NC* is used for the Boundary Scan.
2. NC** is reserved for TRST input.
3. NC*** is reserved for HSTL interface.

KM718FV4022(256Kx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQb_1	NC	V_{SS}	NC*	V_{SS}	DQa_9	NC
E	NC	DQb_2	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa_8
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa_7	V_{DDQ}
G	NC	DQb_3	$\overline{SW}b$	NC*	NC	NC	DQa_6
H	DQb_4	NC	V_{SS}	NC*	V_{SS}	DQa_5	NC
J	V_{DDQ}	V_{DD}	NC***	V_{DD}	NC***	V_{DD}	V_{DDQ}
K	NC	DQb_5	V_{SS}	K	V_{SS}	NC	DQa_4
L	DQb_6	NC	NC	$\overline{K}$	$\overline{SW}a$	DQa_3	NC
M	V_{DDQ}	DQb_7	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb_8	NC	V_{SS}	SA_{16}	V_{SS}	DQa_2	NC
P	NC	DQb_9	V_{SS}	SA_1	V_{SS}	NC	DQa_1
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	SA_{17}	SA_{14}	NC	SA_3	SA_0	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC**	V_{DDQ}

NOTE : 1. NC* is used for the Boundary Scan.
2. NC** is reserved for TRST input.
3. NC*** is reserved for HSTL interface.

FUNCTION DESCRIPTION

The K7P403623B andK7P401823B are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262,144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.
Single differential PECL level K clocks or single ended or differential LVCMOS/LVTTL clock are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.
During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are both sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operations is on the Address and Control Input.
Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(t_{ZZR}) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SWa}$	$\overline{SWb}$	$\overline{SWc}$	$\overline{SWd}$	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	D_{IN}	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	D_{IN}	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	D_{IN}	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	D_{IN}	Write fourth byte
↑	L	X	L	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Write all byte

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Output Supply Voltage Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on any I/O pin Relative to V_{SS}	V_{TERM}	-0.3 to V_{DD}+0.3	V
Maximum Power Dissipation	P_D	1.5	W
Output Short-Circuit Current	I_{OUT}	25	mA
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature	T_{STG}	-65 to 150	°C

NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Output Power Supply Voltage (for 2.5V I/O)	V_{DDQ}	2.375	2.5	2.9	V	
Output Power Supply Voltage (for 3.3V I/O)	V_{DDQ}	3.135	3.3	3.6	V	
Input High Level (for 2.5V I/O)	V_{IH}	1.7	-	V_{DD}+0.3	V	
Input Low Level (for 2.5V I/O)	V_{IL}	-0.3	-	0.7	V	
Input High Level (for 3.3V I/O)	V_{IH}	2.0	-	V_{DD}+0.3	V	
Input Low Level (for 3.3V I/O)	V_{IL}	-0.3	-	0.8	V	
PECL Clock Input High Level	V_{IH}-PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	V_{IL}-PECL	1.490	-	1.825	V	1
Clock Input Signal Voltage	V_{IN}	-0.3	-	3.45	V	2
Clock Input Differential Voltage	V_{DIF}-CLK	0.2	-	V_{DD}+0.6	V	2
Clock Input Common Mode Voltage	V_{CM}-CLK	1.1	-	2.1	V	2
Operating Junction Temperature	T_J	10	-	110	°C	

NOTE

1. For operation with differential PECL clock inputs.
2. For operation with single ended or differential LVCMOS / LVTTL clock input.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD65} I_{DD70} I_{DD75}	-	300 290 280	mA	1, 2
Average Power Supply Operating Current-x18 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD65} I_{DD70} I_{DD75}	-	290 280 270	mA	1, 2
Power Supply Standby Current (V_{IN}=V_{IH} or V_{IL}, ZZ=V_{IH})	I_{SB}	-	120	mA	1
Input Leakage Current (V_{IN}=V_{SS} or V_{DDQ})	I_{LI}	-1	1	μA	
Output Leakage Current (V_{OUT}=V_{SS} or V_{DDQ}, ZZ=V_{IH}, $\overline{G}$=V_{IH})	I_{LO}	-1	1	μA	
Output High Voltage(I_{OH}=-4mA) for V_{DDQ}=3.3V Output High Voltage(I_{OH}=-4mA) for V_{DDQ}=2.5V	V_{OH1} V_{OH2}	2.4 2.0	V_{DDQ}	V	
Output Low Voltage(I_{OL}=4mA)	V_{OL}	V_{SS}	0.4	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.

PIN CAPACITANCE

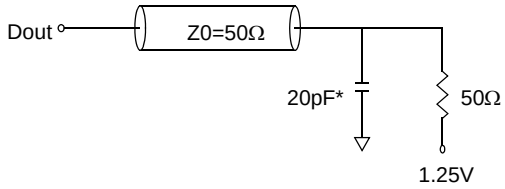
Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{IN}	-	5	pF
Output Capacitance	C_{OUT}	-	7	pF

NOTE : Periodically sampled and not 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V_{DD}	3.15~3.45	V
Output Power Supply Voltage	V_{DDQ}	2.4~2.6	V
Input High/Low Level	V_{IH}/V_{IL}	1.7/0.7	V
Clock Input High/Low Level(PECL)	V_{IH}/V_{IL}	2.4/1.5	V
Input Rise/Fall Time	T_R/T_F	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T_R/T_F	1.0/1.0	ns
Input and Out Timing Reference Level		1.25	V
Clock Input Timing Reference Level		Cross Point	V

AC TEST OUTPUT LOAD

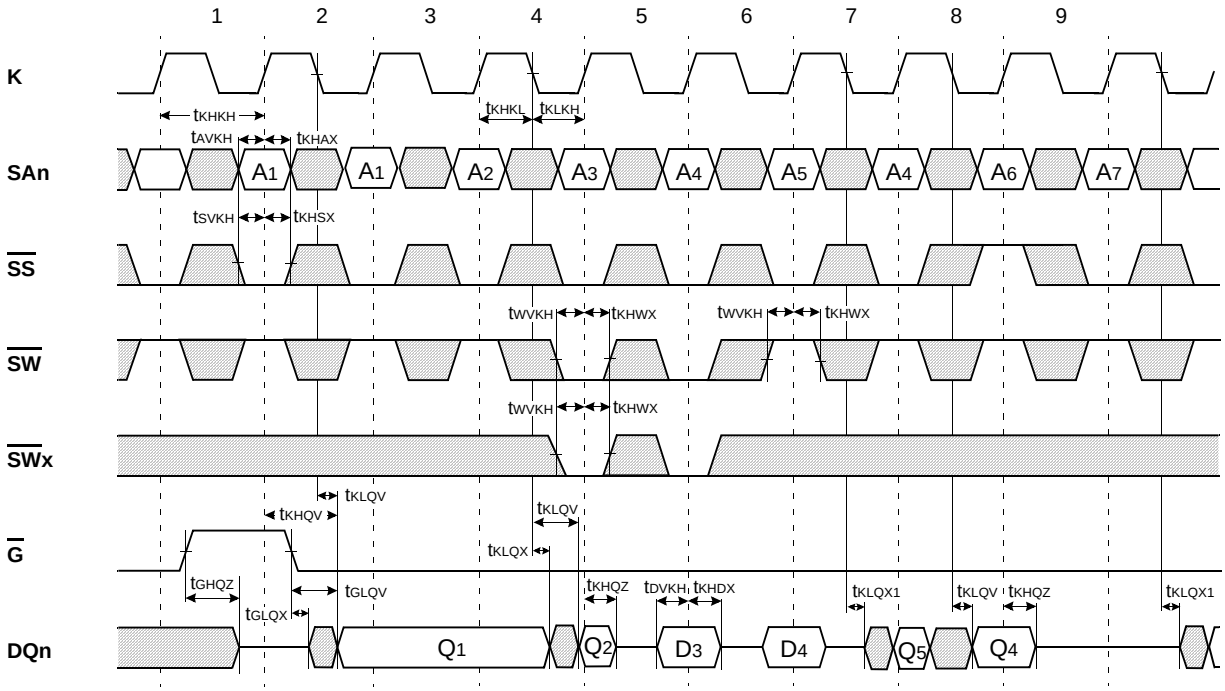


*Capacitive load consists of all components of the tester environment

AC CHARACTERISTICS

Parameter	Symbol	-65		-70		-75		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	6.0	-	6.5	-	7.0	-	ns	
Clock High Pulse Width	t_{KHKL}	2.0	-	2.0	-	2.0	-	ns	
Clock Low Pulse Width	t_{KLKH}	2.0	-	2.0	-	2.0	-	ns	
Clock High to Output Valid	t_{KHQV}	-	6.5	-	7.0	-	7.5	ns	
Clock Low to Output Valid	t_{KLQV}	-	2.5	-	2.5	-	3.0	ns	
Clock Low to Output Hold	t_{KLQX}	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	t_{AVKH}	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	t_{KHAX}	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	t_{DVKH}	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	t_{KHDX}	1.0	-	1.0	-	1.0	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Setup Time	t_{WVKH}	0.5	-	0.5	-	0.5	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Hold Time	t_{KHWX}	1.0	-	1.0	-	1.0	-	ns	
$\overline{SS}$ Setup Time	t_{SVKH}	0.5	-	0.5	-	0.5	-	ns	
$\overline{SS}$ Hold Time	t_{KHSX}	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	t_{KHQZ}	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	t_{KLQX1}	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ High to Output High-Z	t_{GHQZ}	-	2.5	-	3.0	-	3.5	ns	
$\overline{G}$ Low to Output Low-Z	t_{GLQX}	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	t_{GLQV}	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	t_{ZZE}	-	15	-	15	-	15	ns	
ZZ Low to Recovery(Wake-up Time)	t_{ZZR}	-	20	-	20	-	20	ns	

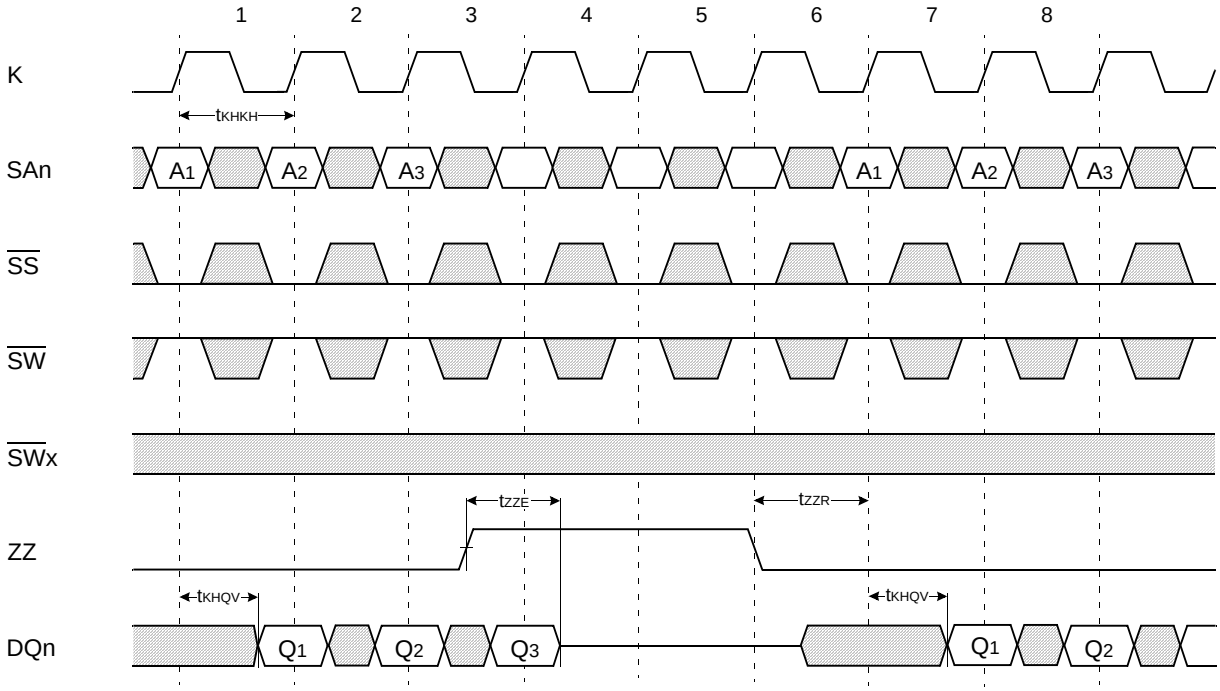
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES



NOTE

1. D3 is the input data written in memory location A3.
2. Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.
3. Data is valid at the output at the later of t_{KHQV} following the rising clock edge, or t_{KLQV} following the fallowing clock edge.
4. When $\overline{SS}$ is sampled high or $\overline{SW}$ is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than t_{KHQZ} following the rising clock edge.
5. When $\overline{SS}$ is low and $\overline{SW}$ is high on the rising edge of clock, the outputs go into Low-Z state(being driven) no earlier than t_{KLQX1} following the next falling edge of clock.
6. When the SRAM is deselected, the output goes Hi-Z at t_{KHQZ} following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until t_{KLQX1} after the falling clock edge.

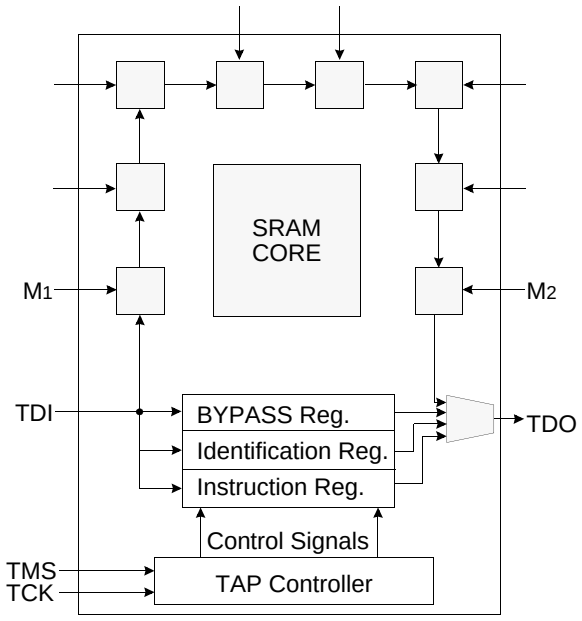
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



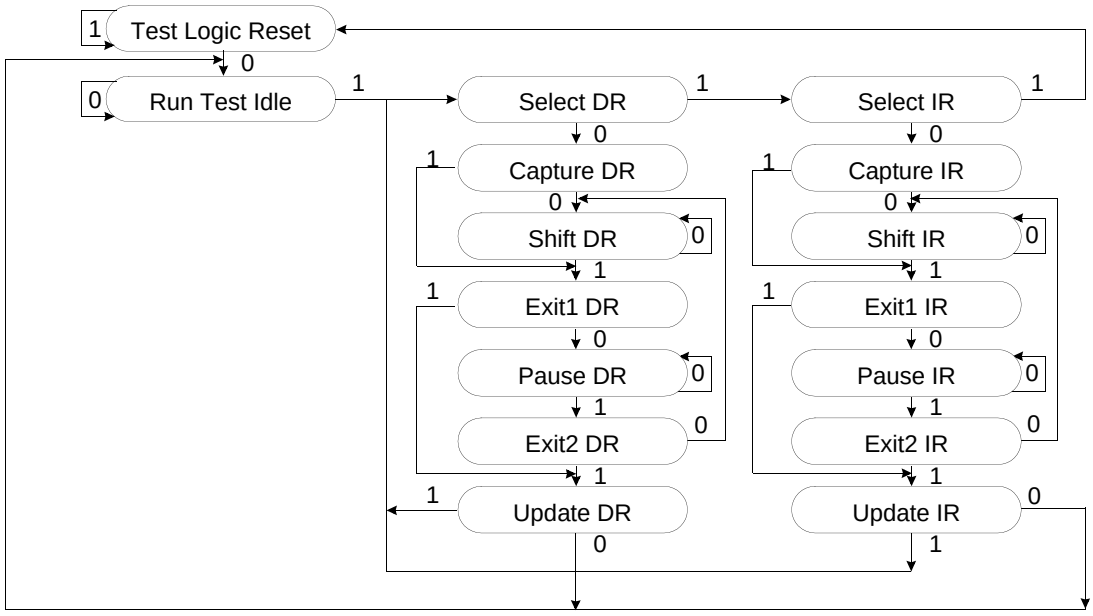
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to VSS when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	xxxxxx	00001001110	1
256Kx18	0000	00110 00011	xxxxxx	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA_9		SA_8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA_{10}		SA_7	5A	33
39	3C	SA_{11}		SA_6	5C	32
40	2C	SA_{12}		SA_5	6C	31
41	2A	SA_{13}		SA_4	6A	30
42	2D	DQc_9		DQb_9	6D	29
43	1D	DQc_8		DQb_8	7D	28
44	2E	DQc7		DQb_7	6E	27
45	1E	DQc_6		DQb_6	7E	26
46	2F	DQc_5		DQb_5	6F	25
47	2G	DQc_4		DQb_4	6G	24
48	1G	DQc_3		DQb_3	7G	23
49	2H	DQc_2		DQb_2	6H	22
50	1H	DQc_1		DQb_1	7H	21
51	3G	$\overline{SW}c$		$\overline{SW}b$	5G	20
52	4D	NC		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	NC		$\overline{K}$	4L	17
55	4H	NC		$\overline{SW}a$	5L	16
56	4M	$\overline{SW}$		DQa_1	7K	15
57	3L	$\overline{SW}d$		DQa_2	6K	14
58	1K	DQd_1		DQa_3	7L	13
59	2K	DQd_2		DQa_4	6L	12
60	1L	DQd_3		DQa_5	6M	11
61	2L	DQd_4		DQa_6	7N	10
62	2M	DQd_5		DQa_7	6N	9
63	1N	DQd_6		DQa_8	7P	8
64	2N	DQd_7		DQa_9	6P	7
65	1P	DQd_8		ZZ	7T	6
66	2P	DQd_9		SA_3	5T	5
67	3T	SA_{14}		SA_2	6R	4
68	2R	SA_{15}		SA_1	4T	3
69	4N	SA_{16}		SA_0	4P	2
70	3R	M_1		M_2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA_9		SA_8	5B	25
27	2B	NC		NC	6B	24
28	3A	SA_{10}		SA_7	5A	23
29	3C	SA_{11}		SA_6	5C	22
30	2C	SA_{12}		SA_5	6C	21
31	2A	SA_{13}		SA_4	6A	20
				DQa_9	6D	19
32	1D	DQb_1				
33	2E	DQb_2				
				DQa_8	7E	18
				DQa_7	6F	17
34	2G	DQb_3				
				DQa_6	7G	16
				DQa_5	6H	15
35	1H	DQb_4				
36	3G	$\overline{SW}b$				
37	4D	NC		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	NC		$\overline{K}$	4L	12
40	4H	NC		$\overline{SW}a$	5L	11
41	4M	$\overline{SW}$		DQa_4	7K	10
42	2K	DQb_5		DQa_3	6L	9
43	1L	DQb_6				
44	2M	DQb_7		DQa_2	6N	8
45	1N	DQb_8		DQa_1	7P	7
				ZZ	7T	6
46	2P	DQb_9		SA_3	5T	5
47	3T	SA_{14}		SA_2	6R	4
48	2R	SA_{15}				
49	4N	SA_{16}		SA_1	4P	3
50	2T	SA_{17}		SA_0	6T	2
51	3R	M_1		M_2	5R	1

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	1.7	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.8	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.1	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

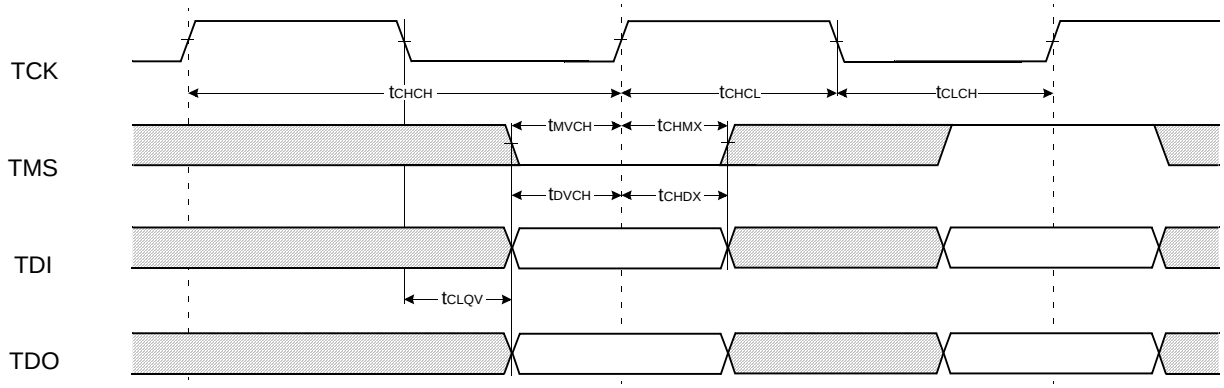
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load.

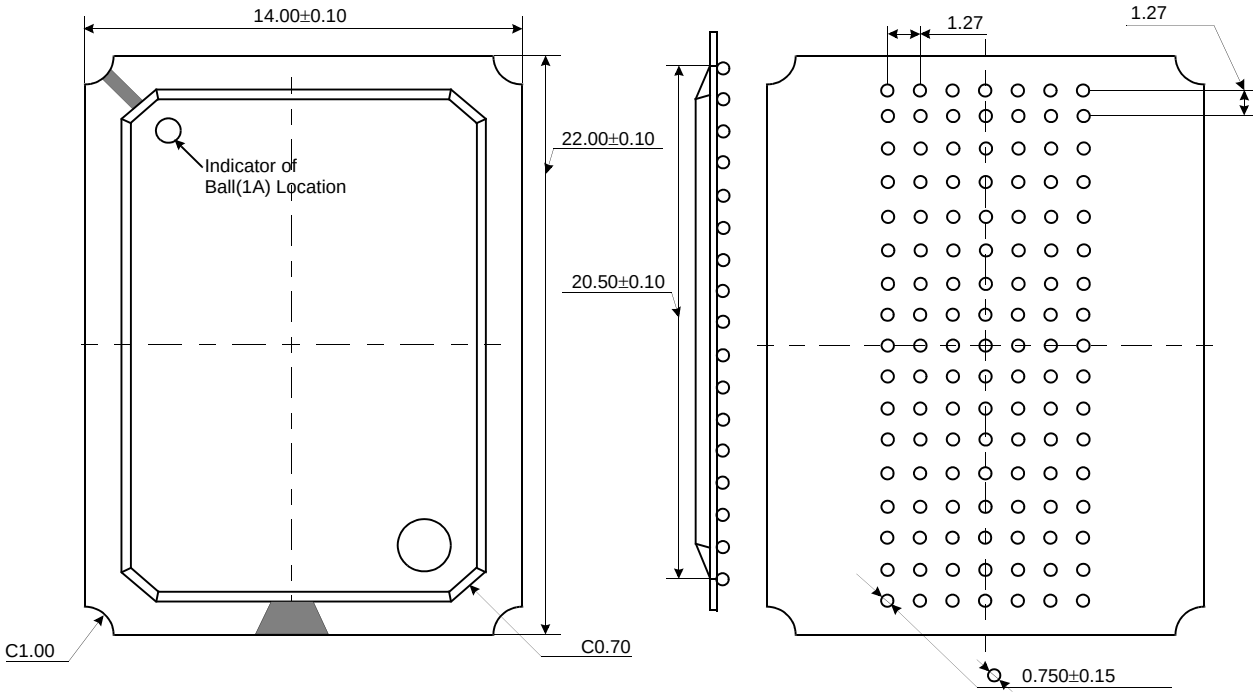
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient	Theta_JA	TBD	°C/W	
Junction to Case	Theta_JC	TBD	°C/W	
Junction to Solder Ball	Theta_JB	TBD	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times Theta\_JA$.