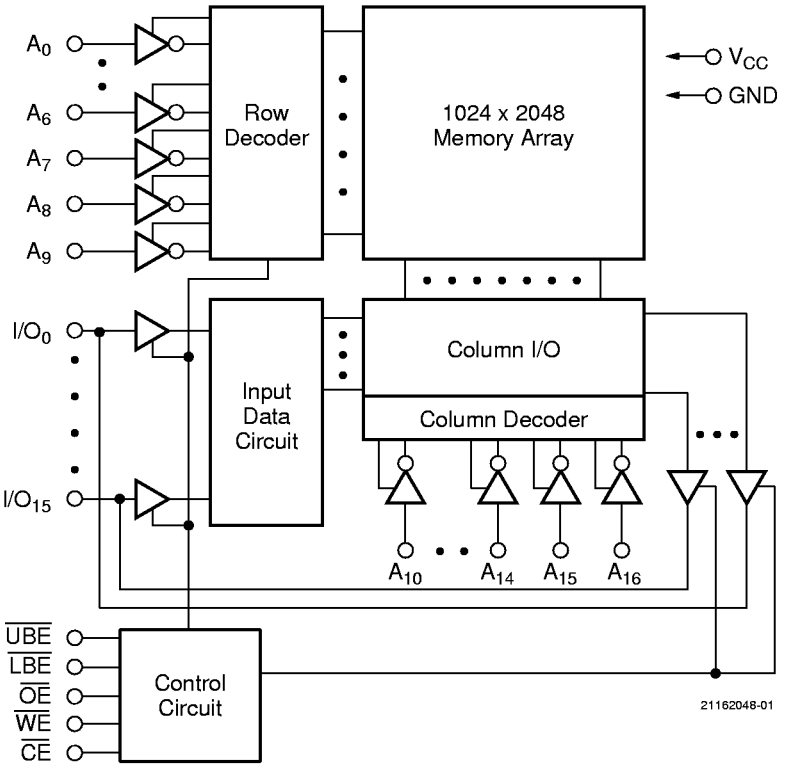
Features

- High-speed: 55, 70 ns
- Ultra low CMOS standby current of 2µA (max.)
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention current (V_{CC} = 2V)
- Extended Operating Voltage: 2.3V – 3.6V
- Packages
  - 44-pin TSOP (Standard)
  - 48 BGA

Description

The V62C21162048 is a 2,097,152-bit static random-access memory organized as 131,072 words by 16 bits. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power		Temperature Mark
	T	B	55	70	L	LL	
0°C to 70°C	•	•	•	•	•	•	Blank
–40°C to +85°C	•	•	•			•	I

Pin Descriptions

A_0–A_{16} Address Inputs
These 17 address inputs select one of the 128K x 16 bit segments in the RAM.

$\overline{CE}$ Chip Enable Input
$\overline{CE}$ is active LOW. It must be active to read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when deselected.

$\overline{OE}$ Output Enable Input
The output enable input is active LOW. When $\overline{OE}$ is Low with $\overline{CE}$ Low and $\overline{WE}$ High, data will be presented on the I/O pins. The I/O pins will be in the high impedance state when $\overline{OE}$ is High.

$\overline{UBE}$, $\overline{LBE}$ Byte Enable
Active low inputs. These inputs are used to enable the upper or lower data byte.

$\overline{WE}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present at the I/O pins; when $\overline{WE}$ is LOW and $\overline{OE}$ is HIGH, the data present on the I/O pins will be written into the selected memory locations.

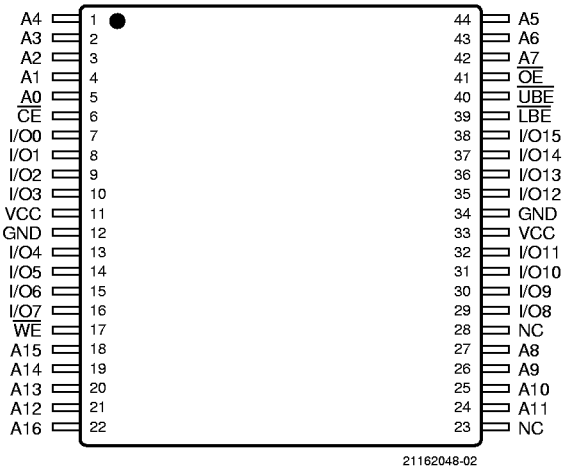
I/O_0–I/O_{15} Data Input and Data Output Ports
These 16 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

GND Ground

Pin Configurations (Top View)

44-Pin TSOP-II (Standard)



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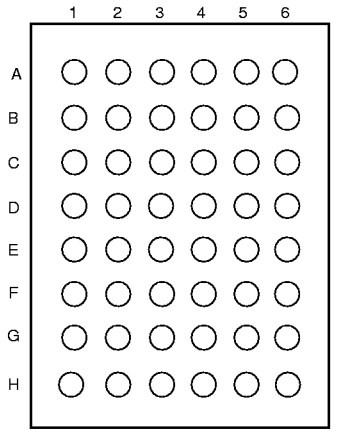
48 BGA



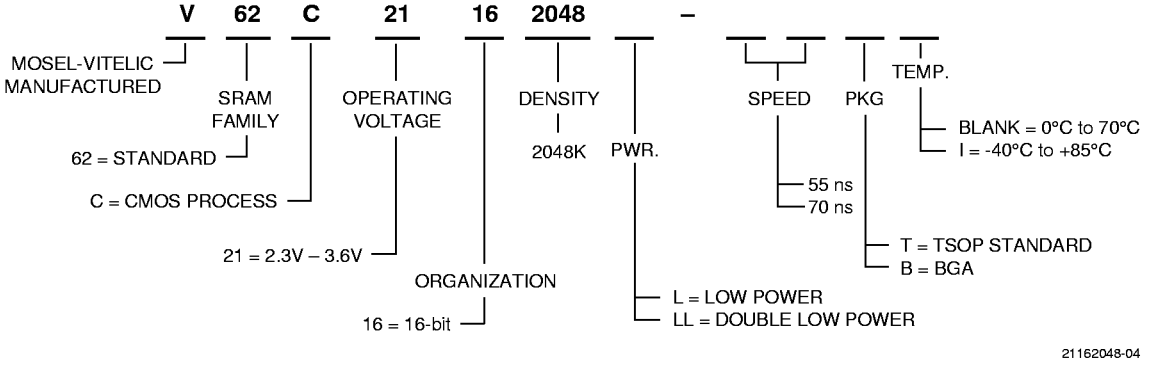
TOP VIEW

	1	2	3	4	5	6
A	$\overline{BLE}$	OE	A0	A1	A2	NC
B	I/O8	$\overline{BHE}$	A3	A4	$\overline{CE}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	VSS	I/O11	NC	A7	I/O3	VCC
E	VCC	I/O12	NC	A16	I/O4	VSS
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	$\overline{WE}$	I/O7
H	NC	A8	A9	A10	A11	NC

Note: NC means no connect.
21162048-03

TOP VIEW

Part Number Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Industrial	Units
V_{CC}	Supply Voltage	-0.5 to V_{CC} + 0.5	-0.5 to V_{CC} + 0.5	V
V_N	Input Voltage	-0.5 to V_{CC} + 0.5	-0.5 to V_{CC} + 0.5	V
V_{DQ}	Input/Output Voltage Applied	V_{CC} + 0.3	V_{CC} + 0.3	V
T_{BIAS}	Temperature Under Bias	-10 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C

NOTE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance* T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:
1. This parameter is guaranteed and not tested.

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{UBE}$	$\overline{LBE}$	I/O_{8-15} Operation	I/O_{0-7} Operation
Standby	H	X	X	X	X	High Z	High Z
Output Disable	L	X	X	H	H	High Z	High Z
Output Disable	L	H	H	X	X	High Z	High Z
Read	L	L	H	L	L	D_{OUT}	D_{OUT}
Read	L	L	H	L	H	D_{OUT}	High Z
Read	L	L	H	H	L	High Z	D_{OUT}
Write	L	X	L	L	L	D_{IN}	D_{IN}
Write	L	X	L	L	H	D_{IN}	High Z
Write	L	X	L	H	L	High Z	D_{IN}

NOTE:
X = Don't Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, V_{CC} = 2.3V – 3.6V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage(1,2)		-0.3	—	0.4	V
V_{IH}	Input HIGH Voltage(1)		2.2	—	V_{CC} + 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-1	—	1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	-1	—	1	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	—	—	V

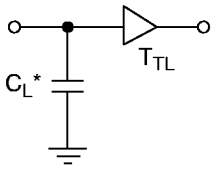
Symbol	Parameter	Power	Com.(4)	Ind.	Units
I_{CC}	Operating Power Supply Current, $\overline{CE}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	L	5	6	mA
		LL	4	5	
I_{CC1}	Average Operating Current, $\overline{CE}_1$ = V_{IL}, Output Open, V_{CC} = Max., f = f_{MAX}(3)		50	60	mA
I_{SB}	TTL Standby Current $\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}(3)	L	0.5	1	mA
		LL	0.2	1	
I_{SB1}	CMOS Standby Current, $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, V_{CC} = Max., f = 0	L	10	20	µA
		LL	2	5	

NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -3.0V for pulse width < 20ns.
3. f_{MAX} = $1/t_{RC}$.
4. Maximum values.

AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise and Fall Times	5 ns
Timing Reference Levels	1.4V
Output Load	see below

AC Test Loads and Waveforms



* Includes scope and jig capacitance

C_L = 30 pF + 1 T_{TL} Load

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Key to Switching Waveforms

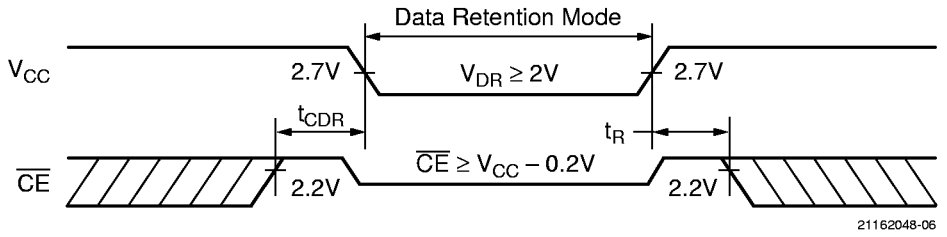
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Data Retention Characteristics

Symbol	Parameter		Power	Min.	Typ.(2)	Max.	Units
V_{DR}	V_{CC} for Data Retention $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$			2.0	—	3.6	V
I_{CCDR}	Data Retention Current $\overline{CE} \geq V_{DR} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	Com'l	L	—	1	2	µA
			LL	—	0.5	1	
		Ind.	L	—	—	5	
			LL	—	—	3	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time (see Retention Waveform)			t_{RC}(1)	—	—	ns

NOTES:
1. t_{RC} = Read Cycle Time
2. T_A = +25°C.

Low V_{CC} Data Retention Waveform ($\overline{CE}$ Controlled)



AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

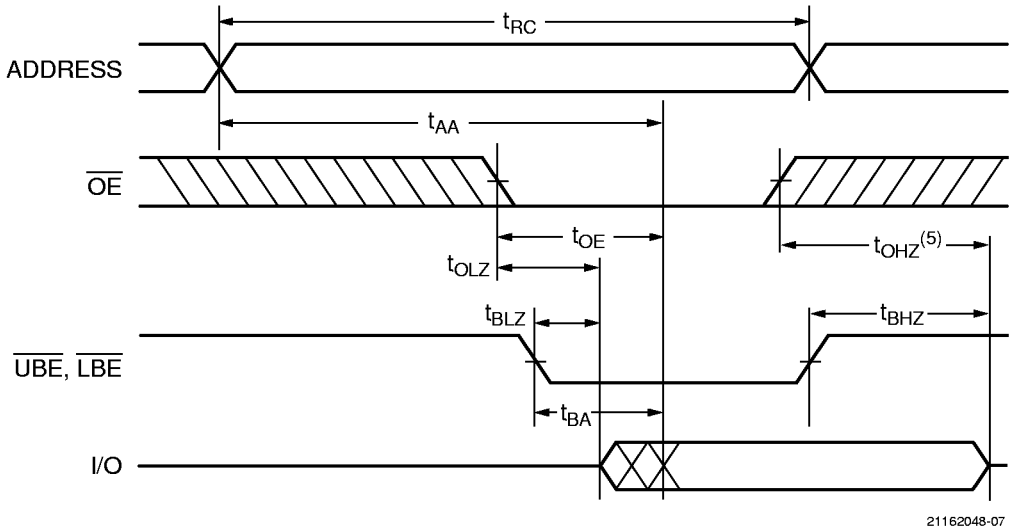
Parameter Name	Parameter	55		-70		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{ACS}	Chip Enable Access Time	—	55	—	70	ns
t_{BA}	$\overline{UBE}$, $\overline{LBE}$ Access Time	—	35	—	35	ns
t_{OE}	Output Enable to Output Valid	—	35	—	35	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	—	10	—	ns
t_{BLZ}	$\overline{UBE}$, $\overline{LBE}$ to Output in Low Z	5	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	ns
t_{CHZ}	Chip Disable to Output in High Z	0	25	0	25	ns
t_{OHZ}	Output Disable to Output in High Z	0	25	0	25	ns
t_{BHZ}	$\overline{UBE}$, $\overline{LBE}$ to Output in High Z	0	25	0	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	ns

Write Cycle

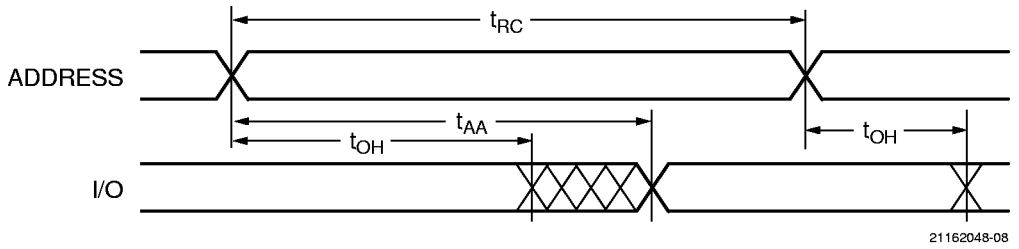
Parameter Name	Parameter	55		-70		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{CW}	Chip Enable to End of Write	50	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	50	—	60	—	ns
t_{WP}	Write Pulse Width	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{WHZ}	Write to Output High-Z	0	10	0	25	ns
t_{WLZ}	Write to Output Low Z	3	—	5	—	ns
t_{DW}	Data Setup to End of Write	25	—	30	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	ns
t_{BW}	$\overline{UBE}$, $\overline{LBE}$ to End of Write	50	—	60	—	ns

Switching Waveforms (Read Cycle)

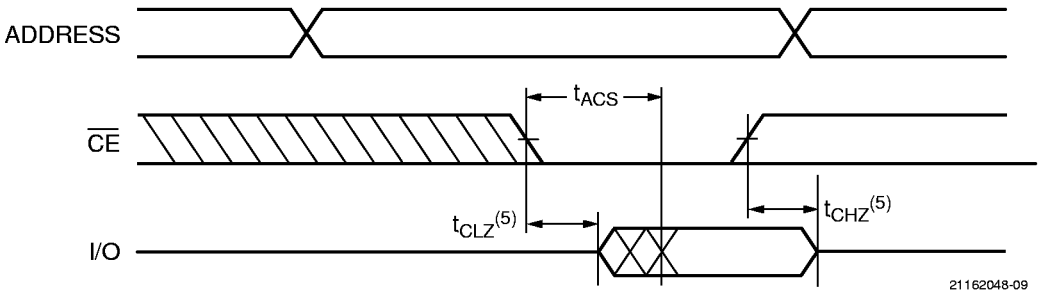
Read Cycle 1(1, 2)



Read Cycle 2(1, 2, 4, 6)



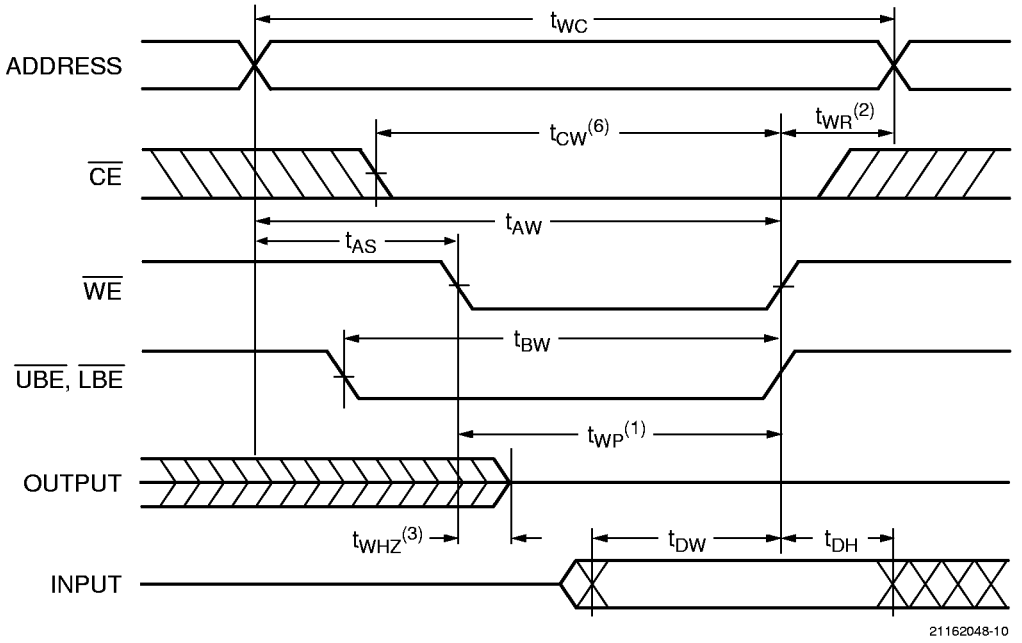
Read Cycle 3(1, 3, 4, 6)



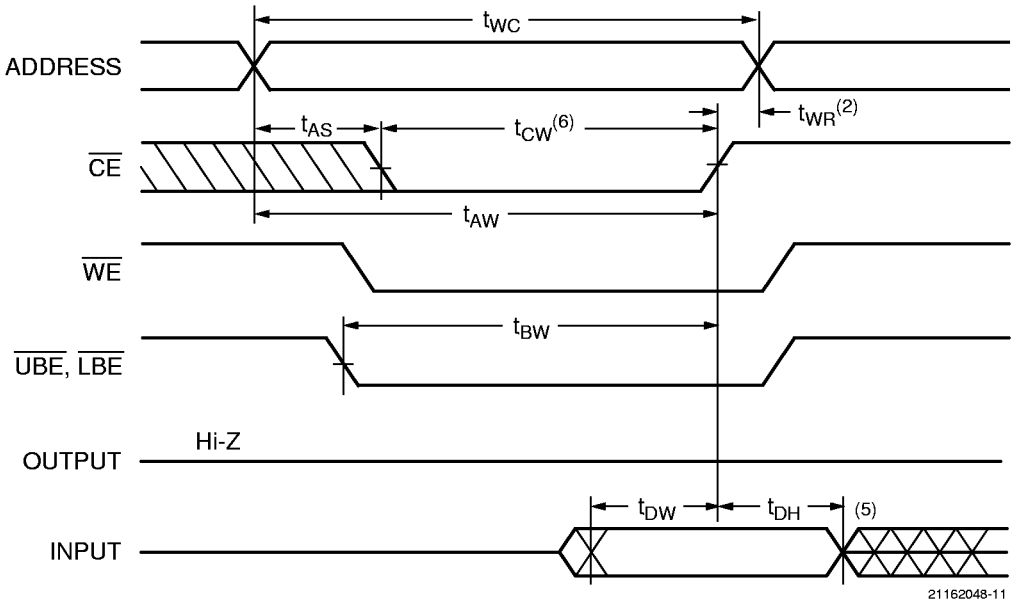
NOTES:
1. $\overline{WE}$ = V_{IH}.
2. $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.
6. $\overline{UBE}$ = V_{IL}, $\overline{LBE}$ = V_{IL}.

Switching Waveforms (Write Cycle)

Write Cycle 1 ($\overline{WE}$ Controlled)[4]



Write Cycle 2 ($\overline{CE}$ Controlled)[4]

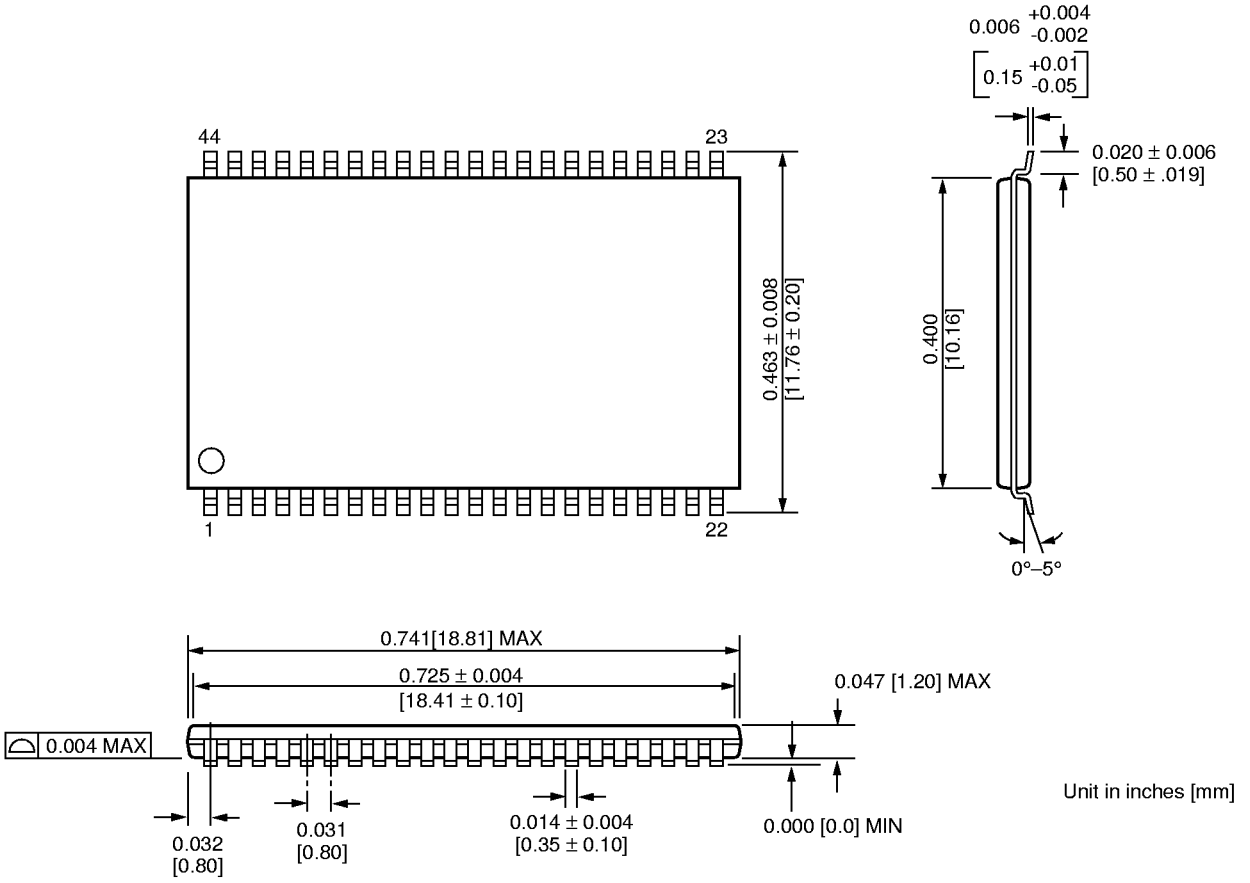


NOTES:

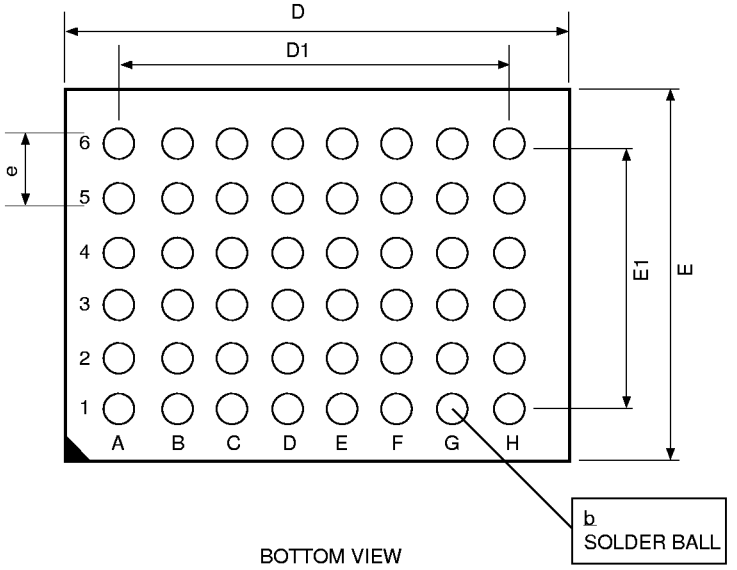
1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE}$ = V_{IL} or V_{IH}. However it is recommended to keep $\overline{OE}$ at V_{IH} during write cycle to avoid bus contention.
5. If $\overline{CE}$ is LOW during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from $\overline{CE}$ going low to the end of write.

Package Diagrams

44-pin 400 mil TSOP-II

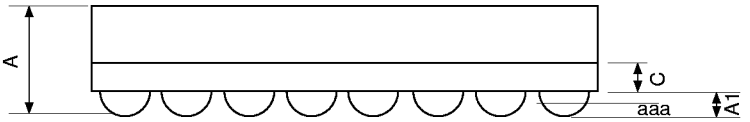


48 Ball—9x12 fpBGA (Ultra Low Power)



BOTTOM VIEW

SYMBOL	UNIT.MM
A	1.05+0.15
A1	0.25±0.05
b	0.35±.0.05
c	0.30(TYP)
D	12.00±0.10
D1	5.25
E	9.00±0.10
E1	3.75
e	0.75TYP
aaa	0.10



SIDE VIEW