

TOSHIBA Field Effect Transistor Silicon N/P Channel MOS Type(π-MOSVI)

# SSM6L09FU

Power Management Switch  
High Speed Switching Applications

- Small package
- Low on-resistance      Q1:  $R_{DS(ON)} = 0.7 \Omega$  (max) (@ $V_{GS} = 10 V$ )  
                                      Q2:  $R_{DS(ON)} = 2.7 \Omega$  (max) (@ $V_{GS} = -10 V$ )

## Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DSS}$	30	V
Gate-Source voltage		$V_{GSS}$	±20	V
Drain current	DC	$I_D$	400	mA
	Pulse	$I_{DP}$	800	

## Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DSS}$	-30	V
Gate-Source voltage		$V_{GSS}$	±20	V
Drain current	DC	$I_D$	-200	mA
	Pulse	$I_{DP}$	-400	

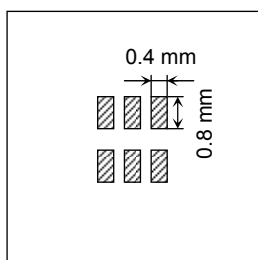
## Absolute Maximum Ratings (Q1, Q2 common) (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power dissipation	$P_D$ (Note 1)	300	mW
Channel temperature	$T_{ch}$	150	°C
Storage temperature range	$T_{stg}$	-55~150	°C

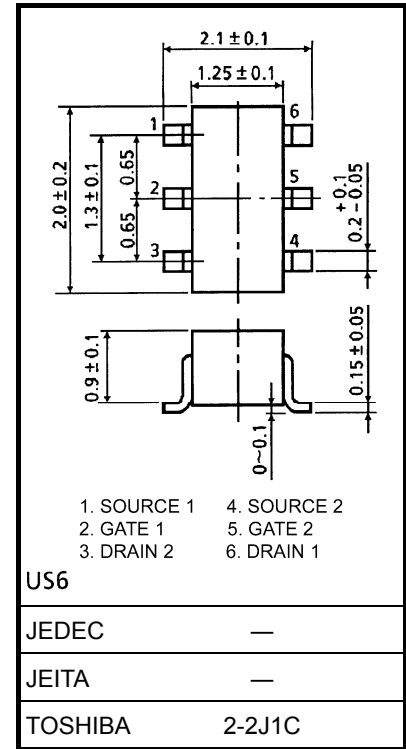
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board  
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.32 mm<sup>2</sup> × 6)

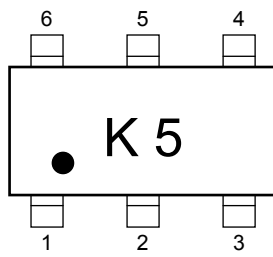


Unit: mm

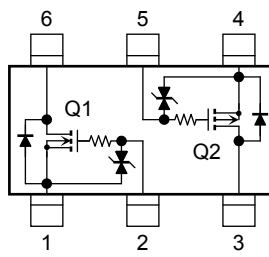


Weight: 6.8 mg (typ.)

## Marking(top view)



## Equivalent Circuit



## Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

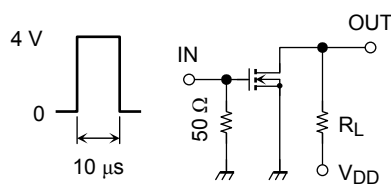
## Q1 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0$	30	—	—	V	
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0$	—	—	1	$\mu\text{A}$	
Gate threshold voltage	$V_{th}$	$V_{DS} = 5\text{ V}, I_D = 0.1\text{ mA}$	1.1	—	1.8	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 5\text{ V}, I_D = 200\text{ mA}$ (Note2)	270	—	—	mS	
Drain-Source on-resistance	$R_{DS(ON)}$	$I_D = 200\text{ mA}, V_{GS} = 10\text{ V}$ (Note2)	—	0.5	0.7	$\Omega$	
		$I_D = 200\text{ mA}, V_{GS} = 4\text{ V}$ (Note2)	—	0.8	1.2		
		$I_D = 200\text{ mA}, V_{GS} = 3.3\text{ V}$ (Note2)	—	1.0	1.7		
Input capacitance	$C_{iss}$	$V_{DS} = 5\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	20	—	pF	
Reverse transfer capacitance	$C_{rss}$		—	7	—	pF	
Output capacitance	$C_{oss}$		—	16	—	pF	
Switching time	Turn-on time	$t_{on}$	$V_{DD} = 5\text{ V}, I_D = 200\text{ mA},$ $V_{GS} = 0\text{ to }4\text{ V}$	—	72	—	ns
	Turn-off time	$t_{off}$		—	68	—	

Note2: Pulse test

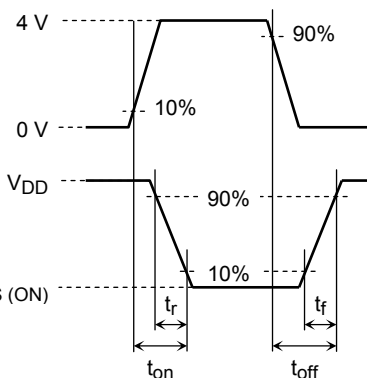
## Switching Time Test Circuit

(a) Test circuit



$V_{DD} = 5\text{ V}$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 ( $Z_{out} = 50\ \Omega$ )  
 Common Source  
 $T_a = 25^\circ\text{C}$

(b)  $V_{IN}$



(c)  $V_{OUT}$

## Precaution

$V_{th}$  can be expressed as the voltage between the gate and source when the low operating current value is  $I_D = 0.1\text{ mA}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires a higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .)

Be sure to take this into consideration when using the device.

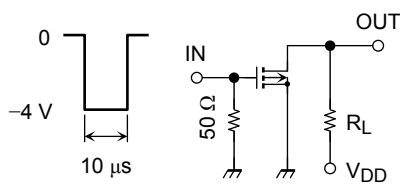
## Q2 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0$	-30	—	—	V
Drain cut-off current	$I_{DSS}$	$V_{DS} = -30 \text{ V}, V_{GS} = 0$	—	—	-1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = -5 \text{ V}, I_D = -0.1 \text{ mA}$	-1.1	—	-1.8	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -5 \text{ V}, I_D = -100 \text{ mA}$ (Note3)	115	—	—	mS
Drain-Source on-resistance	$R_{DS(ON)}$	$I_D = -100 \text{ mA}, V_{GS} = -10 \text{ V}$ (Note3)	—	2.1	2.7	$\Omega$
		$I_D = -100 \text{ mA}, V_{GS} = -4 \text{ V}$ (Note3)	—	3.3	4.2	
		$I_D = -100 \text{ mA}, V_{GS} = -3.3 \text{ V}$ (Note3)	—	4.0	6.0	
Input capacitance	$C_{iss}$	$V_{DS} = -5 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	22	—	pF
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = -5 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	5	—	pF
Output capacitance	$C_{oss}$	$V_{DS} = -5 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	14	—	pF
Switching time	Turn-on time	$t_{on}$	—	85	—	ns
	Turn-off time	$t_{off}$		85		

Note3: Pulse test

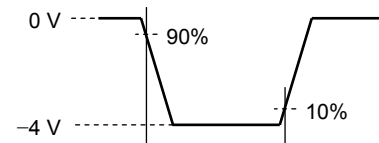
## Switching Time Test Circuit

### (a) Test circuit

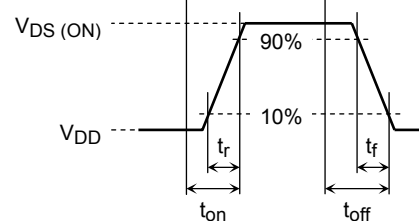


$V_{DD} = -5 \text{ V}$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5 \text{ ns}$   
 $(Z_{out} = 50 \Omega)$   
 Common Source  
 $T_a = 25^\circ\text{C}$

### (b) $V_{IN}$



### (c) $V_{OUT}$

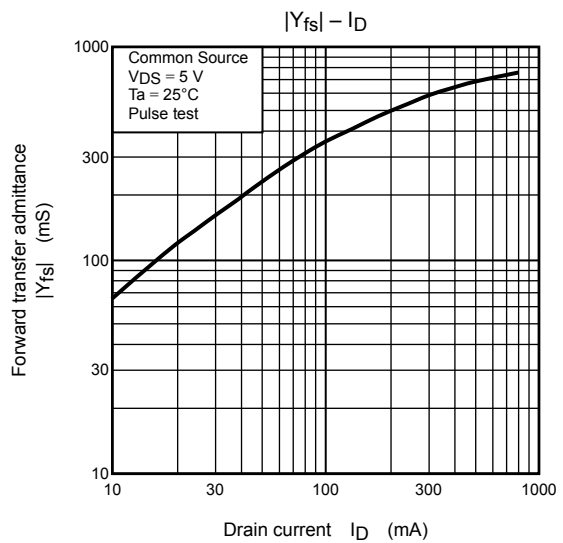
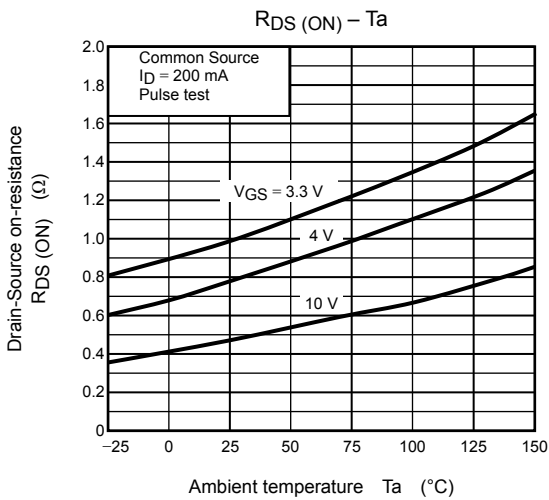
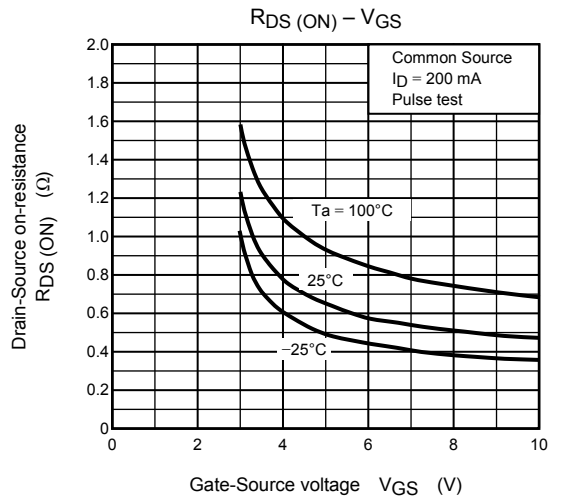
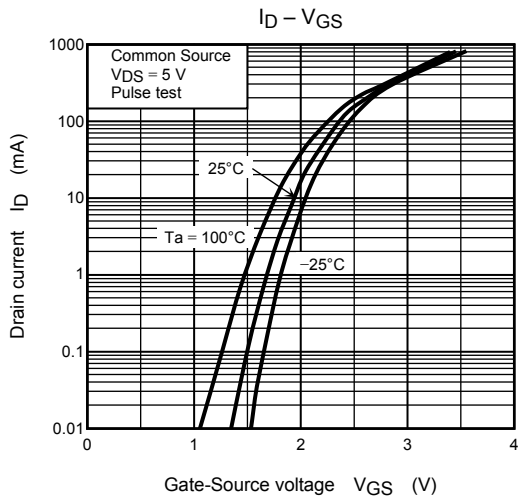
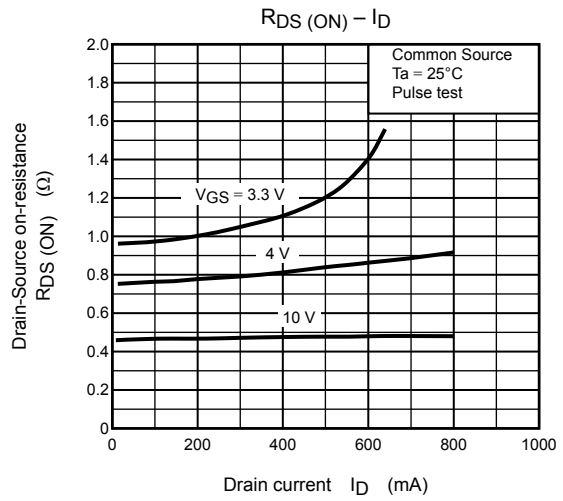
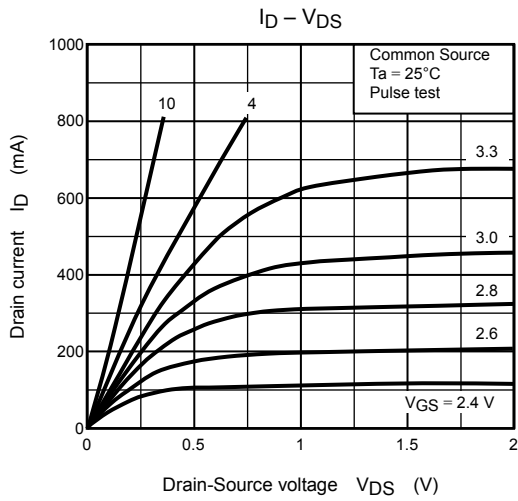


## Precaution

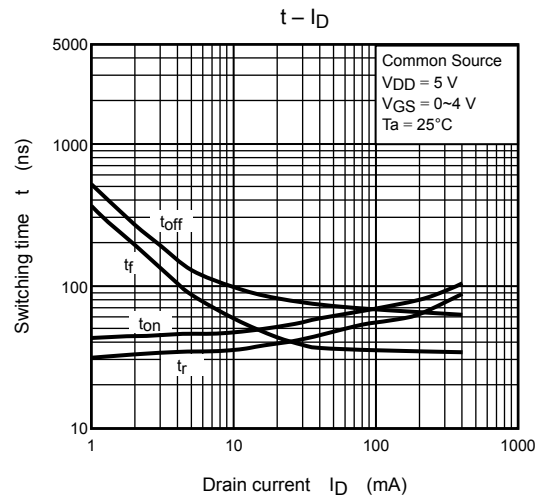
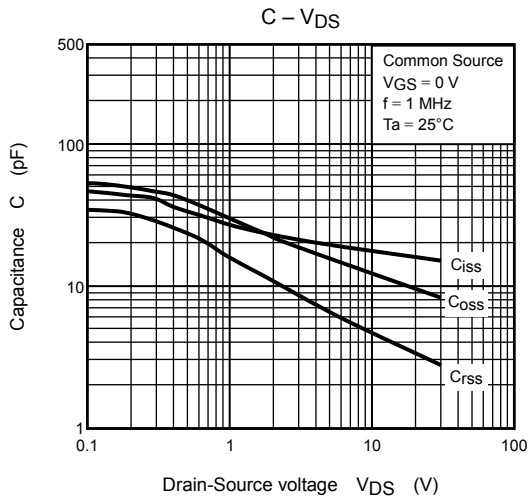
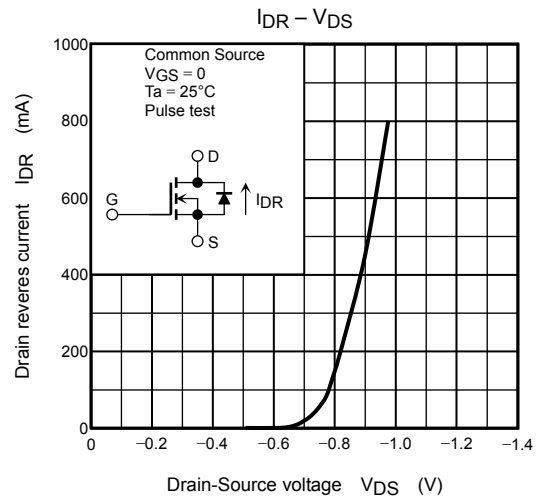
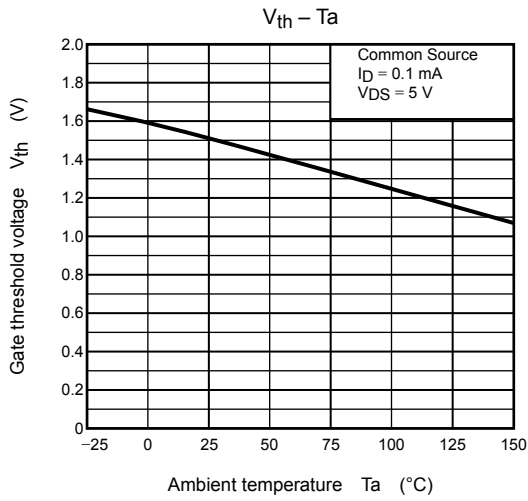
$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = -0.1 \text{ mA}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires lower voltage than  $V_{th}$ . (Relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ )

Please take this into consideration for using the device.

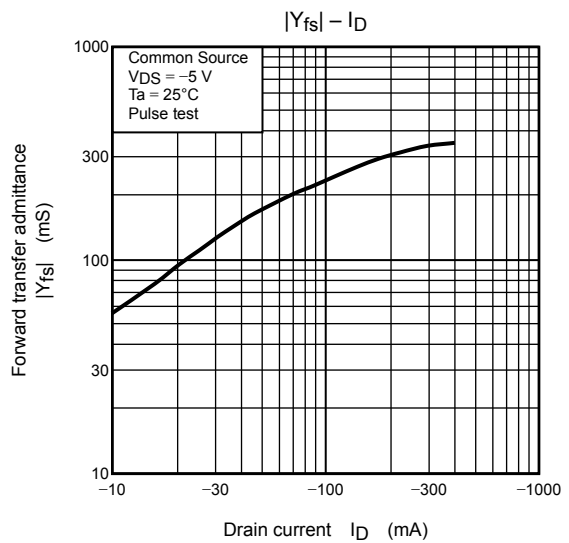
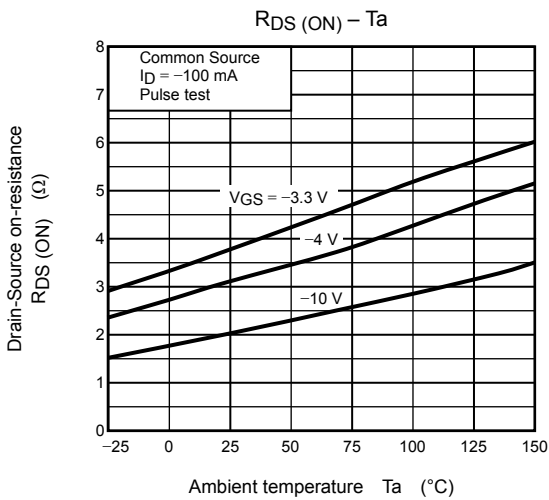
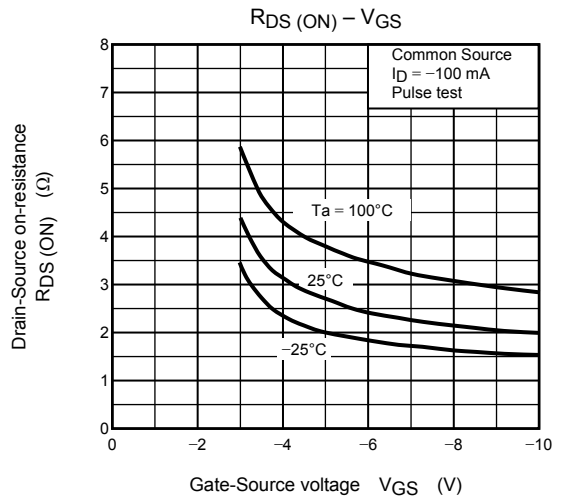
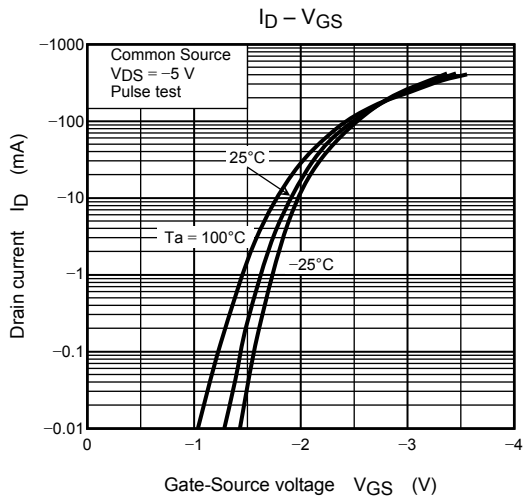
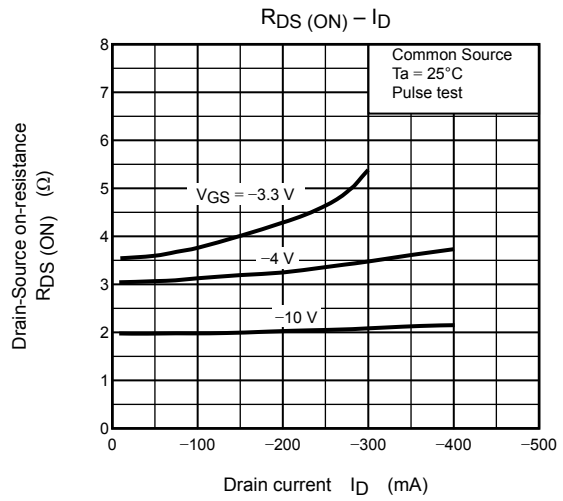
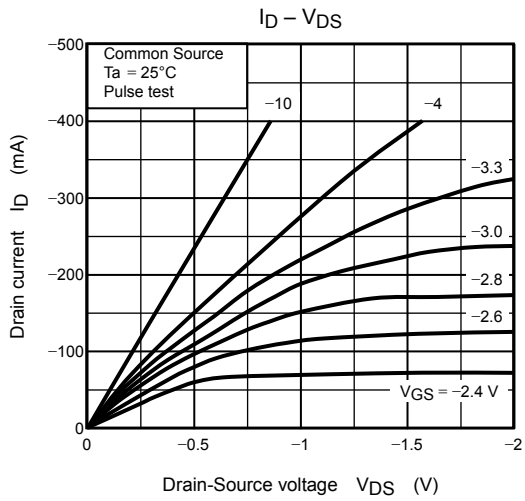
Q1 (Nch MOS FET)



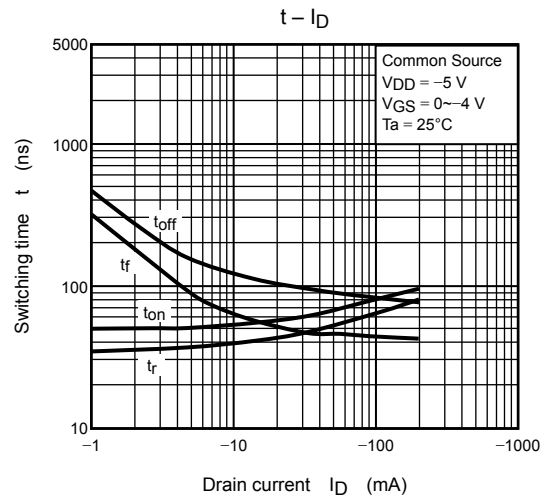
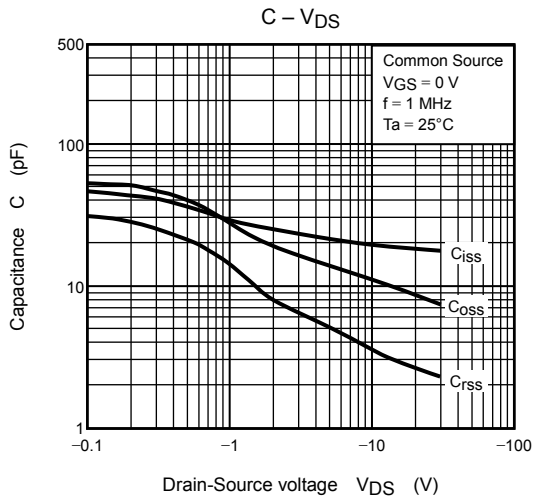
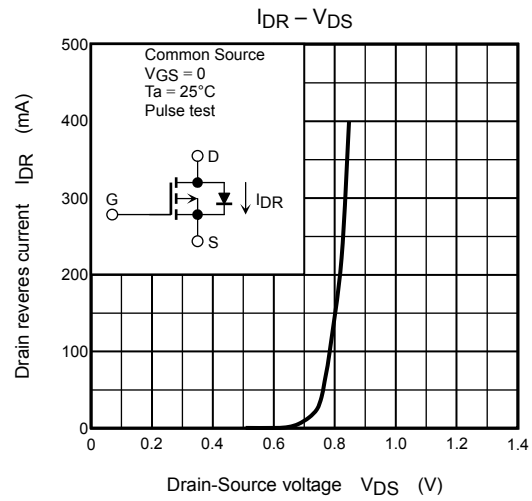
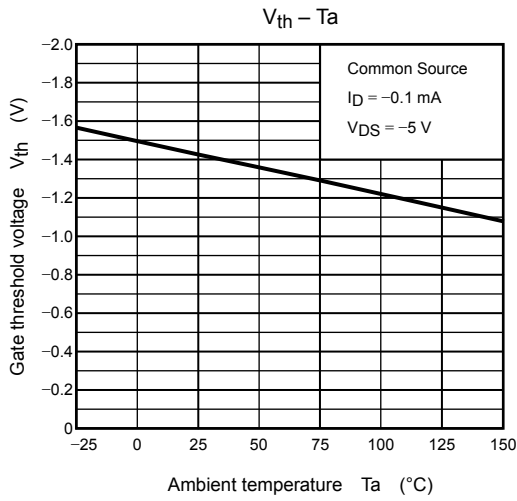
## Q1 (Nch MOS FET)



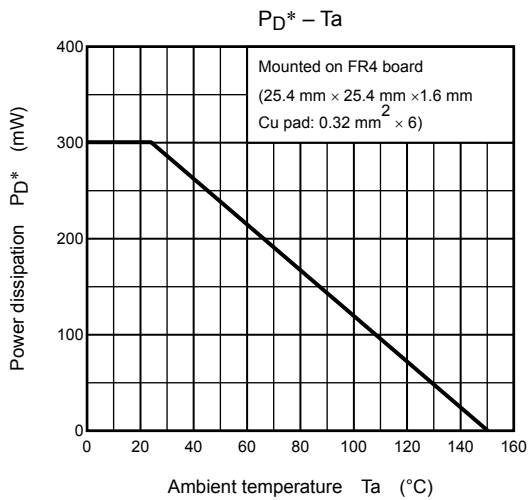
Q2 (Pch MOS FET)



## Q2 (Pch MOS FET)



## Common Characteristics



\*: Total rating



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