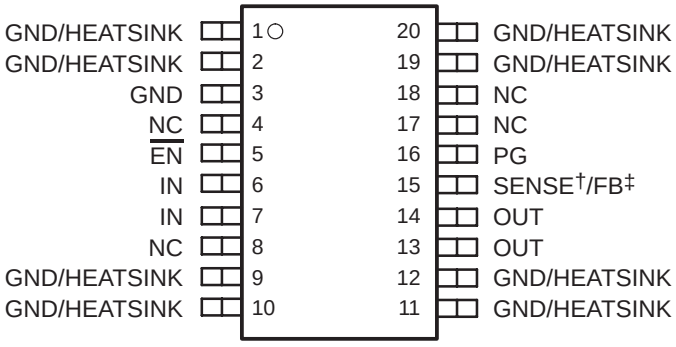
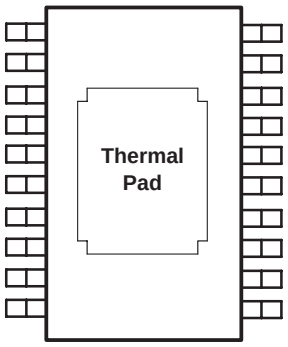
- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Very Low-Dropout Voltage . . . Maximum of 32 mV at I_O = 100 mA (TPS71H50)**
- **Very Low Quiescent Current − Independent of Load . . . 285 μA Typ**
- **Extremely Low Sleep-State Current 0.5 μA Max**
- **2% Tolerance Over Specified Conditions For Fixed-Output Versions**
- **Output Current Range of 0 mA to 500 mA**
- **TSSOP Package Option Offers Reduced Component Height for Space-Critical Applications**
- **Thermally Enhanced Surface-Mount Package**
- **Power-Good (PG) Status Output**

PWP PACKAGE
(TOP VIEW)



PWP PACKAGE
(BOTTOM VIEW)



NC − No internal connection
† SENSE − Fixed voltage options only (TPS71H33, TPS71H48, and TPS71H50)
‡ FB − Adjustable version only (TPS71H01)

description

The TPS71Hxx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS71H50) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ ($\overline{enable}$) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at T_J = 25°C.

description (continued)

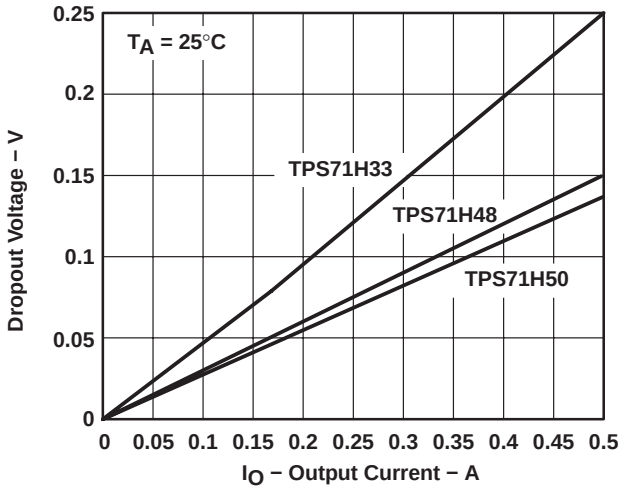


Figure 1. Dropout Voltage Versus Output Current

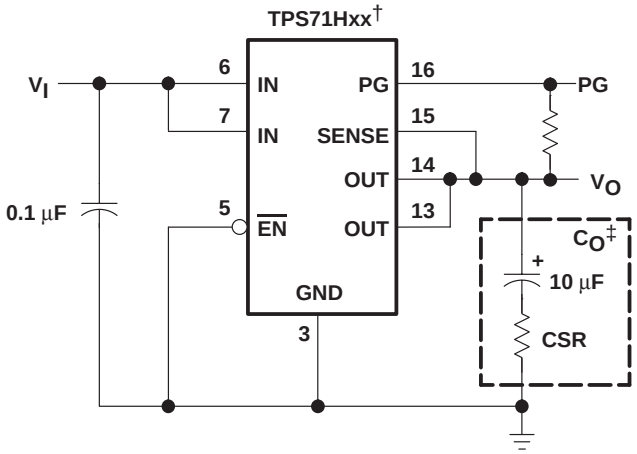
Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

The TPS71Hxx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71Hxx family is available in a TSSOP (20-pin) thermally enhanced surface-mount power package. The package has an innovative thermal pad that, when soldered to the printed-wiring board (PWB), enables the device to dissipate several watts of power (see Thermal Information section). Maximum height of the package is 1.2 mm.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			TSSOP (PWP)
	MIN	TYP	MAX	
−55°C to 150°C	4.9	5	5.1	TPS71H50QPWPLE
	4.75	4.85	4.95	TPS71H48QPWPLE
	3.23	3.3	3.37	TPS71H33QPWPLE
	Adjustable† 1.2 V to 9.75 V			TPS71H01QPWPLE

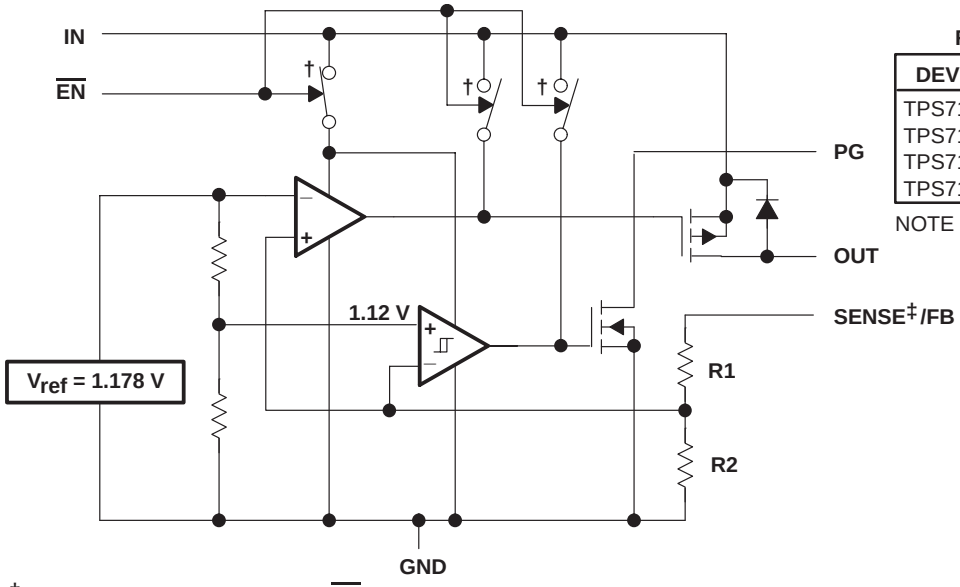
† The PWP package is only available left-end taped and reeled, as indicated by the LE suffix on the device type. The TPS71H01Q is programmable using an external resistor divider (see application information).



† TPS71H33, TPS71H48, TPS71H50 (fixed-voltage options)
‡ Capacitor selection is nontrivial. See application information section for details.

Figure 2. Typical Application Configuration

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS71H01	0	∞	Ω
TPS71H33	420	233	kΩ
TPS71H48	726	233	kΩ
TPS71H50	756	233	kΩ

NOTE A: Resistors are nominal values only.

COMPONENT COUNT	
MOS transistors	464
Bilpolar transistors	41
Diodes	4
Capacitors	17
Resistors	76

† Switch positions are shown with $\overline{EN}$ low (active).
‡ For most applications, SENSE should be externally connected to OUT as close as possible to the device. (For other implementations, refer to SENSE-pin connection discussion in Applications Information section.)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I, PG, SENSE, $\overline{EN}$ . . . . . −0.3 V to 11 V
Output current, I_O . . . . . 2 A
Continuous total power dissipation . . . . . See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J . . . . . −55°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 − FREE-AIR TEMPERATURE (see Figure 3)§

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PWP¶	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 − CASE TEMPERATURE (see Figure 4)§

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
PWP¶	25 W	285.7 mW/°C	22.9 W	7.1 W

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.
¶ Refer to Thermal Information section for detailed power dissipation considerations when using the TSSOP packages.

DISSIPATION DERATING CURVE†
vs
FREE-AIR TEMPERATURE

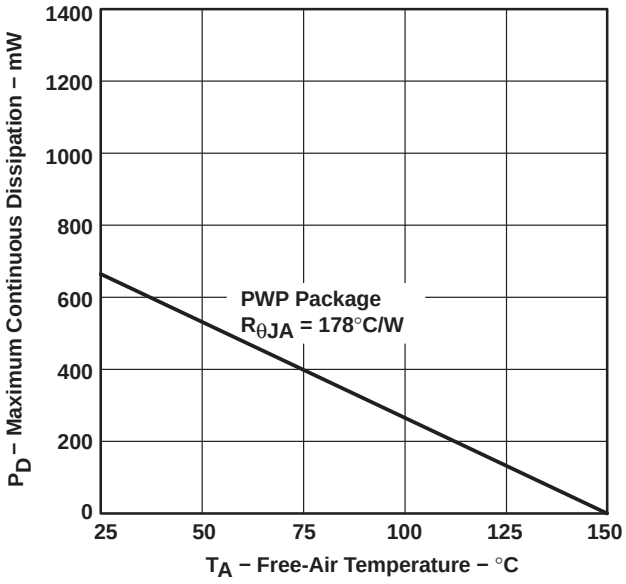


Figure 3

MAXIMUM CONTINUOUS DISSIPATION†
vs
CASE TEMPERATURE

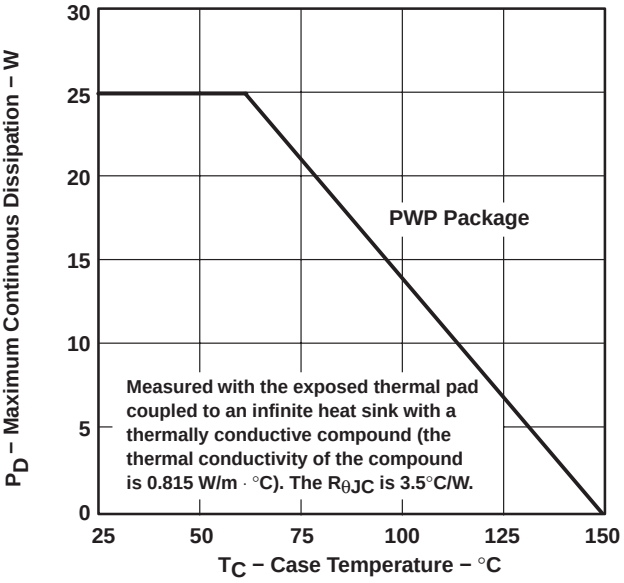


Figure 4

† Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS71H01Q	2.5	10	V
	TPS71H33Q	3.77	10	
	TPS71H48Q	5.2	10	
	TPS71H50Q	5.33	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$ Because the TPS71H01 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS71H01.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR‡ = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	T_J	TPS71H01Q, TPS71H33Q TPS71H48Q, TPS71H50Q			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O$ + 1 V, 0 mA ≤ I_O ≤ 500 mA	25°C		285	350	μA
		−40°C to 125°C			460	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			2	
Output current limit	V_O = 0, V_I = 10 V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	μA
		−40°C to 125°C			1	
PG leakage current	Normal operation, V_{PG} = 10 V	25°C		0.02	0.5	μA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5		0.5	μA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 μA I_{PG} = 300 μA	25°C		1.06	1.5	V
		−40°C to 125°C			1.9	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS71H01 electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS71H01Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.178		V
	2.5 V ≤ V_I ≤ 10 V, See Note 1	5 mA ≤ I_O ≤ 500 mA,	−40°C to 125°C	1.143		1.213	V
Reference voltage temperature coefficient			−40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V,	50 μA ≤ I_O ≤ 150 mA	25°C		0.7	1	Ω
			−40°C to 125°C			1	
	V_I = 2.4 V,	150 mA ≤ I_O ≤ 500 mA	25°C		0.83	1.3	
			−40°C to 125°C			1.3	
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 500 mA	25°C		0.52	0.85	
			−40°C to 125°C			0.85	
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 500 mA	25°C		0.32		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 500 mA	25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, See Note 1	50 μA ≤ I_O ≤ 500 mA,	25°C			18	mV
			−40°C to 125°C			25	
Output regulation	I_O = 5 mA to 500 mA, See Note 1	2.5 V ≤ V_I ≤ 10 V,	25°C			14	mV
			−40°C to 125°C			25	
	I_O = 50 μA to 500 mA, See Note 1	2.5 V ≤ V_I ≤ 10 V,	25°C			22	mV
			−40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	48	59		dB
			−40°C to 125°C	44			
		I_O = 500 mA, See Note 1	25°C	45	54		
			−40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		95		μVrms
		C_O = 10 μF	25°C		89		
		C_O = 100 μF	25°C		74		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		−40°C to 125°C	1.101		1.145	V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 μA,	V_I = 2.13 V	25°C		0.1	0.4	V
			−40°C to 125°C			0.4	
FB input current			25°C	−10	0.1	10	nA
			−40°C to 125°C	−20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 27) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. (For other programmed values, see Figure 26.)

TPS71H33 electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS71H33Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		4.5	7	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		47	60	
			−40°C to 125°C			80	
	I_O = 500 mA,	V_I = 3.23 V	25°C		235	300	
			−40°C to 125°C			400	
Pass-element series resistance	(3.23 V − V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,	25°C		0.47	0.6	Ω
			−40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			20	mV
			−40°C to 125°C			27	
Output regulation	I_O = 5 mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	38	mV
			−40°C to 125°C			75	
	I_O = 50 μA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		30	60	mV
			−40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	43	54		dB
			−40°C to 125°C	40			
		I_O = 500 mA	25°C	39	49		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		274		μVrms
		C_O = 10 μF	25°C		228		
		C_O = 100 μF	25°C		159		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	2.868		3	V
PG hysteresis voltage			25°C		35		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS71H48 electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS71H48Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	4.75		4.95	
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V	25°C		2.9	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.75 V	25°C		30	37	
			−40°C to 125°C			54	
	I_O = 500 mA,	V_I = 4.75 V	25°C		150	180	
			−40°C to 125°C			250	
Pass-element series resistance	(4.75 V − V_O)/I_O, I_O = 500 mA	V_I = 4.75 V,	25°C		0.32	0.35	Ω
			−40°C to 125°C			0.52	
Input regulation	V_I = 5.85 V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			27	mV
			−40°C to 125°C			37	
Output regulation	I_O = 5 mA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		12	42	mV
			−40°C to 125°C			80	
	I_O = 50 μA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		42	60	mV
			−40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	42	53		dB
			−40°C to 125°C	39			
		I_O = 500 mA	25°C	39	50		
			−40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		410		μVrms
		C_O = 10 μF	25°C		328		
		C_O = 100 μF	25°C		212		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	4.5		4.7	V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.12 V	25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS71H50 electrical characteristics at I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS71H50Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		2.9	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.88 V	25°C		27	32	
			−40°C to 125°C			47	
	I_O = 500 mA,	V_I = 4.88 V	25°C		146	170	
			−40°C to 125°C			230	
Pass-element series resistance	(4.88 V − V_O)/I_O, I_O = 500 mA	V_I = 4.88 V.	25°C		0.29	0.32	Ω
			−40°C to 125°C			0.47	
Input regulation	V_I = 6 V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			25	mV
			−40°C to 125°C			32	
Output regulation	I_O = 5 mA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		30	45	mV
			−40°C to 125°C			86	
	I_O = 50 μA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		45	65	mV
			−40°C to 125°C			140	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	45	55		dB
			−40°C to 125°C	40			
		I_O = 500 mA	25°C	42	52		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		430		μVrms
		C_O = 10 μF	25°C		345		
		C_O = 100 μF	25°C		220		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	4.55		4.75	V
PG hysteresis voltage			25°C		53		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	5
		vs Input voltage	6
		vs Free-air temperature	7
V_{DO}	Typical dropout voltage	vs Output current	8
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	9
ΔV_O	Change in output voltage	vs Free-air temperature	10
V_O	Output voltage	vs Input voltage	11
ΔV_O	Change in output voltage	vs Input voltage	12
V_O	Output voltage	vs Output current	13
			14
			15
			16
	Ripple rejection	vs Frequency	17
			18
			19
			20
	Output spectral noise density	vs Frequency	21
			22
			23
			24
$r_{DS(on)}$	Pass-element resistance	vs Input voltage	25
R	Divider resistance	vs Free-air temperature	26
$I_{I(SENSE)}$	SENSE current	vs Free-air temperature	27
	FB leakage current	vs Free-air temperature	28
V_I	Minimum input voltage for active-pass element	vs Free-air temperature	29
	Minimum input voltage for valid PG	vs Free-air temperature	30
$I_{I(EN)}$	Input current ($\overline{EN}$)	vs Free-air temperature	31
	Output voltage response from enable ($\overline{EN}$)		32
V_{PG}	Power-good (PG) voltage	vs Output voltage	33
CSR	Compensation series resistance	vs Output current	34
			35
CSR	Compensation series resistance	vs Ceramic capacitance	36
			37
CSR	Compensation series resistance	vs Output current	38
			39
CSR	Compensation series resistance	vs Ceramic capacitance	40
			41

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs OUTPUT CURRENT

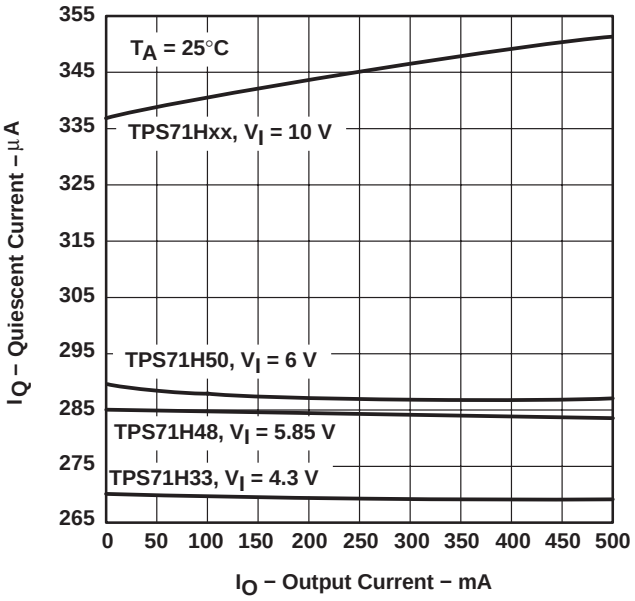


Figure 5

QUIESCENT CURRENT vs INPUT VOLTAGE

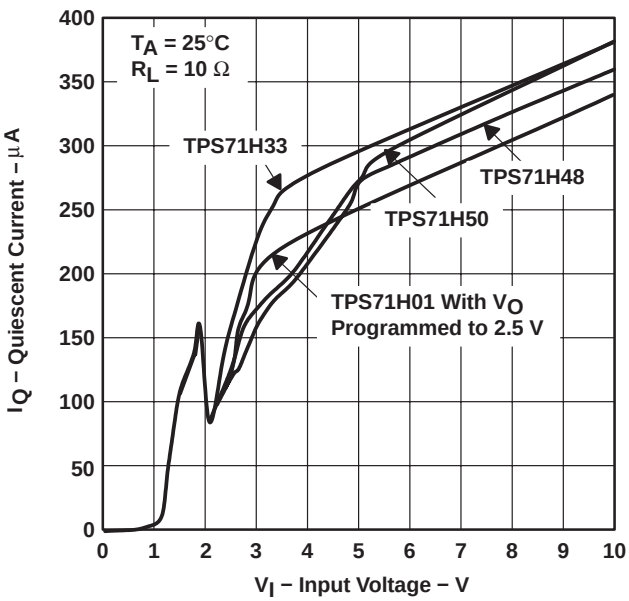


Figure 6

TPS71H48Q QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

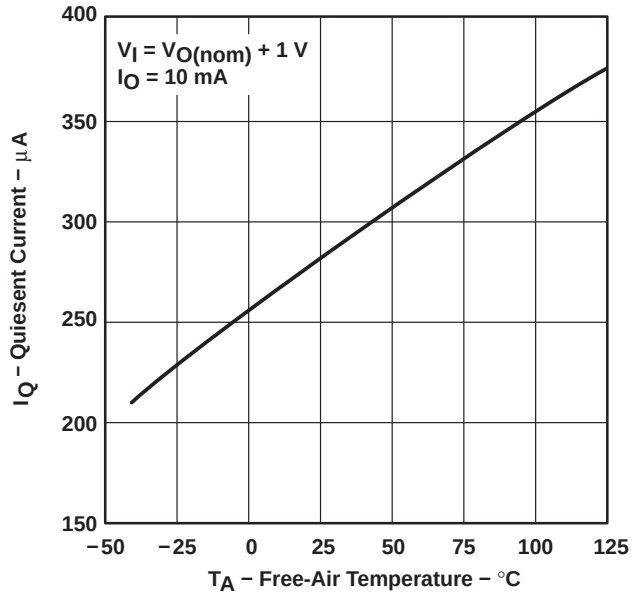


Figure 7

DROPOUT VOLTAGE vs OUTPUT CURRENT

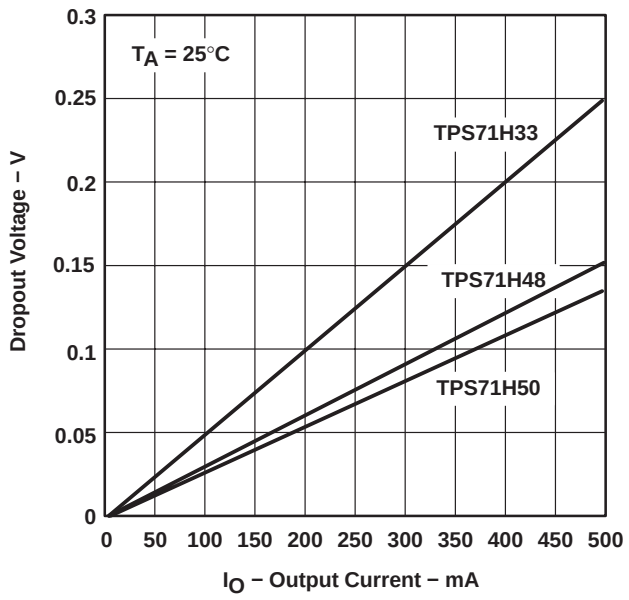


Figure 8

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

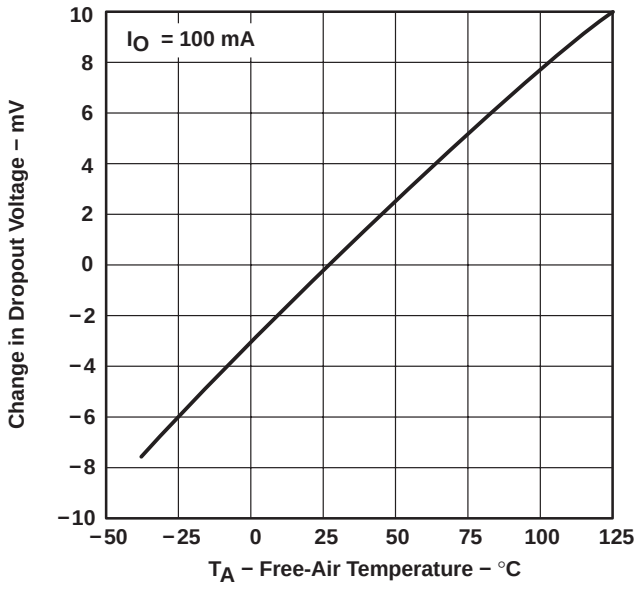


Figure 9

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

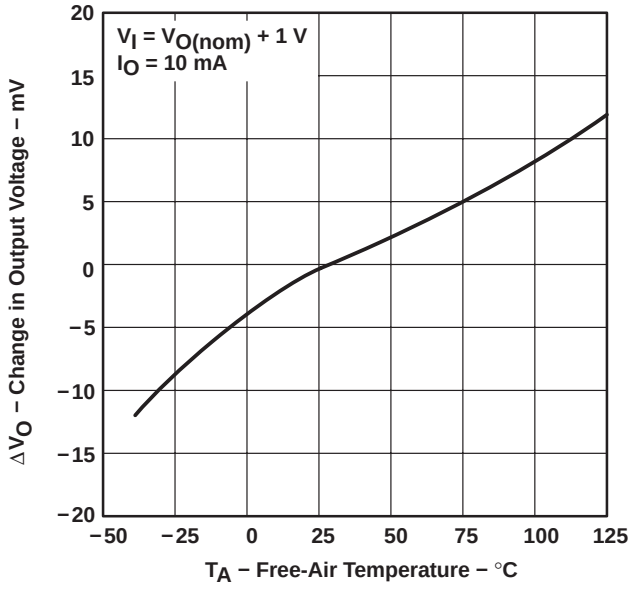


Figure 10

OUTPUT VOLTAGE vs INPUT VOLTAGE

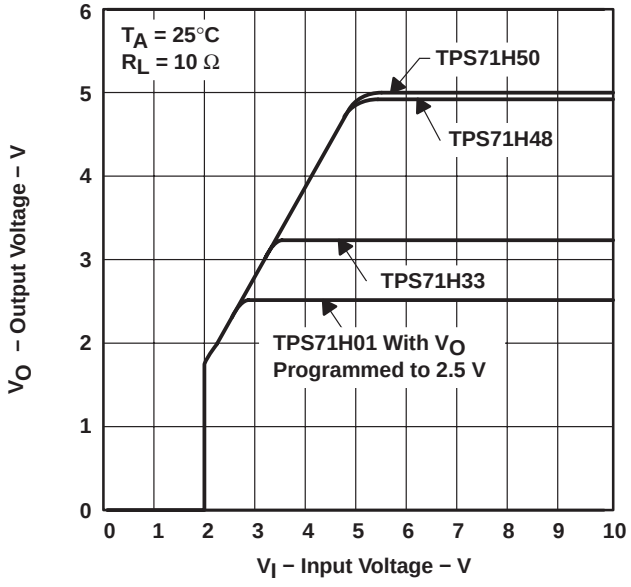


Figure 11

CHANGE IN OUTPUT VOLTAGE vs INPUT VOLTAGE

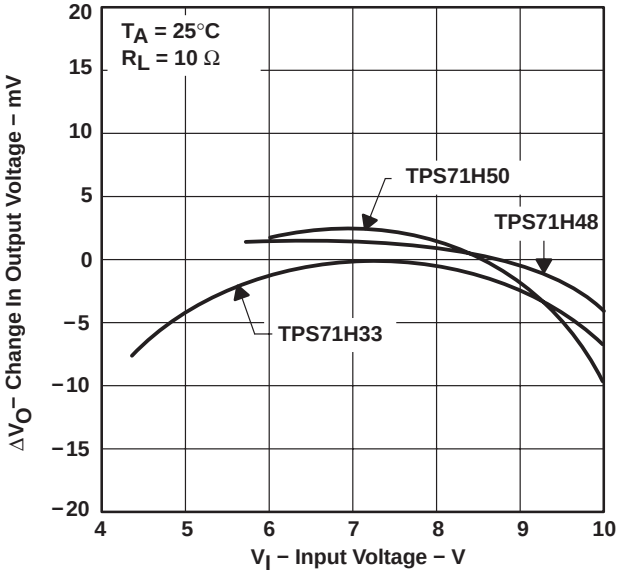


Figure 12

TYPICAL CHARACTERISTICS

TPS71H01Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

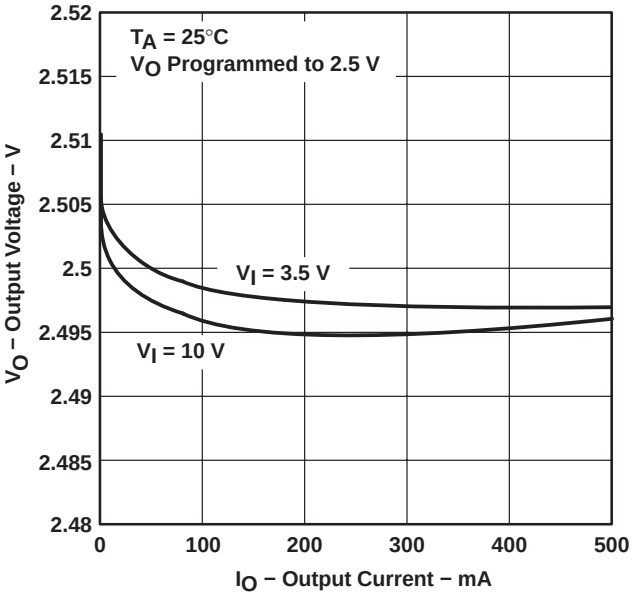


Figure 13

TPS71H33Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

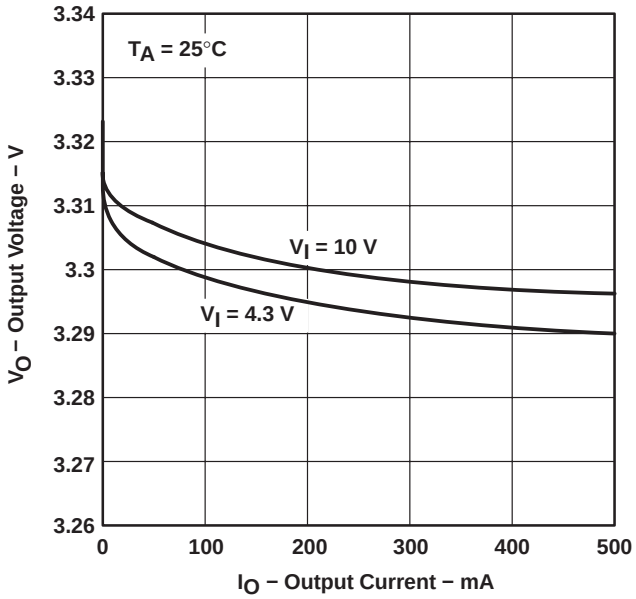


Figure 14

TPS71H48Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

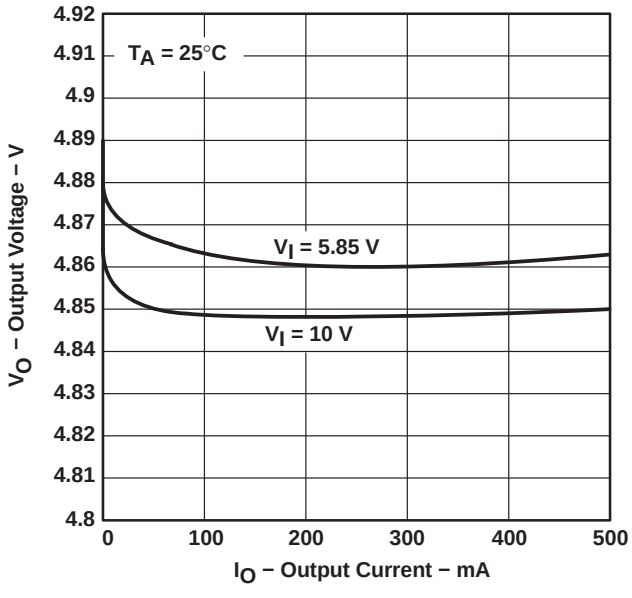


Figure 15

TPS71H50Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

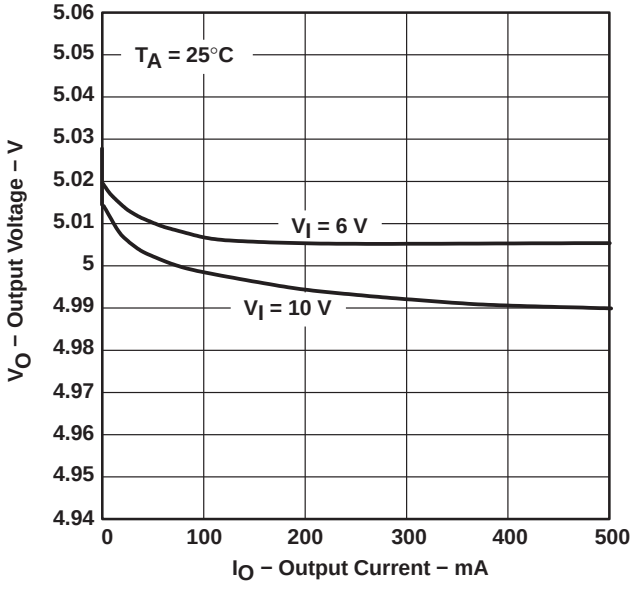


Figure 16

TYPICAL CHARACTERISTICS

TPS71H01Q
RIPPLE REJECTION
vs
FREQUENCY

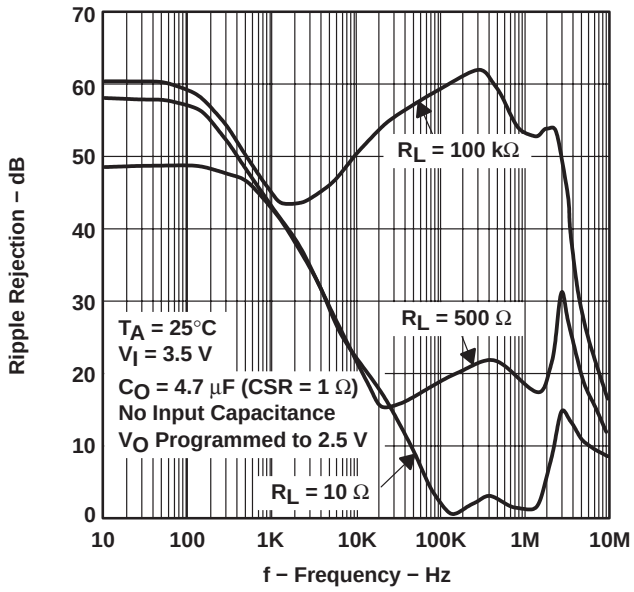


Figure 17

TPS71H33Q
RIPPLE REJECTION
vs
FREQUENCY

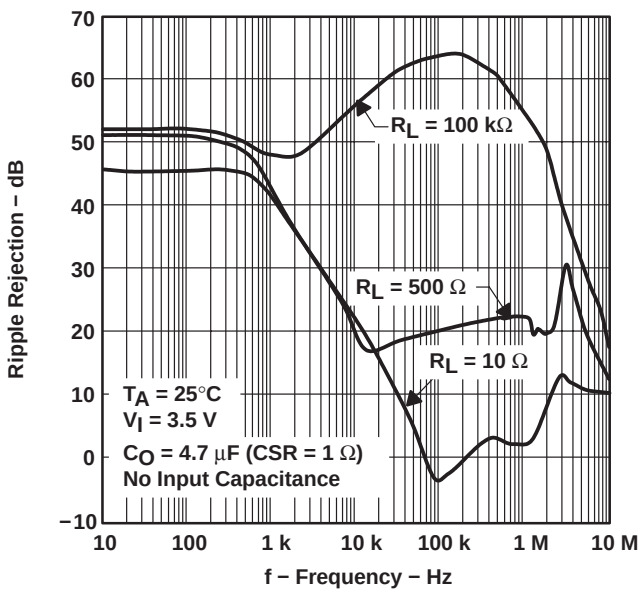


Figure 18

TPS71H48Q
RIPPLE REJECTION
vs
FREQUENCY

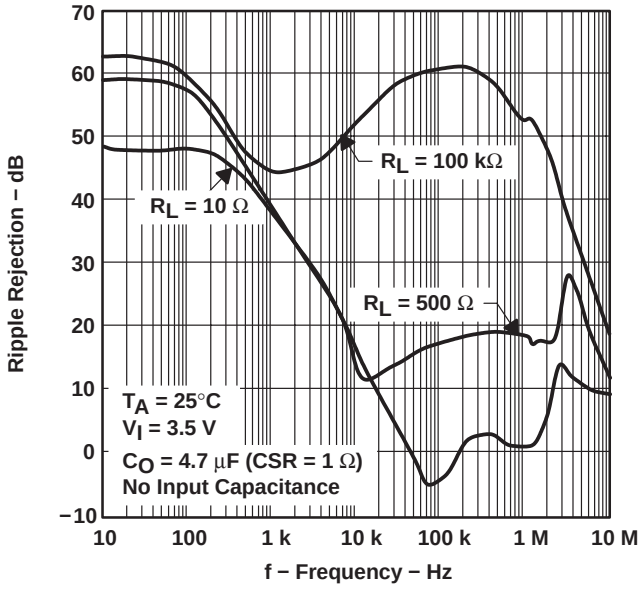


Figure 19

TPS71H50Q
RIPPLE REJECTION
vs
FREQUENCY

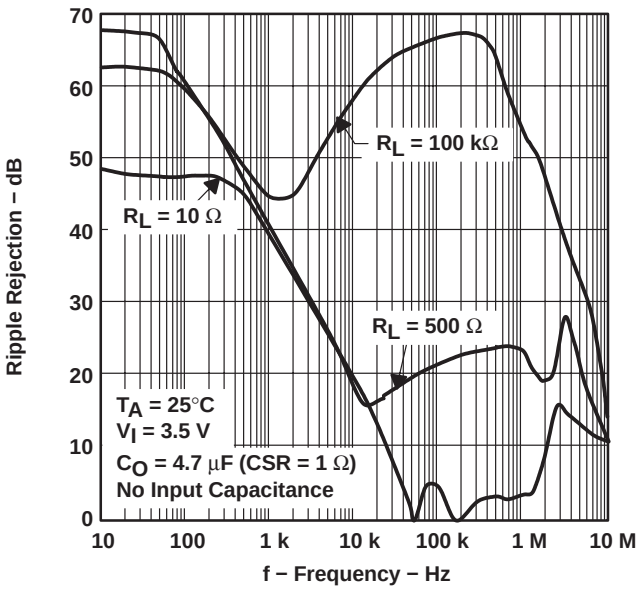


Figure 20

TYPICAL CHARACTERISTICS

TPS71H01Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

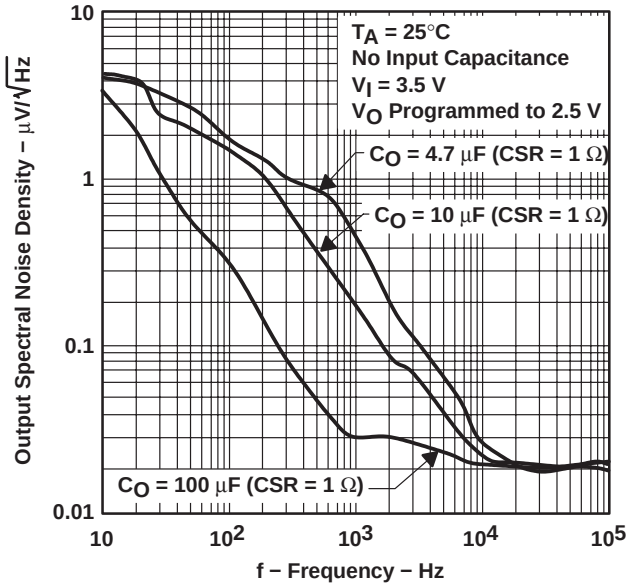


Figure 21

TPS71H33Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

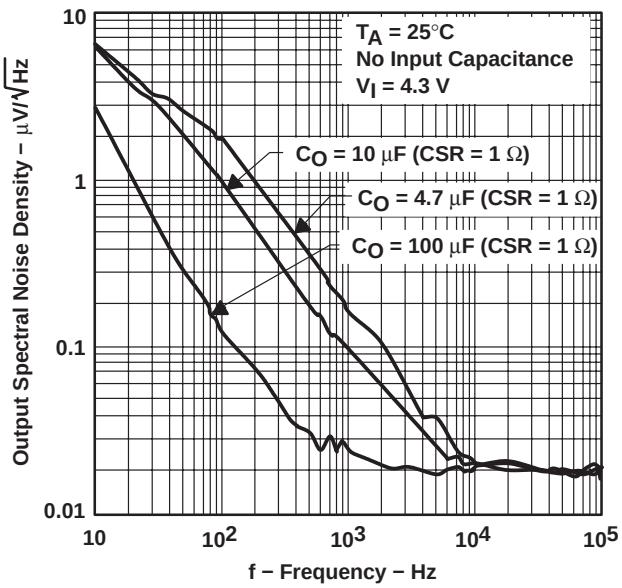


Figure 22

TPS71H48Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

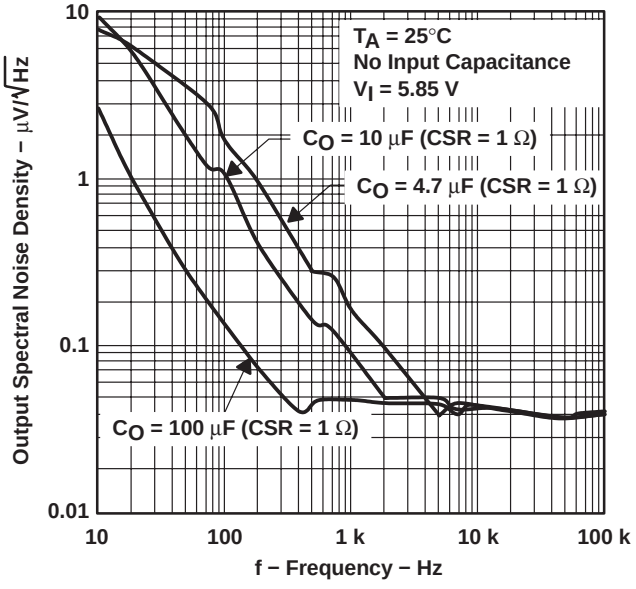


Figure 23

TPS71H50Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

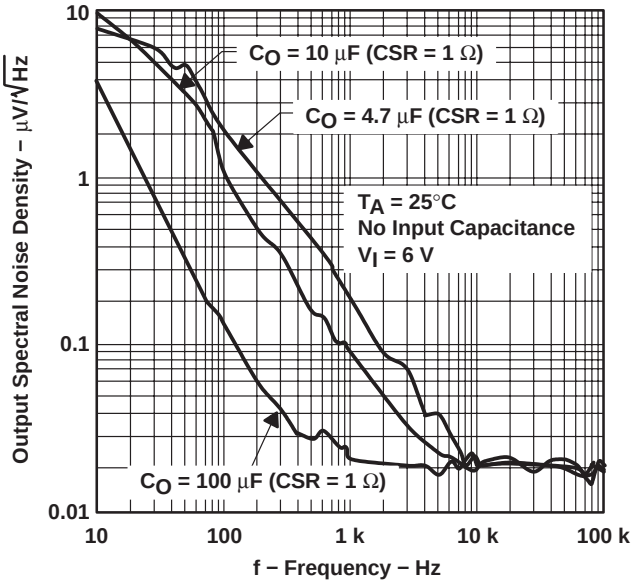


Figure 24

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

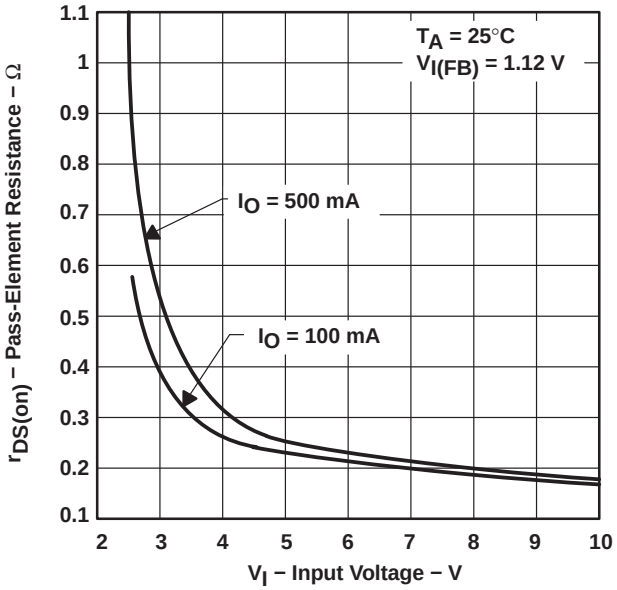


Figure 25

DIVIDER RESISTANCE vs FREE-AIR TEMPERATURE

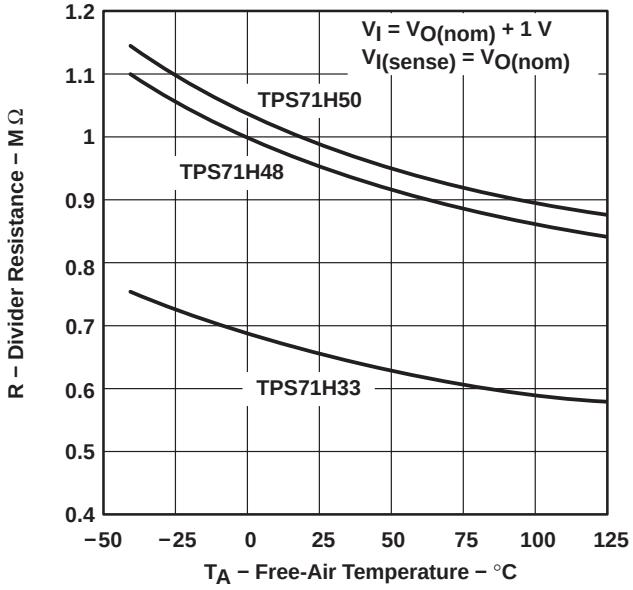


Figure 26

FIXED-OUTPUT VERSIONS SENSE PIN CURRENT vs FREE-AIR TEMPERATURE

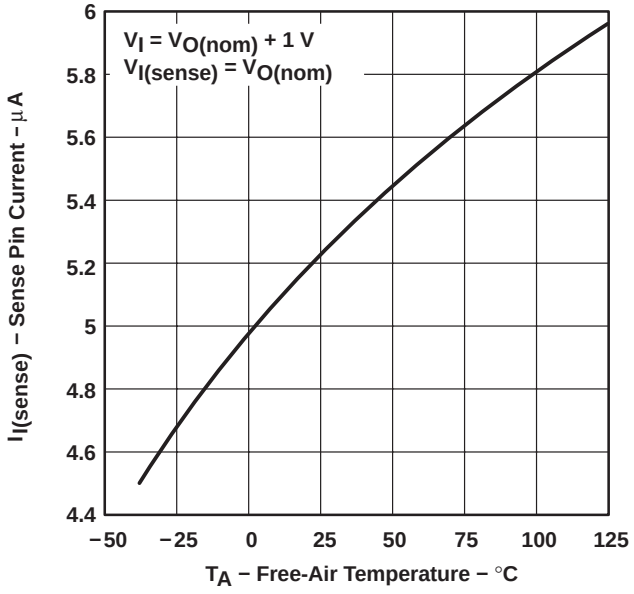


Figure 27

ADJUSTABLE VERSION FB LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

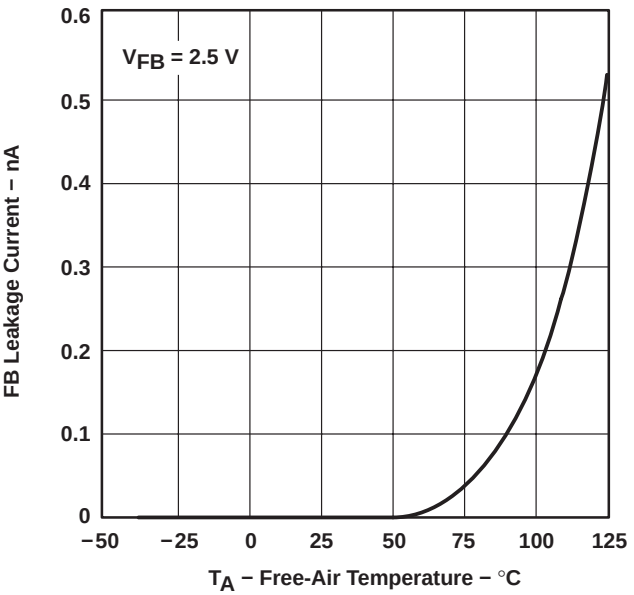


Figure 28

TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE PASS ELEMENT vs FREE-AIR TEMPERATURE

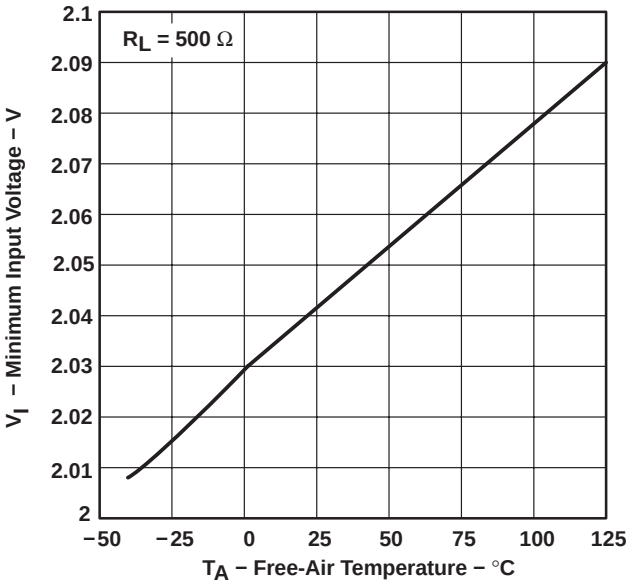


Figure 29

MINIMUM INPUT VOLTAGE FOR VALID POWER GOOD (PG) vs FREE-AIR TEMPERATURE

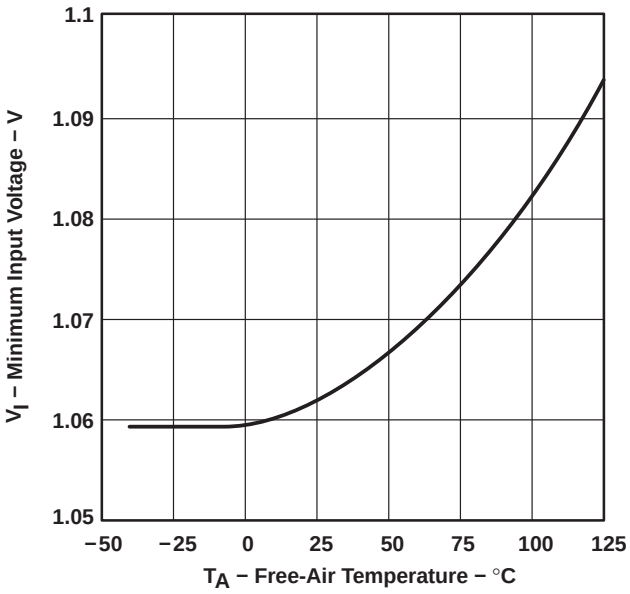


Figure 30

$\overline{EN}$ INPUT CURRENT vs FREE-AIR TEMPERATURE

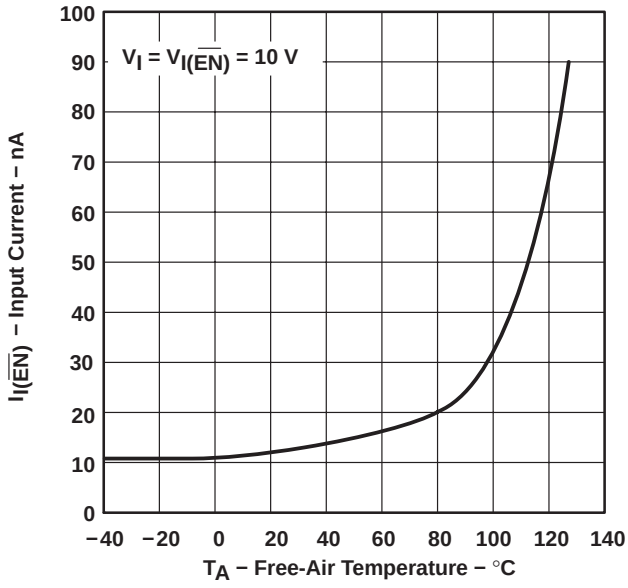


Figure 31

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE ($\overline{EN}$)

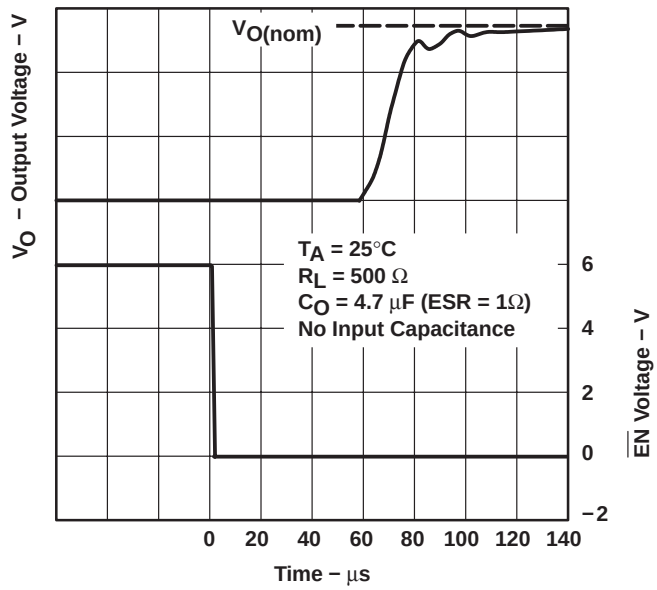


Figure 32

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE

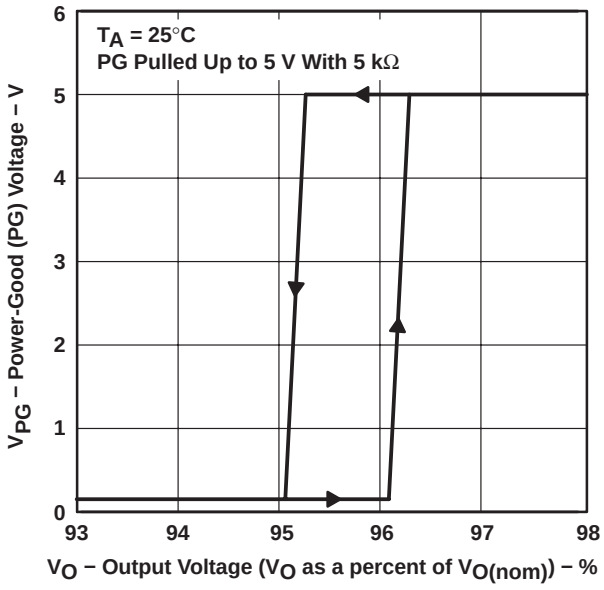


Figure 33

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

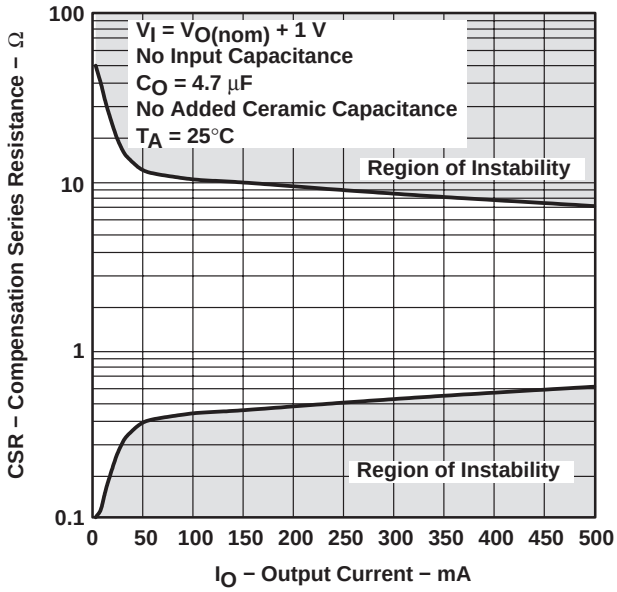


Figure 34

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

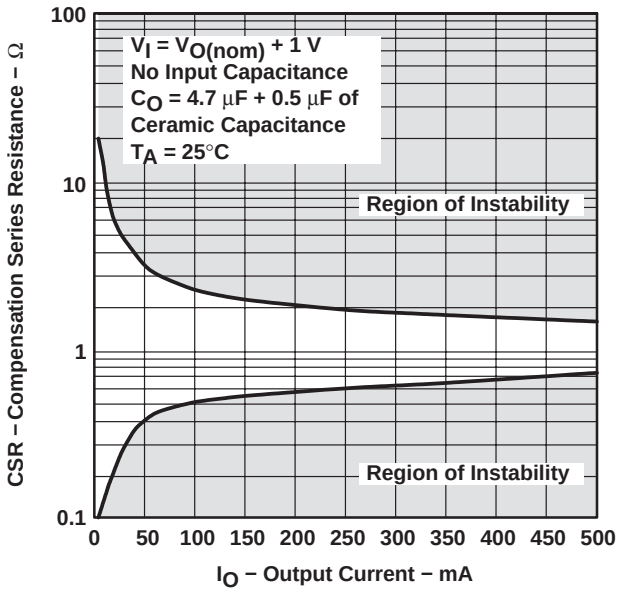


Figure 35

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

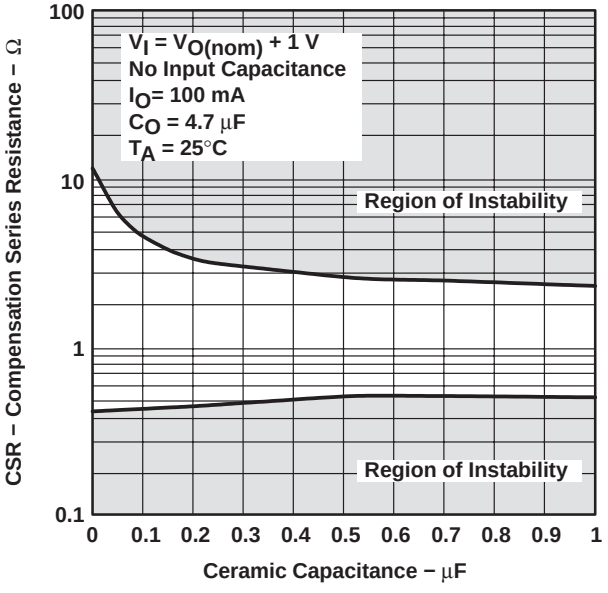


Figure 36

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

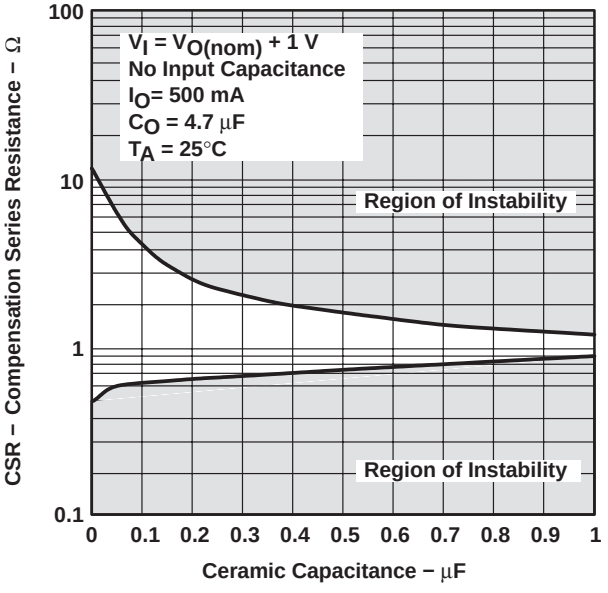


Figure 37

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

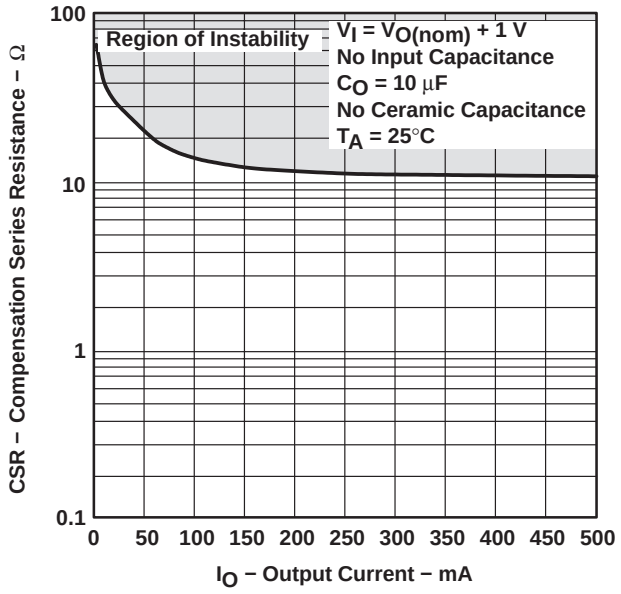


Figure 38

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

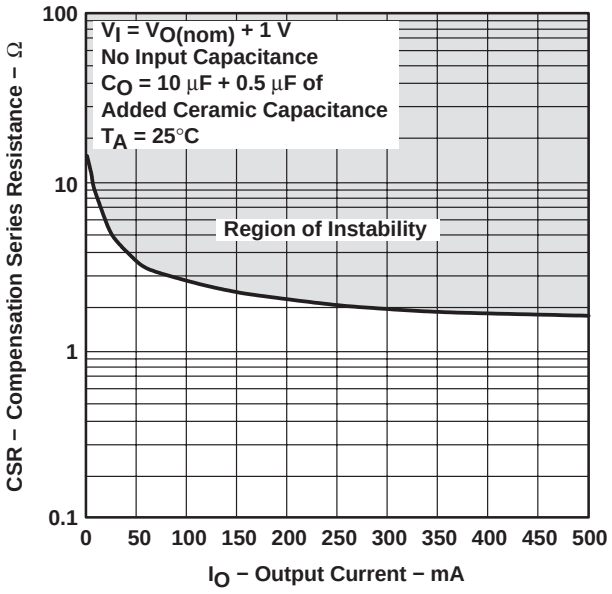


Figure 39

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

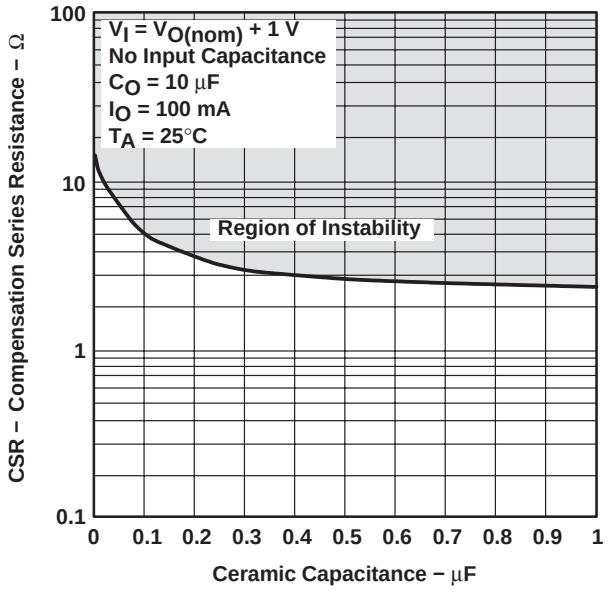


Figure 40

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

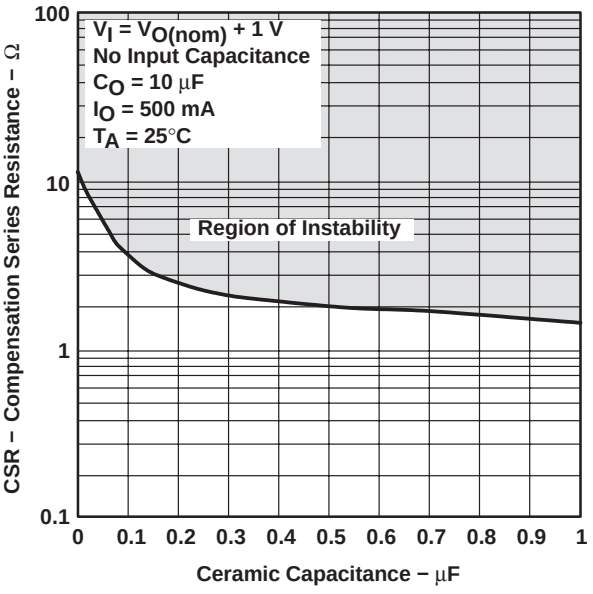
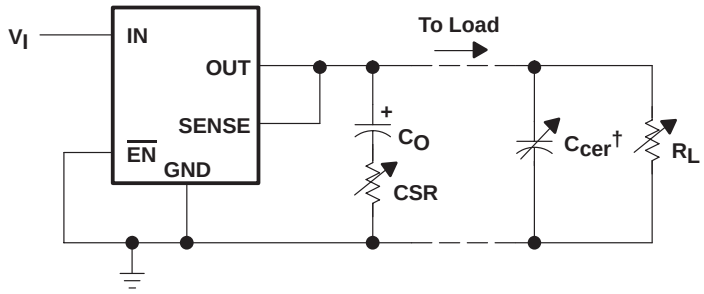


Figure 41

† CSR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS



† Ceramic capacitor

Figure 42. Test Circuit for Typical Regions of Stability (see Figures 34 through 41)

THERMAL INFORMATION

standard TSSOP-20

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 43 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 44. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board ($L \times W \times H = 3.2$ inch $\times$ 3.2 inch $\times$ 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

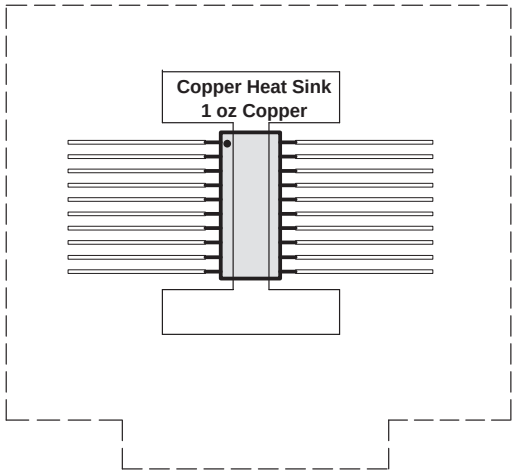


Figure 43. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

Figure 45 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m $\times$ °C.

THERMAL INFORMATION

standard TSSOP-20 (continued)

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT vs AIR FLOW

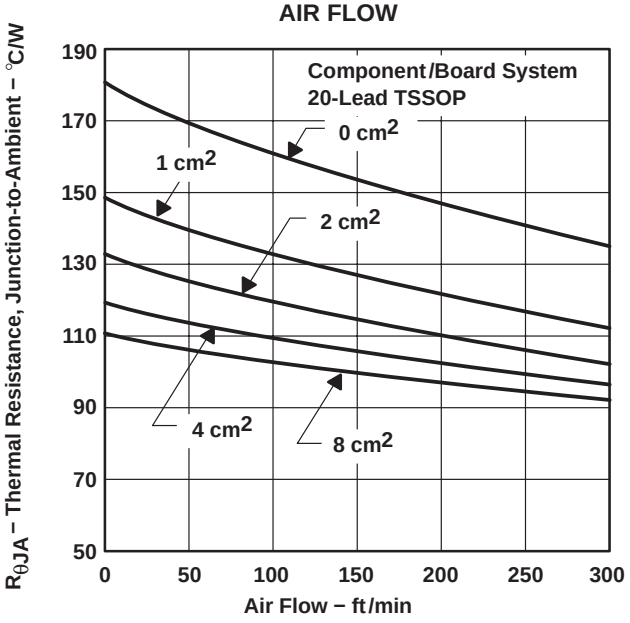


Figure 44

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT vs AIR FLOW

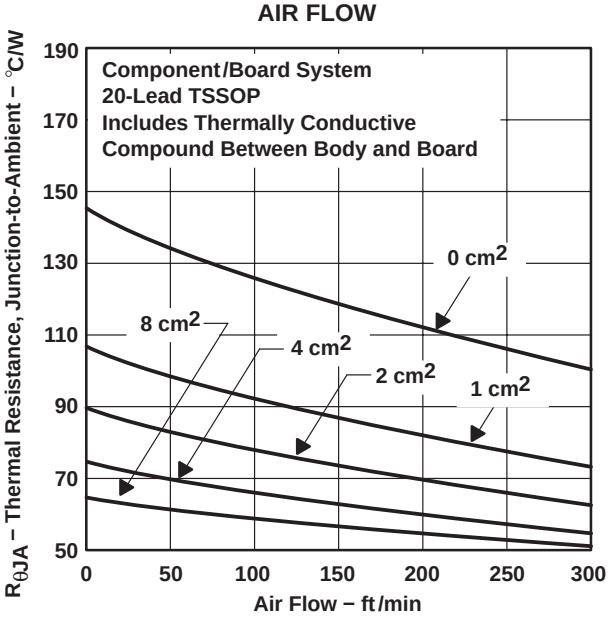


Figure 45

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature (i.e., 150°C absolute maximum and 125°C maximum recommended operating temperature for specified operation).

This limit should then be applied to the internal power dissipated by the TPS71Hxx regulator. The equation for calculating total internal power dissipation of the TPS71Hxx is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS71Hxx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O$$

THERMAL INFORMATION

standard TSSOP-20 (continued)

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where T_A = 55°C, airflow = 100 ft/min, copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 45, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{94°C/W} = 745 \text{ mW}$$

If the system implements a TPS71H48 regulator where V_I = 6 V and I_O = 385 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

thermally enhanced TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 46(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

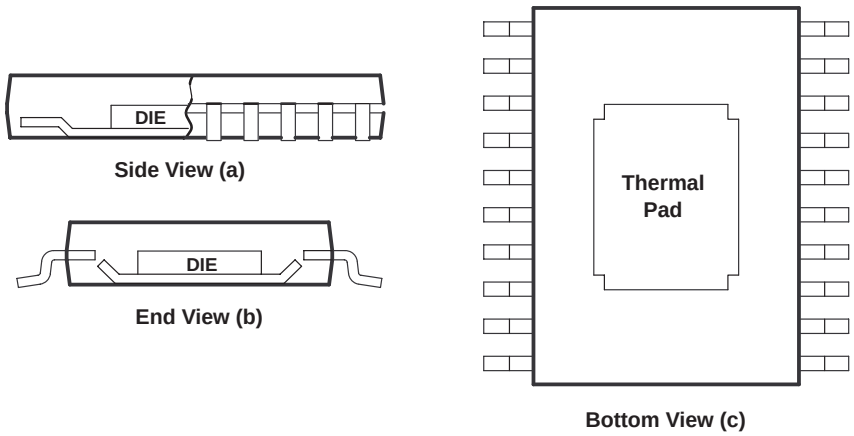


Figure 46. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 48(a), 8 cm^2 of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 47 and 48). The line drawn at 0.3 cm^2 in Figures 47 and 48 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 50.

The thermal pad is directly connected to the substrate of the IC, which for the TPS71HxxQPWP series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWB can be a ground plane or left electrically isolated. In other TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 12 independent leads that can be used as inputs and outputs (Note: leads 1, 2, 9, 10, 11, 12, 19, and 20 are internally connected to the thermal pad and the IC substrate).

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

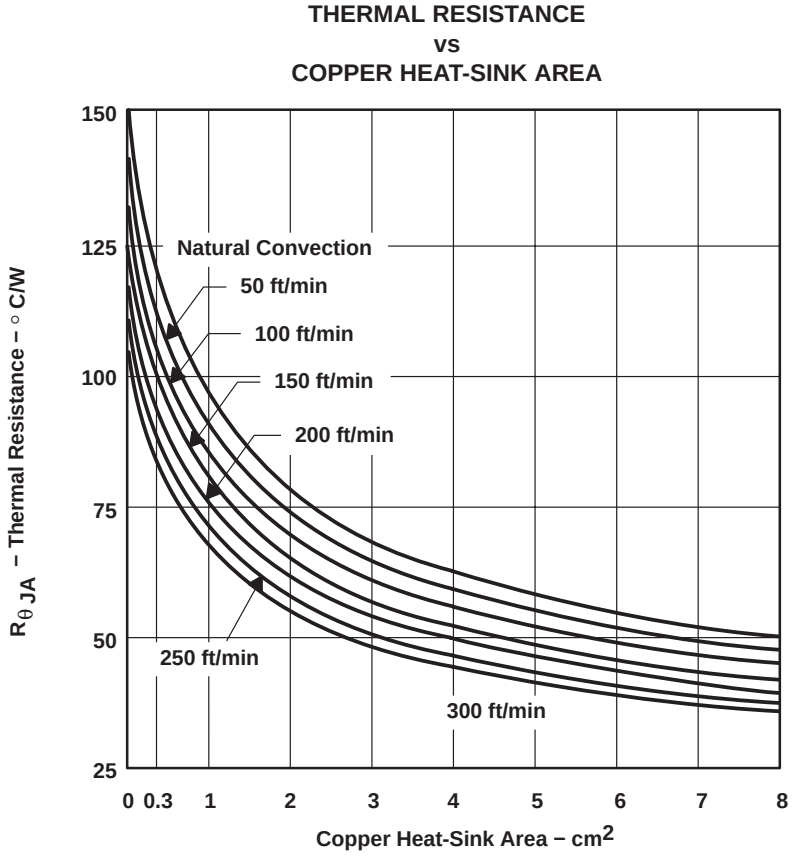


Figure 47

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

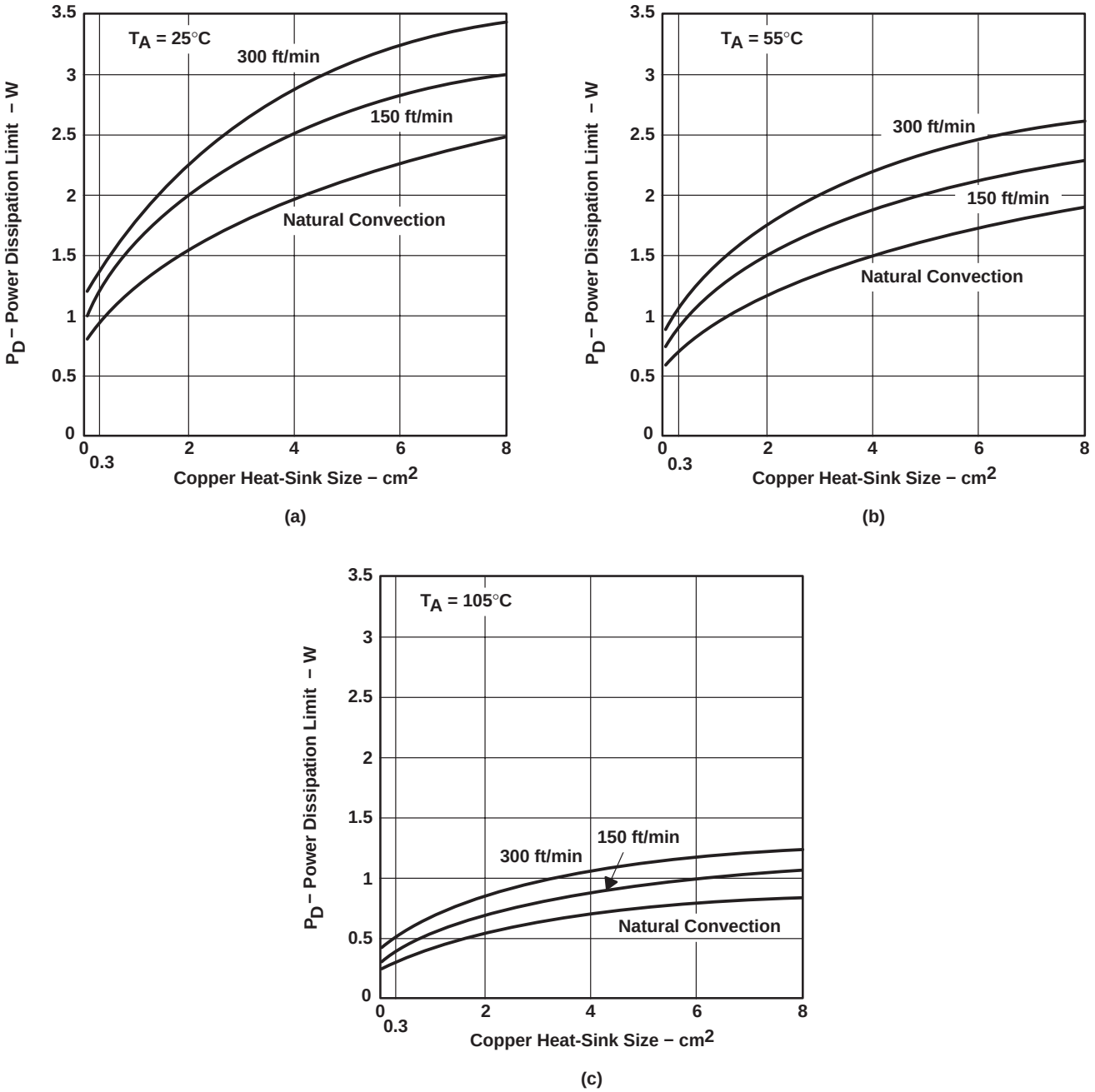
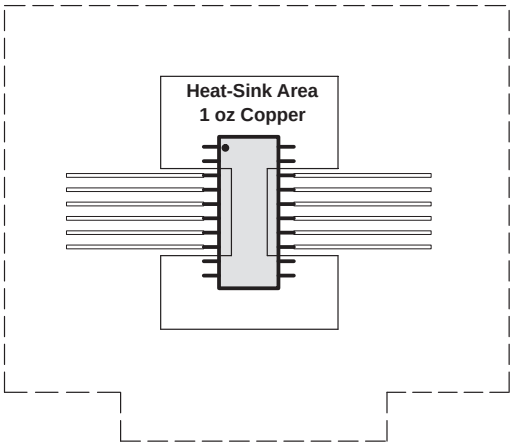


Figure 48. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

Figure 49 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figures 47 and 48. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 47 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.



Board thickness	62 mils
Board size	3.2 in. × 3.2 in.
Board material	FR4
Copper trace/heat sink	1 oz
Exposed pad mounting	63/67 tin/lead solder

Figure 49. PWB Layout (Including Copper Heatsink Area) for Thermally Enhanced PWP Package

From Figure 47, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}}$$

Where

$T_J$max is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS71H33QPWP regulator. The equation for calculating total internal power dissipation of the TPS71H33QPWP is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O + V_I \times I_Q$$

Since the quiescent current of the TPS71H33QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O$$

For the case where T_A = 55°C, airflow = 200 ft/min, copper heat-sink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 47, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{50°C/W} = 1.4\ W$$

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

If the system implements a TPS71H33QPWP regulator, where V_I = 6 V and I_O = 500 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O = (6 - 3.3) \times 0.5 = 1.35\ W$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

mounting information

Since the thermal pad is not a primary connection for an electrical signal, the importance of the electrical connection is not significant. The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figures 47 and 48 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 50 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 2, 9, 10, 11, 12, 19, and 20.

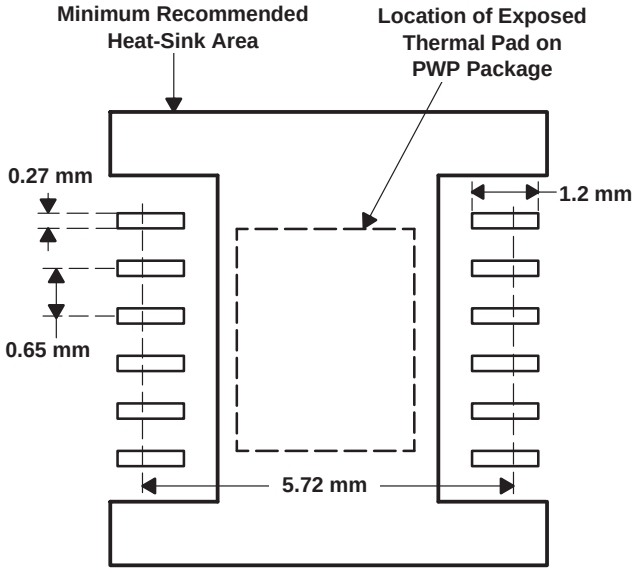


Figure 50. PWP Package Land Pattern

reliability information

This section includes demonstrated reliability test results obtained from the qualification program. Accelerated tests are performed at high-stress conditions so that product reliability can be established during a relatively short test duration. Specific stress conditions are chosen to represent accelerated versions of various device-application environments and allow meaningful extrapolation to normal operating conditions.

component level reliability test results

preconditioning

Preconditioning of components prior to reliability testing is employed to simulate the actual board assembly process used by the customer. This ensures that reliability test results are more representative of those that would be seen in the final application. The general form of the preconditioning sequence includes a moisture soak followed by multiple vapor-phase-reflow or infrared-reflow solder exposures. All components used in the following reliability tests were preconditioned in accordance with JEDEC Test Method A113 for Level 1 (not moisture-sensitive) products.

THERMAL INFORMATION

high-temperature life test

High-temperature life testing is used to demonstrate long-term reliability of the product under bias. The potential failure mechanisms evaluated with this stress are those associated with dielectric integrity and design or process sensitivity to mobile-ion phenomena. Components are tested at an elevated ambient temperature of 155°C for an extended period. Results are derated using the Arrhenius equation to an equivalent number of unit hours at a representative application temperature. The corresponding predicted failure rate is expressed in FITs, or failures per billion device-hours. The failure rate shown in this case is data-limited since no actual failures were experienced during qualification testing.

PREDICTED LONG-TERM FAILURE RATE

Number of Units	Equivalent Unit Hours at 55°C and 0.7 eV	FITs at 50% CL
325	24,468,090	36.2

biased humidity test

Biased humidity testing is used to evaluate the effects of moisture penetration on plastic-encapsulated devices under bias. This stress verifies the integrity of the package construction and the die passivation system. The primary potential failure mechanism is electrolytic corrosion. Components are biased in a low power state to reduce heat dissipation and are subjected to a 120°C, 85%-relative-humidity environment for 100 hours.

BIASED HUMIDITY TEST RESULTS

Equivalent Unit Hours at 85°C and 85% RH	Failures
357,000	0

autoclave test

The autoclave stress is used to assess the capabilities of the die and package construction materials with respect to moisture ingress and extended exposure. Predominant failure mechanisms include leakage currents that result from internal moisture accumulation and galvanic corrosion resulting from reactions with any present ionic contaminants. Components are subjected to a 121°C, 15 PSIG, 100%-relative-humidity environment for 240 hours.

AUTOCLAVE TEST RESULTS

Total Unit Hours	Failures
54,720	0

thermal shock test

Thermal shock testing is used to evaluate the capability of the component to withstand mechanical stress resulting from differences in thermal coefficients of expansion among the die and package construction materials. Failure mechanisms are typically related to physical damage at interface locations between different materials. Components are cycled between −65°C and 150°C in liquid mediums for a total duration of 1000 cycles.

THERMAL SHOCK TEST RESULTS

Total Unit Cycles	Failures
345,000	0

THERMAL INFORMATION

PWB assembly level reliability results

temperature cycle test

Temperature cycle testing of the PWB assembly is used to evaluate the capability of the assembly to withstand mechanical stress resulting from the differences in thermal coefficients of expansion among die, package, and PWB board materials. This testing is also used to sufficiently age the soldered thermal connection between the thermal pad and the Cu trace on the FR4 board and evaluate the degradation of the thermal resistance for a board-mounted test unit. The assemblies were cycled between temperature extremes of −40°C and 125°C for a total duration of 730 cycles.

TEMPERATURE CYCLE TEST RESULTS

Total Unit Cycles	Failures	Average Change in $R_{\theta JA(system)}$
36,500	0	−0.41%

solderability test

Solderability testing is used to simulate actual board-mount performance in a reflow process.

Solderability testing is conducted as follows: The test devices are first steam-aged for 8 hours. A stencil is used to apply a solder-paste terminal pattern on a ceramic substrate (nominal stencil thickness is 0.005 inch). The test units are manually placed on the solder-paste footprint with proper implements to avoid contamination. The ceramic substrate and components are subjected to the IR reflow process as follows:

IR REFLOW PROCESS

	PREHEAT SOAK	REFLOW
Temperature	150°C to 170°C	215°C to 230°C
Time	60 sec	60 sec

After cooling to room temperature, the component is removed from the ceramic substrate and the component terminals are subjected to visual inspection at 10X magnification.

Test results are acceptable if all terminations exhibit a continuous solder coating free of defects for a minimum 95% of the critical surface area of any individual termination. Causes for rejection include: dewetting, nonwetting, and pin holes. The component leads and the exposed thermal pad were evaluated against this criteria.

SOLDERABILITY TEST RESULTS

Number of Test Units	Failures
22	0

X-ray test

X-ray testing is used to examine and quantify the voiding of the soldered attachment between the thermal pad and the PWB copper trace. Voiding between 20% and 50% was observed on a 49-piece sample.

APPLICATION INFORMATION

The TPS71Hxx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71Hxx family includes three fixed-output voltage regulators: the TPS71H33 (3.3 V), the TPS71H48 (4.85 V), and the TPS71H50 (5 V). The family also offers an adjustable device, the TPS71H01 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71Hxx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71Hxx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71Hxx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71Hxx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71Hxx family is a 4.85-V regulator, the TPS71H48. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within $\pm$ 2%, allows for operation within the low-end limit of 5-V systems specified to $\pm$ 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71Hxx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS71Hxx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

APPLICATION INFORMATION

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection if the TPS71Hxx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS71Hxx family requires an output capacitor for stability. A low-ESR 10-μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 51). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-μF devices can be screened for ESR. Figures 34 through 41 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μF), the output capacitance can be reduced to 4.7 μF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the ESR graphs (Figures 34 through 41), minimum ESR is not a problem when using 10-μF or larger output capacitors.

The following is a partial listing of surface-mount capacitors usable with the TPS71Hxx family. This information (along with the ESR graphs, Figures 34 through 41) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3

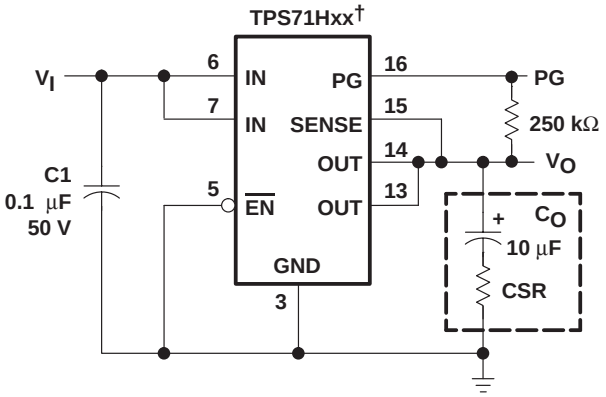
Load < 200 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.



† TPS71H33, TPS71H48, TPS71H50 (fixed-voltage options)

Figure 51. Typical Application Circuit

APPLICATION INFORMATION

programming the TPS71H01 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 52. The equation governing the output voltage is:

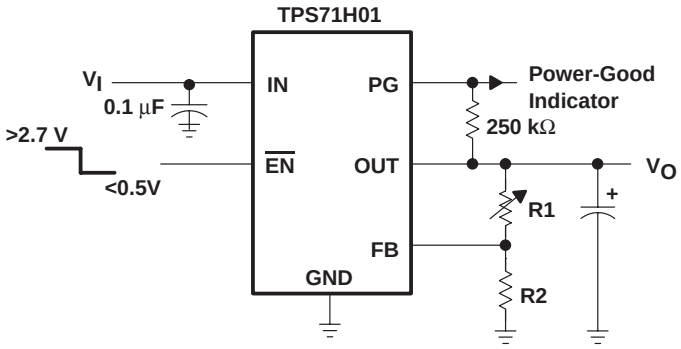
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where

V_{ref} = reference voltage, 1.178 V typ

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 52. TPS71H01 Adjustable LDO Regulator Programming

power-good indicator

The TPS71Hxx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

APPLICATION INFORMATION

regulator protection

The TPS71Hxx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS71Hxx also features internal current limiting and thermal protection. During normal operation, the TPS71Hxx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS71H01QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS71H01QPWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS71H33QPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS71H33QPWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS71H48QPWPLE	OBSOLETE	HTSSOP	PWP	20		TBD	Call TI	Call TI
TPS71H48QPWPRG4	ACTIVE	HTSSOP	PWP	20		TBD	Call TI	Call TI
TPS71H50QPWPRG4	ACTIVE	HTSSOP	PWP	20		TBD	Call TI	Call TI

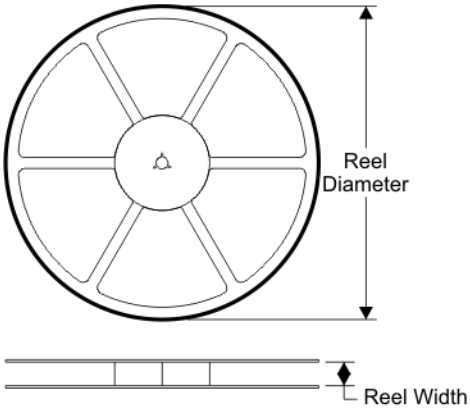
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

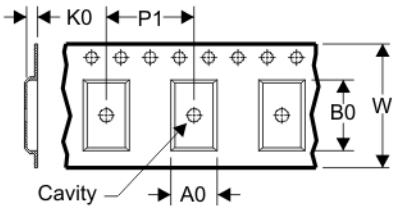
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

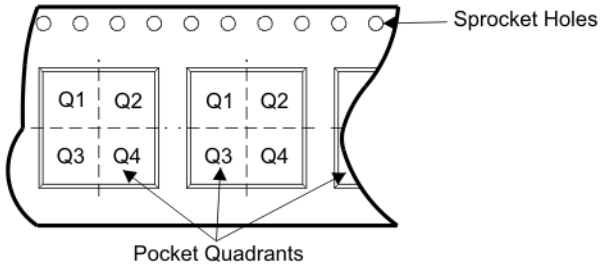


TAPE DIMENSIONS



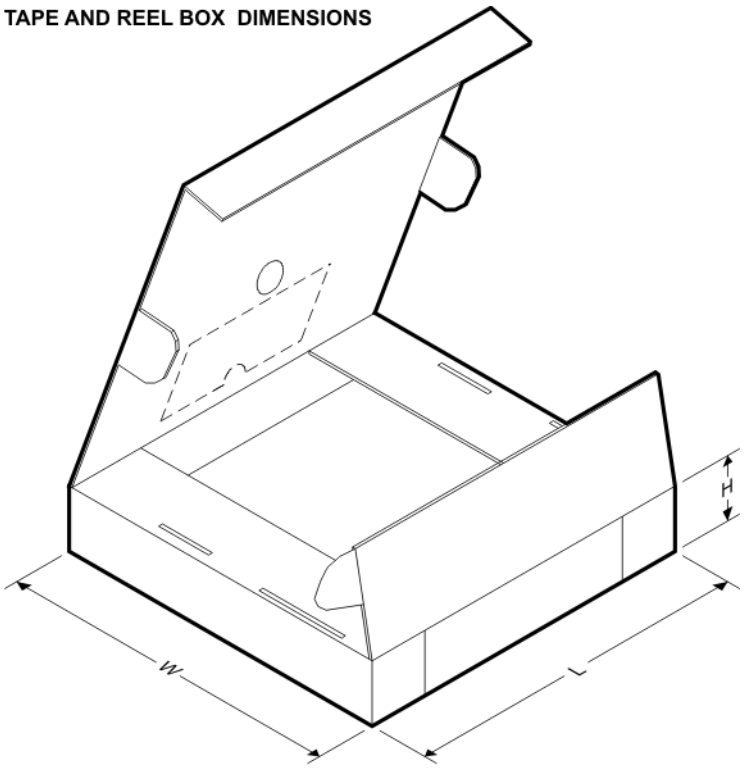
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71H01QPWPR	PWP	20	SITE 60	330	16	6.95	7.1	1.6	8	16	Q1
TPS71H33QPWPR	PWP	20	SITE 60	330	16	6.95	7.1	1.6	8	16	Q1

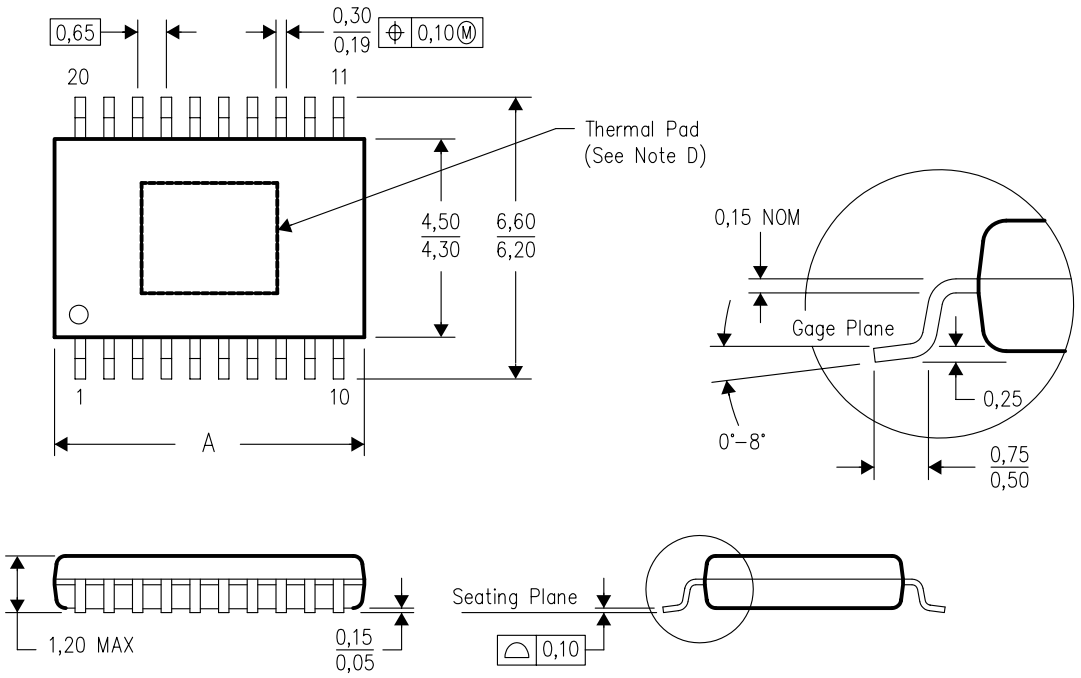
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS71H01QPWPR	PWP	20	SITE 60	346.0	346.0	33.0
TPS71H33QPWPR	PWP	20	SITE 60	346.0	346.0	33.0

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

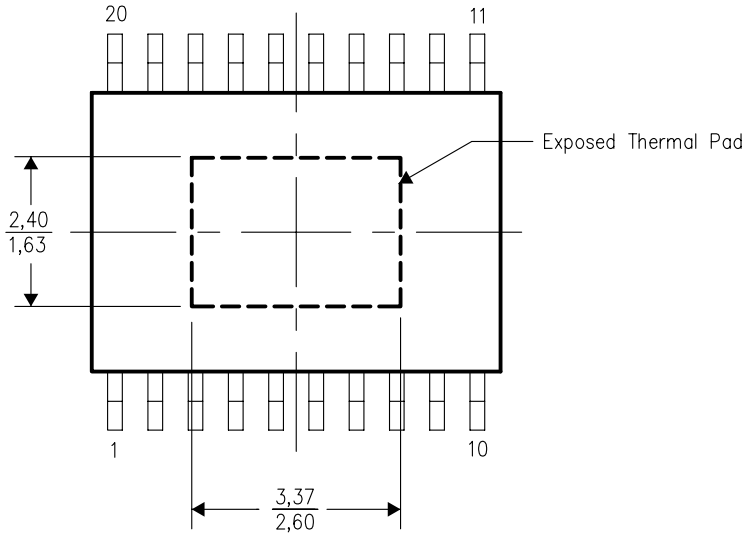
PWP (R–PDSO–G20)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

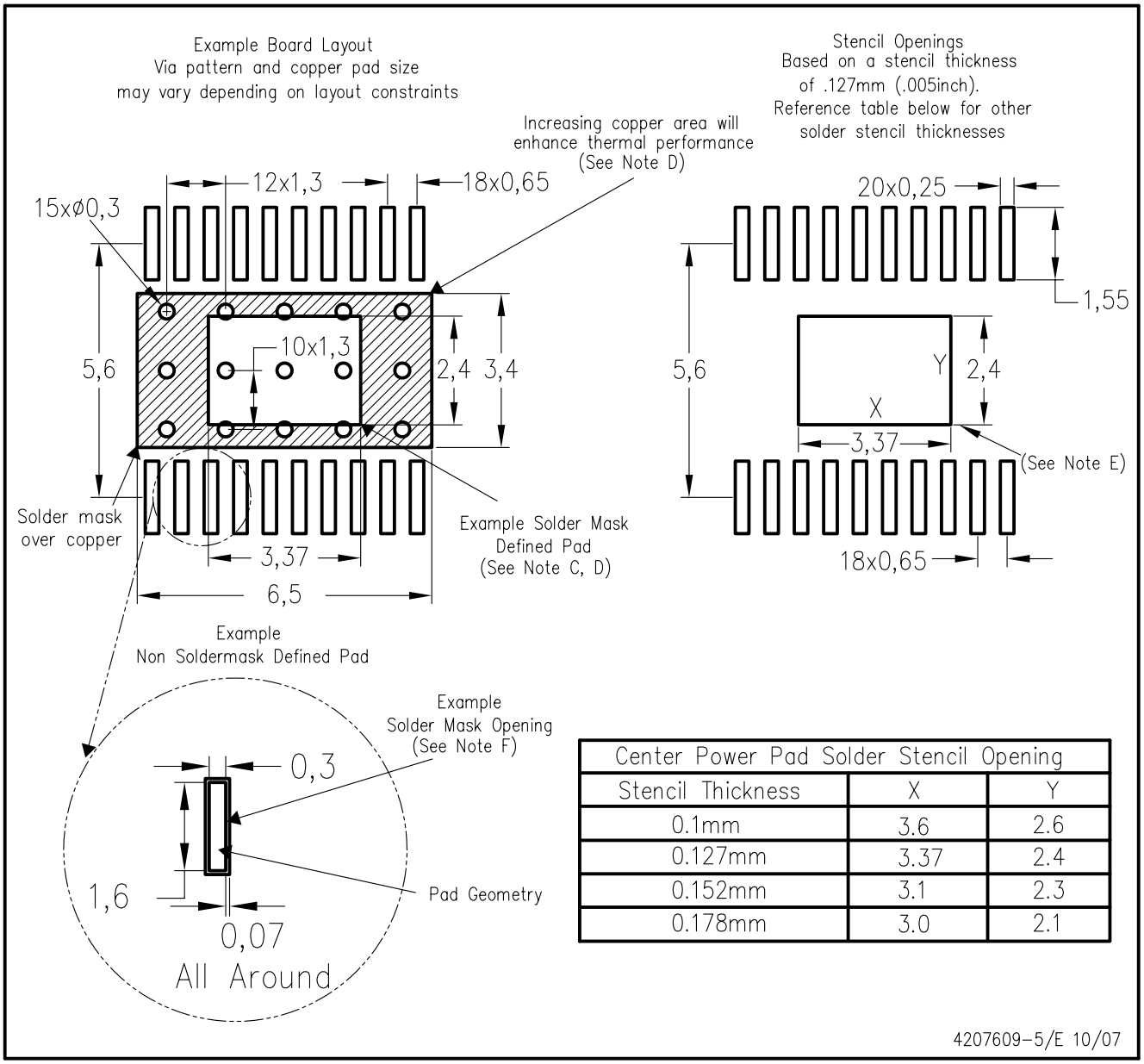


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.6
0.127mm	3.37	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

4207609–5/E 10/07

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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