Ultralow Power, Low Distortion ADC Drivers

Preliminary Technical Data

ADA4940-1/ADA4940-2

FEATURES

Extremely low harmonic distortion: −90 dB THD @ 2 MHz
Low input voltage noise: 4 nV/√Hz
Very low power consumption: 6.5 mW (5 V supply)
1 mV typical offset voltage
Externally adjustable gain
Differential-to-differential or single-to-differential operation
Balanced outputs
16-bit settling time: 85 ns
Output voltage swing from $-V_S$ + 0.1 V to $+V_S$ − 0.1 V
Adjustable output common-mode voltage
Flexible power supplies: 3 V to 7 V
Pb-free, 8-lead SOIC
Pb-free, 3 mm × 3 mm, 16-lead LFCSP
Pb-free, 4 mm × 4 mm, 24-lead LFCSP

APPLICATIONS

Low power ADC drivers
Single-ended-to-differential converters
Differential buffers
Line drivers
Medical imaging
Industrial process controls
Portable electronics

GENERAL DESCRIPTION

The ADA4940-x are low noise, low distortion differential amplifiers with very low power consumption. They are an ideal choice for driving low power, high resolution, high performance SAR, and Σ-Δ analog to digital converters (ADCs) with resolutions up to 18 bits from dc to 2 MHz on just 1.25 mA of quiescent current. The adjustable level of the output common mode allows the ADA4940-x to match the input common-mode voltage of multiple ADCs. The internal common-mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

With the ADA4940-x, differential gain configurations are easily realized with a simple external feedback network of four resistors determining the closed-loop gain of the amplifier. The ADA4940-x is fabricated using Analog Devices, Inc., complementary bipolar process, enabling it to achieve very low levels of distortion with an input voltage noise of only 4 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4940-x make it well suited for a wide variety of data acquisition and signal processing applications.

FUNCTIONAL BLOCK DIAGRAMS

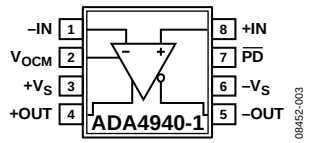

Figure 1. 8-Lead SOIC (Single)

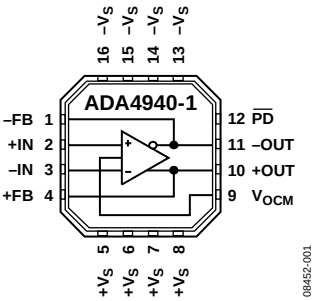

Figure 2.16-Lead LFCSP (Single)

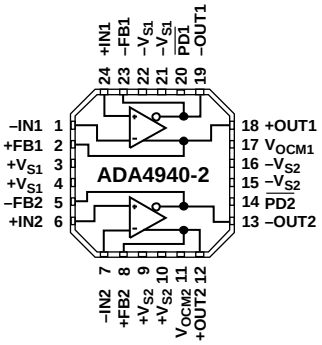

Figure 3. 24-Lead LFCSP (Dual)

The ADA4940-1 is available in a Pb-free, 3 mm × 3 mm, 16-lead LFCSP and 8-lead SOIC. The ADA4940-2 is available in a Pb-free, 4 mm × 4 mm, 24-lead LFCSP. The pinout has been optimized to facilitate the PCB layout and minimize distortion. The ADA4940-1 and ADA4940-2 parts are specified to operate over the −40°C to +105°C temperature range.

Rev. PrB

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SPECIFICATIONS

DIFFERENTIAL INPUT PERFORMANCE

V_S = 5 V, V_{OCM} = 2.5 V, R_F = R_G = 1 kΩ, $R_{L, dm}$ = 1 kΩ, T_A= 25°C, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +105°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{O, dm}$ = 0.1 V p-p		230		MHz
−3 dB Large Signal Bandwidth	$V_{O, dm}$ = 2 V p-p		26		MHz
Bandwidth for 0.1 dB Flatness	$V_{O, dm}$ = 0.1 V p-p		14		MHz
Slew Rate	$V_{O, dm}$ = 2 V step		90		V/µs
Settling Time to 16-Bit Accuracy	$V_{O, dm}$ = 2 V step		85		ns
Overdrive Recovery Time	G = 2, $V_{IN, dm}$ = 12 V p-p triangle wave		80		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	$V_{O, dm}$ = 2 V p-p, f_C = 40 kHz (HD2/HD3)		120/120		dBc
	$V_{O, dm}$ = 2 V p-p, f_C = 1 MHz (HD2/HD3)		108/103		dBc
Second-Order and Third-Order IMD	$V_{O, dm}$ = 2 V p-p, f_C = 1.05 MHz ± 0.05 MHz		94/96		dBc
Input Voltage Noise	f = 100 kHz		3.9		nV/√Hz
Input Current Noise	f = 100 kHz		0.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V		0.25		mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1		µV/°C
Input Bias Current	T_{MIN} to T_{MAX}		1		µA
Input Bias Current Drift			1.3		nA/°C
Input Offset Current			50		nA
Open-Loop Gain			98		dB
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range			−0.2 to +3.8		V
Input Resistance	Differential		33		kΩ
	Common mode		50		MΩ
Input Capacitance	Common mode and differential		1		pF
CMRR	ΔV_{ICM} = ±1 V dc		85		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output		0.1 to 4.9		V
Output Current	Each single-ended output		45		mA
Output Balance Error	f = 1 MHz		65		dB
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		200		MHz
	$V_{O, cm}$ = 2 V p-p		25		MHz
Slew Rate	$V_{O, cm}$ = 2 V p-p		50		V/µs
Gain			1.001		V/V
V_{OCM} INPUT CHARACTERISTICS					
Common-Mode Input Voltage Range			0.8 to 4.3		V
Input Resistance			250		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V		10		mV
Input Voltage Noise	f = 100 kHz		5		nV/√Hz
Input Bias Current			0.3		µA
CMRR (Measured Using 1% Resistors)	$\Delta V_{OCM}/\Delta V_{O, dm}$, ΔV_{OCM} = ±1 V		90		dB

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		3		7	V
Quiescent Current per Amplifier	Powered on		1.25		mA
	Powered off		20		µA
+PSRR	Change in $+V_S$ = ±1 V		90		dB
−PSRR	Change in $-V_S$ = ±1 V		90		dB
OPERATING TEMPERATURE RANGE		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Supply Voltage	TBD V
V_{OCM}	$\pm V_S$
Internal Power Dissipation	TBD mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 3.

Package Type	θ_{JA}	Unit
8-Lead SOIC (Single)/4-Layer		°C/W
16-Lead LFCSP (Single)/4-Layer		°C/W
24-Lead LFCSP (Dual)/4-Layer		°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4940-1/ ADA4940-2 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4940-1/ADA4940-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. RMS voltages and currents should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (θ_{JA} = TBD°C/W, single), 16-lead LFCSP (θ_{JA} = TBD°C/W, single) and 24-lead LFCSP (θ_{JA} = TBD°C/W, dual) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

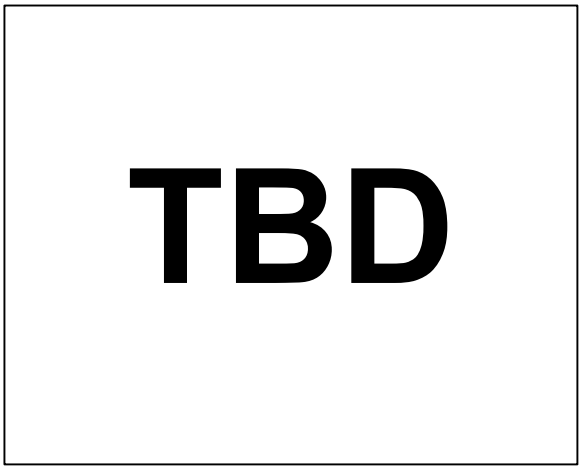

Figure 4. Maximum Safe Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

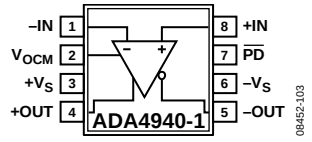

Figure 5. ADA4940-1 Pin Configuration (8-Lead SOIC)

Table 4. ADA4940-1 Pin Function Descriptions (8-Lead SOIC)

Pin No.	Mnemonic	Description
1	−IN	Inverting Input.
2	V_{OCM}	Output Common Mode Voltage.
3	$+V_S$	Positive Supply.
4	+OUT	Positive Output
5	−OUT	Negative Output
6	$-V_S$	Negative Supply.
7	$\overline{PD}$	Power-Down Pin.
8	+IN	Noninverting Input.
EPAD	Exposed paddle (EPAD)	Connect the exposed pad to $-V_S$ or ground.

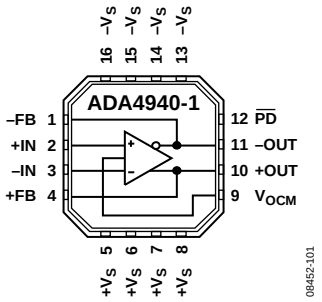

Figure 6. ADA4940-1 Pin Configuration (16-Lead LFCSP)

Table 5. ADA4940-1 Pin Function Descriptions (16-Lead LFCSP)

Pin No.	Mnemonic	Description
1	−FB	Negative Output for Feedback Component Connection
2	+IN	Positive Input Summing Node
3	−IN	Negative Input Summing Node
4	+FB	Positive Output for Feedback Component Connection
5 to 8	$+V_S$	Positive Supply Voltage
9	V_{OCM}	Output Common-Mode Voltage
10	+OUT	Positive Output for Load Connection
11	−OUT	Negative Output for Load Connection
12	$\overline{PD}$	Power-Down Pin
13 to 16	$-V_S$	Negative Supply Voltage
EPAD	Exposed paddle (EPAD)	Connect the exposed pad to −VS or ground.

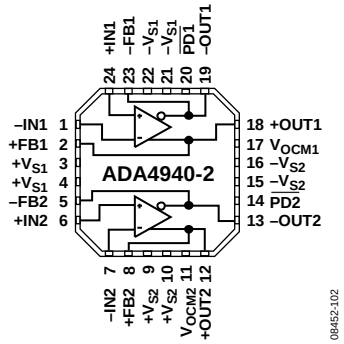

Figure 7. ADA4940-2 Pin Configuration (24-Lead LFCSP)

Table 6. ADA4940-2 Pin Function Descriptions (16-Lead LFCSP)

Pin No.	Mnemonic	Description
1	−IN1	Negative Input Summing Node 1
2	+FB1	Positive Output Feedback Pin 1
3, 4	$+V_{S1}$	Positive Supply Voltage 1
5	−FB2	Negative Output Feedback Pin 2
6	+IN2	Positive Input Summing Node 2
7	−IN2	Negative Input Summing Node 2
8	+FB2	Positive Output Feedback Pin 2
9, 10	$+V_{S2}$	Positive Supply Voltage 2
11	V_{OCM2}	Output Common-Mode Voltage 2
12	+OUT2	Positive Output 2
13	−OUT2	Negative Output 2
14	$\overline{PD2}$	Power-Down Pin 2
15, 16	$-V_{S2}$	Negative Supply Voltage 2
17	V_{OCM1}	Output Common-Mode Voltage 1
18	+OUT1	Positive Output 1
19	−OUT1	Negative Output 1
20	$\overline{PD1}$	Power-Down Pin 1
21, 22	$-V_{S1}$	Negative Supply Voltage 1
23	−FB1	Negative Output Feedback Pin 1
24	+IN1	Positive Input Summing Node 1
EPAD	Exposed paddle (EPAD)	Connect the exposed pad to $-V_S$ or ground.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±2.5 V, G = 1, R_F = R_G = 1 kΩ, R_L = 1 kΩ to ground, unless noted otherwise.

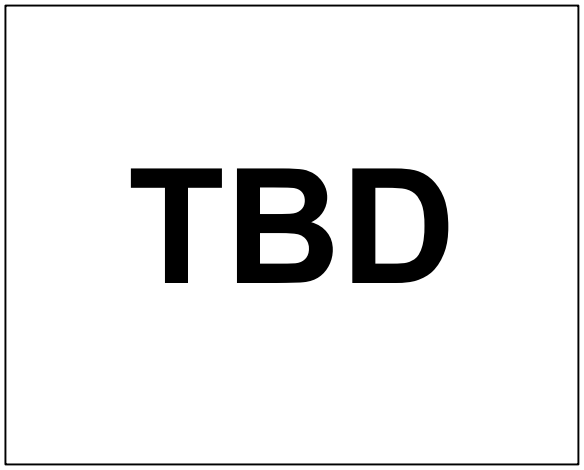

Figure 8. Small Signal Frequency Response for Various Gains (LFCSP)

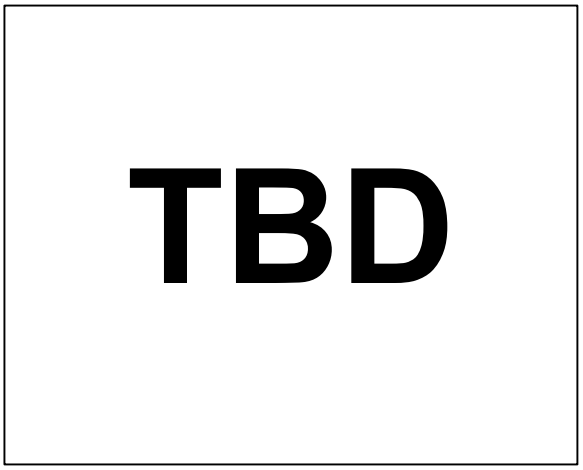

Figure 11. Large Signal Frequency Response for Various Gains

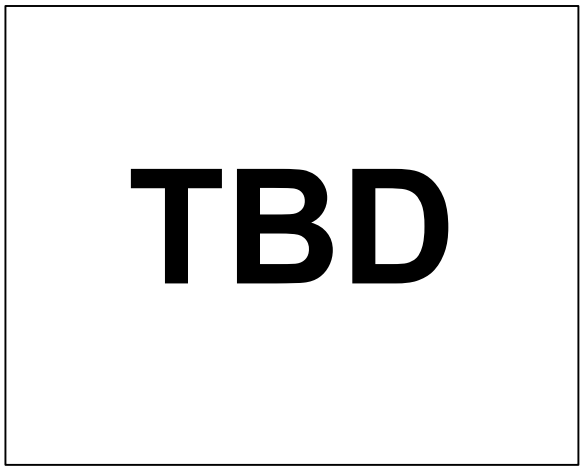

Figure 9. Small Signal Frequency Response for Various Supplies

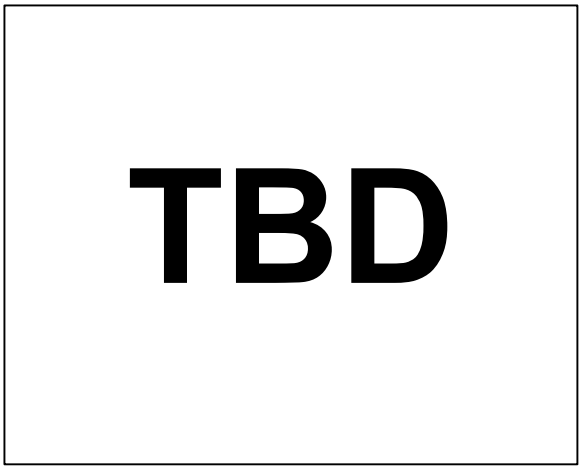

Figure 12. Large Signal Frequency Response for Various Supplies

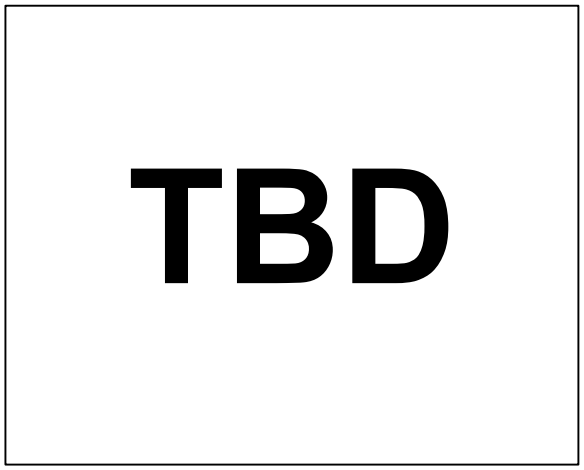

Figure 10. Distortion vs. Frequency and Various Loads

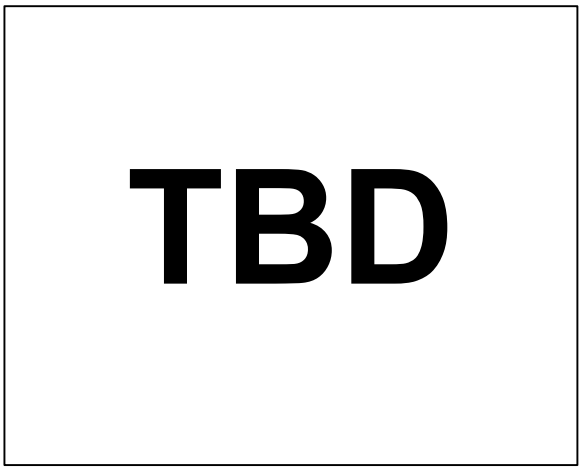

Figure 13. Distortion vs. Frequency and Various Supplies

TEST CIRCUITS

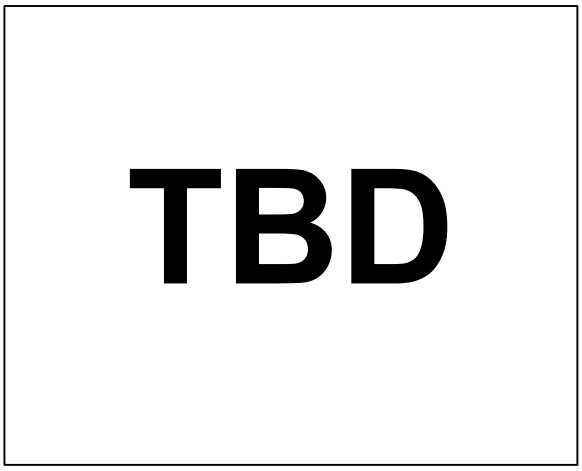

Figure 14. Equivalent Basic Test Circuit

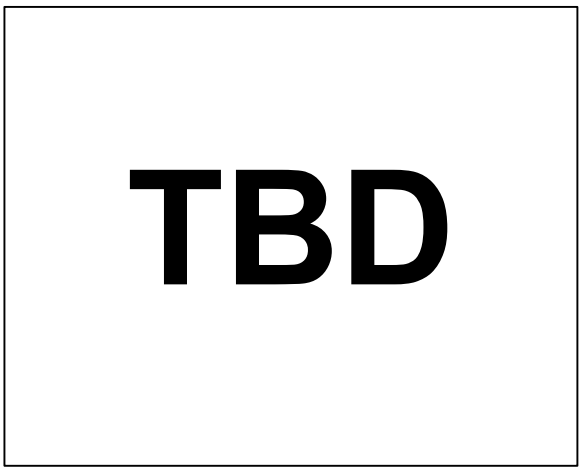

Figure 15. Test Circuit for Output Balance

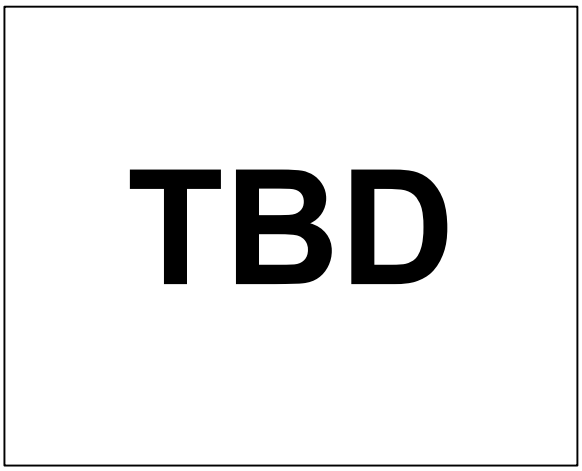

Figure 16. Test Circuit for Distortion Measurements

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

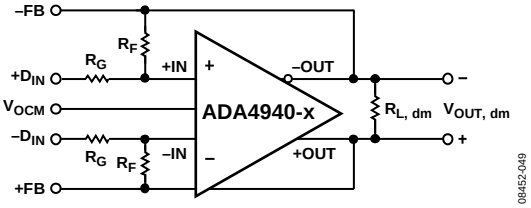

Figure 17. Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-Mode Voltage (CMV)

CMV refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Balance is a measure of how well the differential signals are matched in amplitude and are exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal (see Figure 15). By this definition, the output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The ADA4940-1/ADA4940-2 differ from conventional op amps in that they have two outputs whose voltages move in opposite directions. Like an op amp, they rely on open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4940-1/ADA4940-2 behave much like standard voltage feedback op amps and make it easier to perform single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Also like op amps, the ADA4940-1/ADA4940-2 have high input impedance and low output impedance.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The ADA4940-x architecture results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to zero. This results in nearly perfectly balanced differential outputs that are identical in amplitude and are exactly 180° apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The ADA4940-x uses open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 17). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 17 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes the input resistors (R_G) and feedback resistors (R_F) on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4940-x can be estimated using the noise model in Figure 18. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The noise currents are assumed to be equal and produce a voltage across the parallel combination of the gain and feedback resistances. v_{nCM} is the noise voltage density at the V_{OCM} pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 7 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

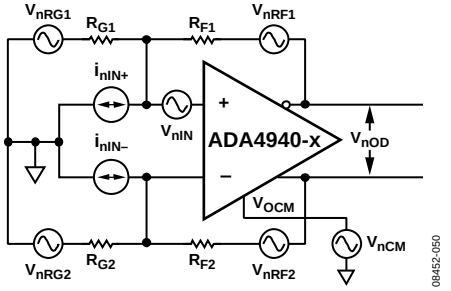

Figure 18. ADA4940-x Noise Model

Table 7. Output Noise Voltage Density Calculations

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Output Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N(v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{G2}\|\|R_{F2})$	G_N	$v_{nO2} = G_N[i_{nIN-} \times (R_{G2}\|\|R_{F2})]$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{G1}\|\|R_{F1})$	G_N	$v_{nO3} = G_N[i_{nIN+} \times (R_{G1}\|\|R_{F1})]$
V_{OCM} Input	v_{nCM}	v_{nCM}	$G_N(\beta_1 - \beta_2)$	$v_{nO4} = G_N(\beta_1 - \beta_2)(v_{nCM})$
Gain Resistor R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	$G_N(1 - \beta_2)$	$v_{nO5} = G_N(1 - \beta_2)(4kTR_{G1})^{1/2}$
Gain Resistor R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	$G_N(1 - \beta_1)$	$v_{nO6} = G_N(1 - \beta_1)(4kTR_{G2})^{1/2}$
Feedback Resistor R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

THE IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from V_{OCM}, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential mode, output offset voltage. When G = 1, with a ground referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, a worst-case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 19, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

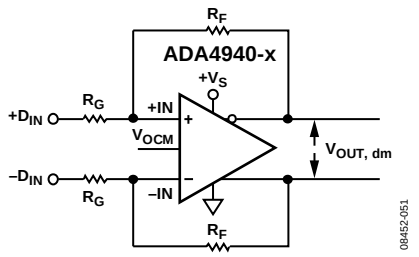

Figure 19. ADA4940-x Configured for Balanced (Differential) Inputs

For an unbalanced, single-ended input signal (see Figure 20), the input impedance is

$$R_{IN, cm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

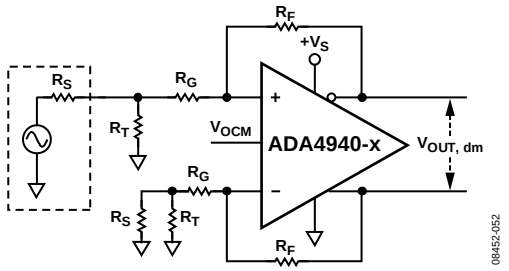

Figure 20. ADA4940-x Configured for Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4940-x is internally biased at a voltage approximately equal to the midsupply point, $[(+V_S) + (-V_S)]/2$. Relying on this internal bias results in an output common-mode voltage that is within approximately 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used. The output common-mode offset listed in the Specifications section assumes that the V_{OCM} input is driven by a low impedance voltage source.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC. However, care must be taken to assure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ. If multiple ADA4940-x devices share one reference output, it is recommended that a buffer be used.

Table 8 and Table 9 list several common gain settings, associated resistor values, input impedance, and output noise density for both balanced and unbalanced input configurations.

Table 8. Differential Ground-Referenced Input, DC-Coupled, 1 kΩ Load; See Figure 19

Nominal Gain (dB)	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)
0				
6				
10				
14				

Table 9. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω, R_L = 1 kΩ; See Figure 20

Nominal Gain (dB)	R_F (Ω)	R_{G1} (Ω)	R_T (Ω)	$R_{IN, cm}$ (Ω)	R_{G2} (Ω)[1]	Differential Output Noise Density (nV/√Hz)
0						
6						
10						
14						

[1] $R_{G2} = R_{G1} + (R_S||R_T)$

LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4940-1/ADA4940-2 are sensitive to the PCB environment in which they operate. Realizing their superior performance requires attention to the details of high speed PCB design.

ADA4940-1 EXAMPLE

The first requirement is a solid ground plane that covers as much of the board area around the ADA4940-1 as possible. However, the area near the feedback resistors (R_F), gain resistors (R_G), and the input summing nodes (Pin 2 and Pin 3) should be cleared of all ground and power planes (see Figure 21). Clearing the ground and power planes minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies.

The thermal resistance, θ_{JA}, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD 51-7.

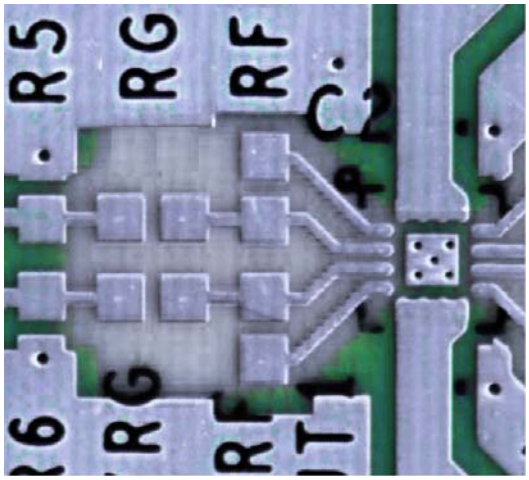

Figure 21. Ground and Power Plane Voiding in Vicinity of R_F and R_G

The power supply pins should be bypassed as close to the device as possible and directly to a nearby ground plane. High frequency ceramic chip capacitors should be used. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 µF) be used for each supply. The 1000 pF capacitor should be placed closer to the device. Further away, low frequency bypassing should be provided, using 10 µF tantalum capacitors from each supply to ground.

Signal routing should be short and direct to avoid parasitic effects. Wherever complementary signals exist, a symmetrical layout should be provided to maximize balanced performance. When routing differential signals over a long distance, PCB traces should be close together, and any differential wiring should be twisted such that loop area is minimized. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

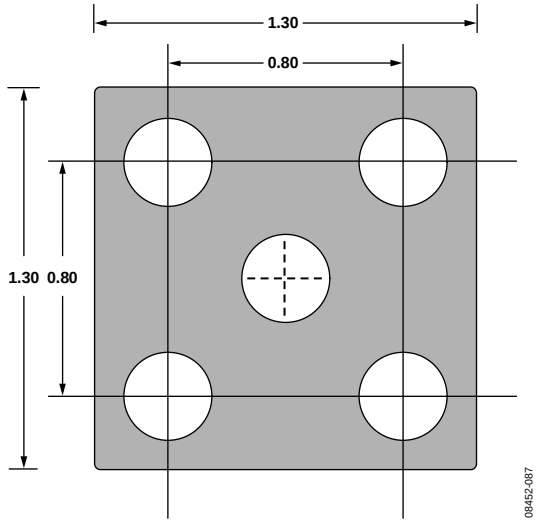

Figure 22. Recommended PCB Thermal Attach Pad Dimensions (Millimeters)

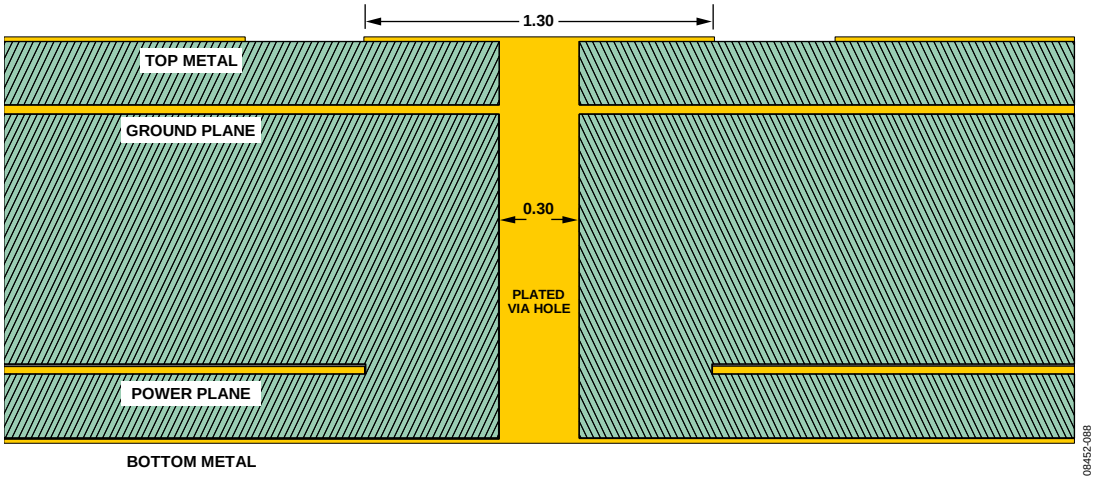

Figure 23. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in Millimeters)

DRIVING HIGH PRECISION ADC

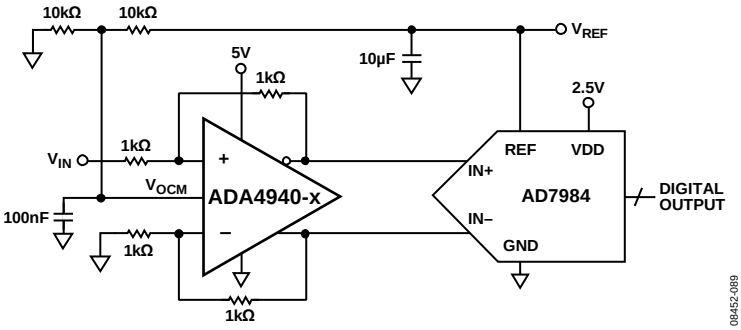

Figure 24. ADA4940-1/ADA4940-2 Driving the AD7984 ADC

OUTLINE DIMENSIONS

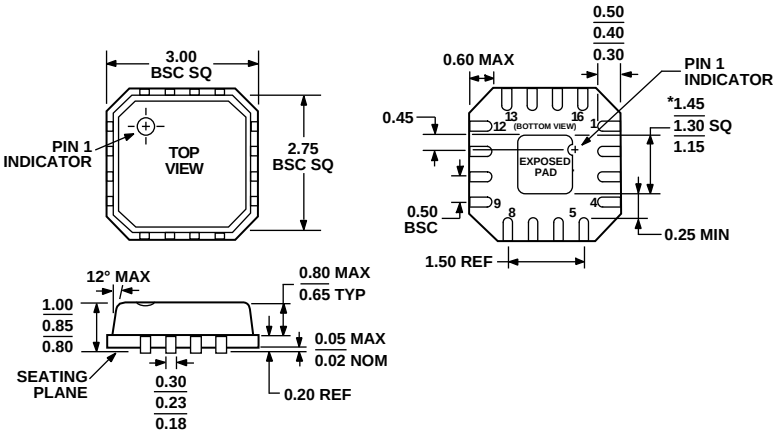

Figure 25. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-2)
Dimensions shown in millimeters

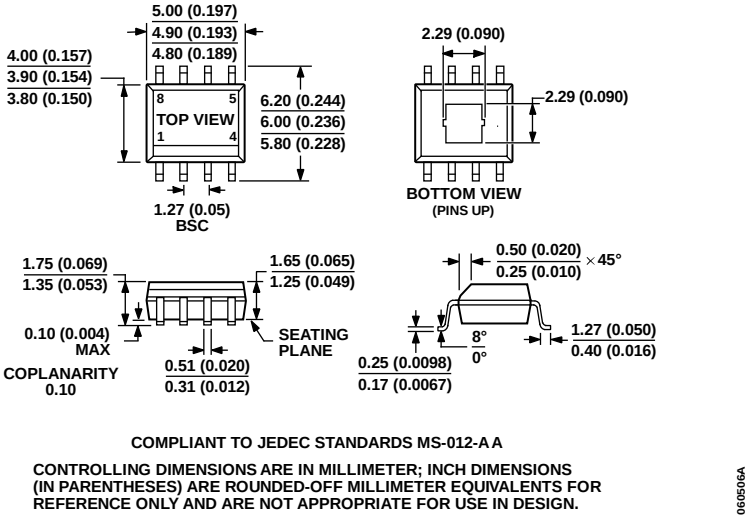

Figure 26. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters and (inches)

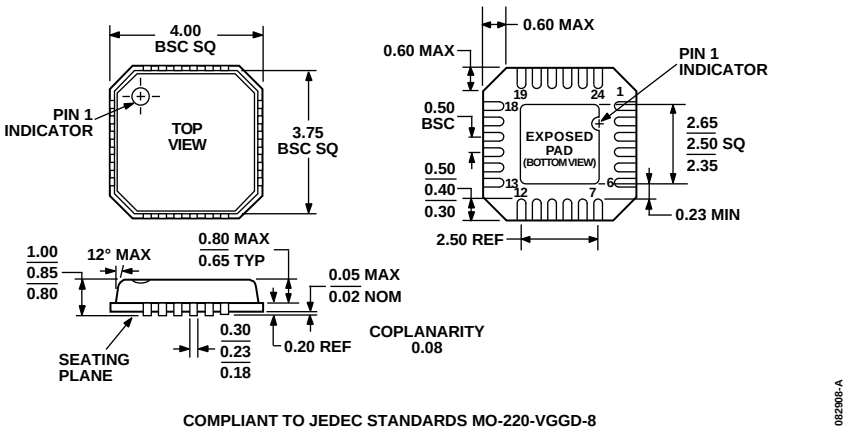

Figure 27. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4940-1ACPZ-R2	–40°C to +105°C	16-Lead LFCSP_VD	CP-16-2	250	
ADA4940-1ACPZ-RL	–40°C to +105°C	16-Lead LFCSP_VD	CP-16-2	5,000	
ADA4940-1ACPZ-R7	–40°C to +105°C	16-Lead LFCSP_VD	CP-16-2	1,500	
ADA4940-1ARDZ	–40°C to +105°C	8-lead SOIC_N_EP	RD-8-1	1	
ADA4940-1ARDZ-RL	–40°C to +105°C	8-lead SOIC_N_EP	RD-8-1	2,500	
ADA4940-1ARDZ-R7	–40°C to +105°C	8-lead SOIC_N_EP	RD-8-1	1,000	
ADA4940-2ACPZ-R2	–40°C to +105°C	24-Lead LFCSP_VQ	CP-24-3	250	
ADA4940-2ACPZ-RL	–40°C to +105°C	24-Lead LFCSP_VQ	CP-24-3	5,000	
ADA4940-2ACPZ-R7	–40°C to +105°C	24-Lead LFCSP_VQ	CP-24-3	1,500	

[1] Z = RoHS Compliant Part.

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PR08452-0-3/10(PrB)