MOTOROLA

MC74AC373
MC74ACT373

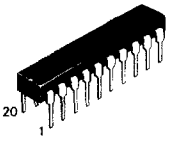
Product Preview

Octal Transparent Latch with 3-State Outputs

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The MC74AC373/74ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

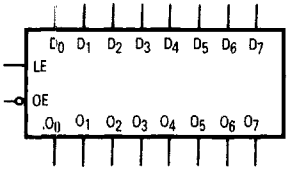
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT373 Has TTL Compatible Inputs

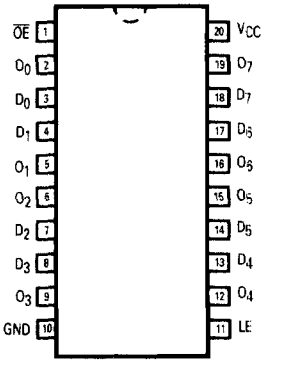


N SUFFIX
CASE 738-03
PLASTIC

DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
$\overline{LE}$	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-State Latch Outputs

TRUTH TABLE

Inputs			Outputs
$\overline{OE}$	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

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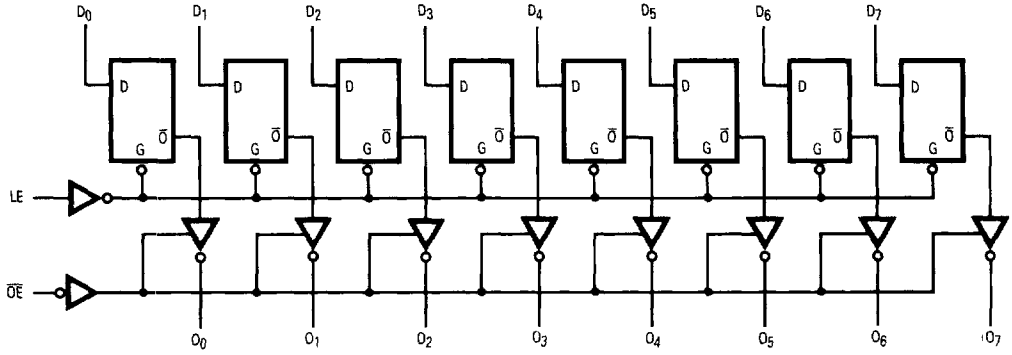
FUNCTIONAL DESCRIPTION

The MC74AC373/74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT373)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0	1.0 1.0	10 7.0	13.5 9.5	1.0 1.0	15 10.5	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0	1.0 1.0	9.5 7.0	13 9.5	1.0 1.0	14.5 10.5	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0	1.0 1.0	10 7.5	13.5 9.5	1.0 1.0	15 10.5	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.5	1.0 1.0	14 10.5	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	9.0 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	8.5 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	10 8.0	12.5 11	1.0 1.0	14.5 12.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	3.5 2.0	5.5 4.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−3.0 −1.5	0 0	0 0	ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.0	5.5 4.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	1.0	8.5	10	1.0	11.5	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.0	8.0	10	1.0	11.5	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0	1.0	8.5	11	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0	1.0	8.0	10	1.0	11.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	8.0	9.5	1.0	10.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.5	9.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	9.0	11	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.5	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	3.0	7.0	8.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0	0	1.0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V

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