Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am29821A/Am29823A/Am29825A
Am29921A/Am29923A/Am29925A

High-Performance Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - CP-Y t_{PD} = 6 ns typical
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down. Outputs have Schottky clamp to ground
- I_{OL}: 48 mA Commercial, 32 mA Military
- Higher speed, lower power versions of the Am29821, Am29823, & Am29825
- Am29900A DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

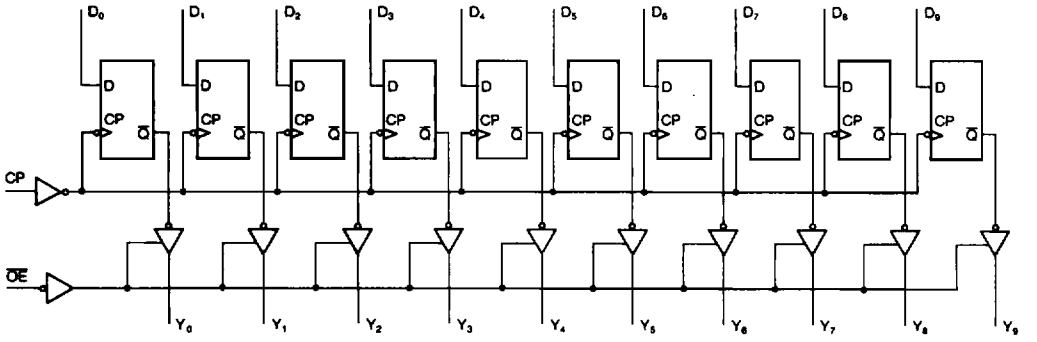
The Am29821A, Am29823A, and Am29825A Buffered Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for address/data paths or buses carrying parity. The Am29800A registers are produced with AMD's exclusive IMOX* bipolar process, and feature typical propagation delays of 6 ns, as well as high-capacitive drive capability.

The Am29821A is a buffered, 10-bit version of the popular '374/'534 functions. The Am29823A is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The Am29825A, an 8-bit buffered register, has all the 9-bit controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multi-user control of the interface; e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. The device is ideal for use as an output port requiring high I_{OL}/I_{OH}.

The Am29800A registers are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for registers with this pinout are the Am29921A, Am29923A, and Am29925A; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS**

Am29821A



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*IMOX is a trademark of Advanced Micro Devices, Inc.
**See following page for additional Block Diagrams.

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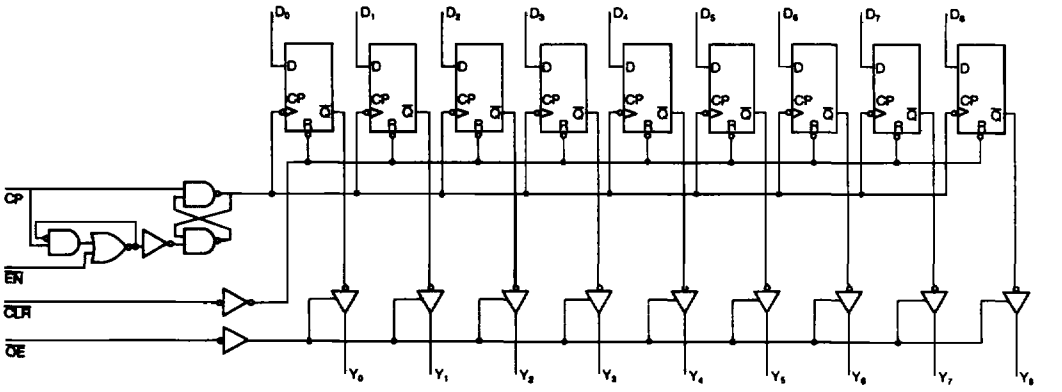
Issue Date: January 1988

BLOCK DIAGRAMS (Cont'd.)

Am29823A



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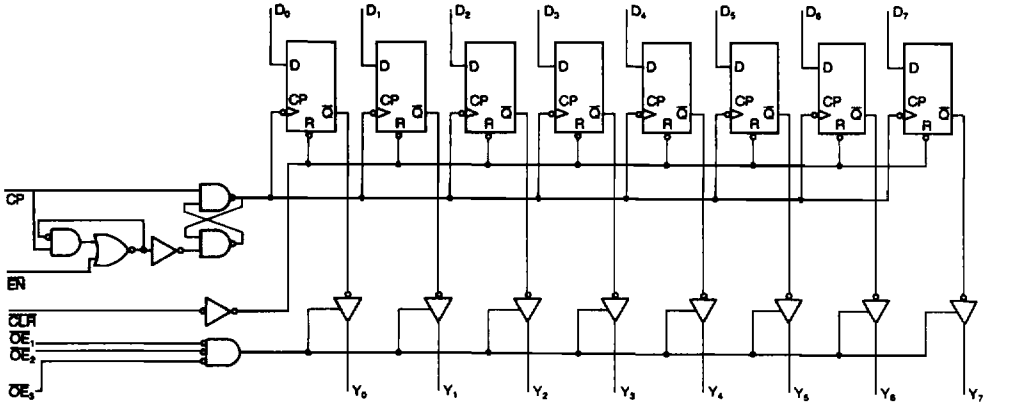
Am29825A



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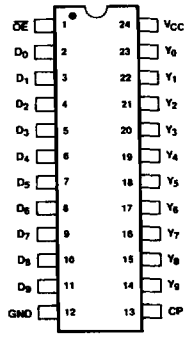
CONNECTION DIAGRAMS
Top View

Am29821A

DIPs*



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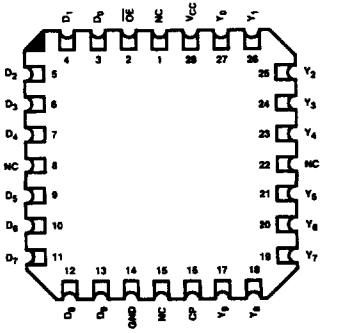
LCC**



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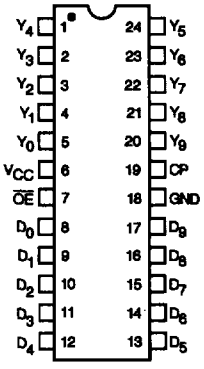
Am29921A

DIPs



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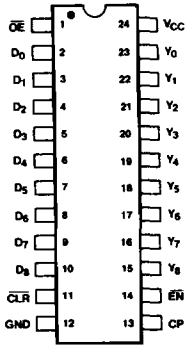
Am29823A

DIPs*



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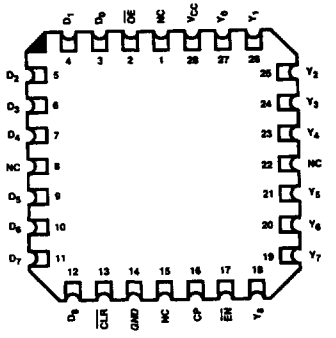

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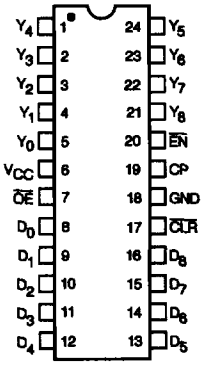
Am29923A
DIPs



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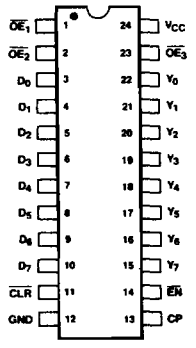
Am29825A

DIPs*



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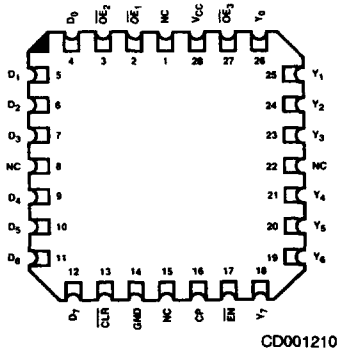
LCC**



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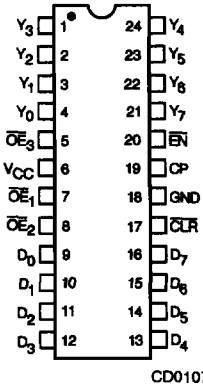
Am29925A
DIPs



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*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

FUNCTION TABLES (Cont'd.)

Am29823A

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	$\overline{Q_I}$	Y_I	Function
H H	H H	L L	L H	↑ ↑	H L	Z Z	Hi-Z
H L	L L	X X	X X	X X	H H	Z L	Clear
H L	H H	H H	X X	X X	NC NC	Z NC	Hold
H H L L	H H H H	L L L L	L H L H	↑ ↑ ↑ ↑	H L H L	Z Z L H	Load

Am29825A

Inputs					Internal	Outputs	
OE*	$\overline{CLR}$	$\overline{EN}$	D_I	CP	$\overline{Q_I}$	Y_I	Function
L L	H H	L L	L H	↑ ↑	H L	Z Z	HI-Z
L H	L L	X X	X X	X X	H H	Z L	Clear
L H	H H	H H	X X	X X	NC NC	Z NC	Hold
L L H H	H H H H	L L L L	L H L H	↑ ↑ ↑ ↑	H L H L	Z Z L H	Load

*OE is an Active-HIGH internal signal produced as follows:

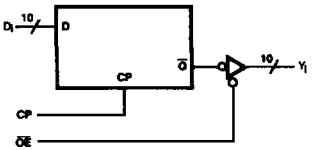
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

LOGIC SYMBOLS

Am29821A



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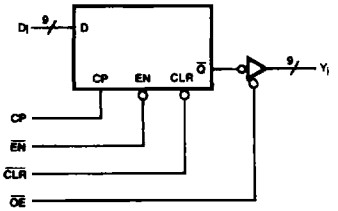
Am29823A



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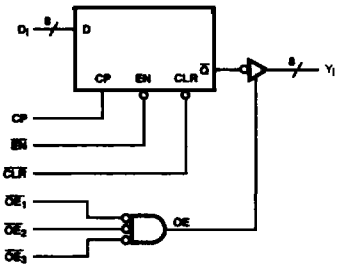
Am29825A



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FUNCTION TABLES

Am29821A

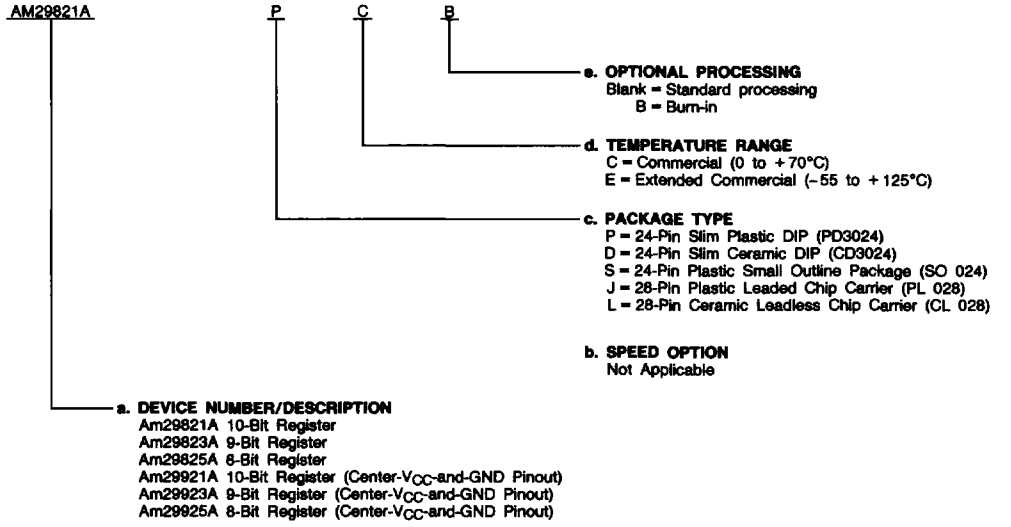
Inputs			Internal	Outputs	
$\overline{OE}$	D_I	CP	$\overline{Q}_I$	Y_I	Function
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

H = HIGH
L = LOW

↑ = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29821A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29823A	
AM29825A	
AM29921A	PC, PCB, DC, DCB, DE
AM29923A	
AM29925A	

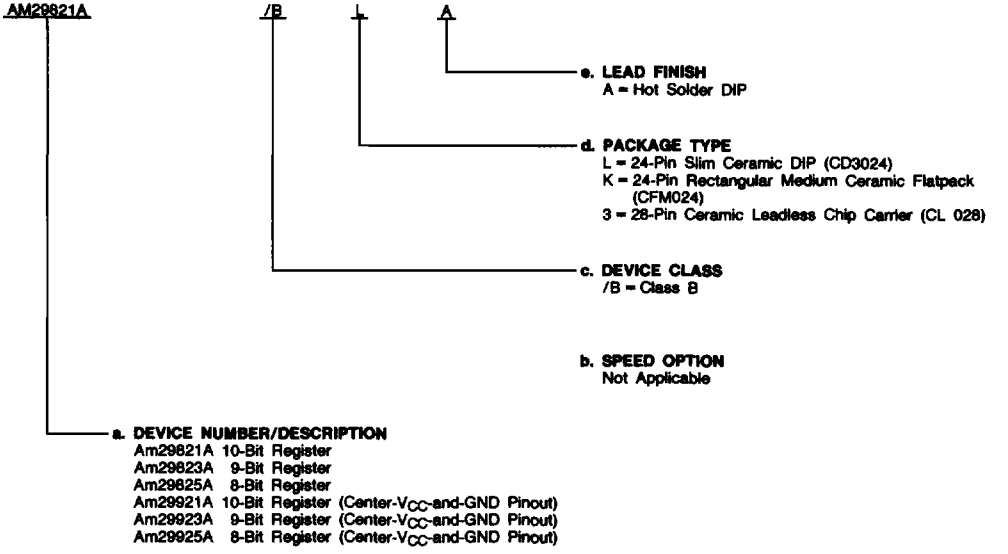
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29821A	/BLA, /BKA, /B3A
AM29823A	
AM29825A	
AM29921A	/BLA
AM29923A	
AM29925A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_i Data Input (Input)
D_i are the register data inputs.

Y_i Data Outputs (Output)
Y_i are the three-state data outputs.

CP Clock Pulse (Input, LOW-to-HIGH Transition)
Clock Pulse is the clock input for the registers. Data is entered into the registers on LOW-to-HIGH transitions.

Am29821A Only

$\overline{OE}$ Output Enable (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is transferred to the Y_i outputs.

Am29823A Only

$\overline{EN}$ Clock Enable (Input, Active LOW)
When the $\overline{EN}$ input is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of data or clock input transitions.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the Y_i outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.

$\overline{OE}$ Output Enable (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are put in the high-impedance state. When $\overline{OE}$ is LOW, the register data is passed to the Y_i outputs.

Am29825A Only

$\overline{EN}$ Clock Enable (Input, Active LOW)
When the $\overline{EN}$ input is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of data or clock input transitions.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and all $\overline{OE}_i$ are LOW, the Y_i outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the register.

$\overline{OE}$ Output Enables (Input, Active LOW)
When $\overline{OE}_1$, $\overline{OE}_2$, and $\overline{OE}_3$ are all LOW, register data is passed to the Y_i outputs. If any or all $\overline{OE}_i$ are HIGH, the Y_i outputs are put in a high-impedance state.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to 5.5 V
DC Input Voltage ..... −1.5 V to +6.0 V
DC Output Current, into Outputs ..... 100 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		Volts
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA		0.5	Volts
			COM'L, I_{OL} = 48 mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−500	μA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	μA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	μA
I_{OZL}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V	V_O = 0.4 V		−50	μA
I_{OZH}			V_O = 2.7 V		50	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	μA
I_{CC}	Supply Current (Note 3)	Am29821A/Am29921A	Outputs LOW		100	mA
			Outputs HIGH		88	
			Outputs Hi-Z		97	
		Am29823A/Am29823A	Outputs LOW		100	mA
			Outputs HIGH		88	
			Outputs Hi-Z		96	
		Am29825A/Am29925A	Outputs LOW		94	mA
			Outputs HIGH		84	
			Outputs Hi-Z		92	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.
3. Clock input, CP, is HIGH after clocking in data. Parameter tested with V_{CC} = Max. and outputs unloaded.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	3.5	8	3.5	9	ns
t_{PHL}				3.5	10	3.5	11.5	ns
t_S	Data to $\overline{CP}$ Setup Time			4		5		ns
t_H	Data to $\overline{CP}$ Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ⌜‾) to CP Setup Time			6		7		ns
t_S	Enable ($\overline{EN}$ _⌟) to CP Setup Time			4		5		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		2		ns
t_{PHL}	Propagation Delay, Clear to Y_i				14		15	
t_{REC}	Clear ($\overline{CLR}$ _⌟) to CP Setup Time			6		8		ns
t_{PWH}	Clock Pulse Width	HIGH		7		8		ns
t_{PWL}		LOW		7		8		ns
t_{PWL}	Clear Pulse Width	LOW		6		7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌜‾ to Y_i				11		12	ns
t_{ZL}					12		13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ _⌟ to Y_i				8		9	ns
t_{LZ}					8		9	ns

*See Test Circuit and Waveforms.