Low EMI Clock Generator for ALI-M1541 for Socket 7 with AGP Boards and Mobile Pentium® II Designs.

Approved Product

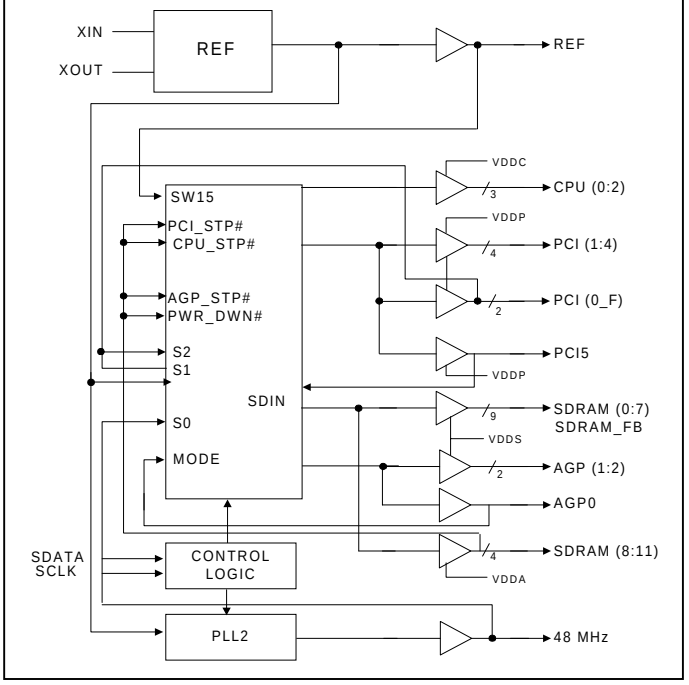
PRODUCT FEATURES

- Supports Pentium®,Pentium®II, M2 & K6 CPUs.
- Supports Mobile Pentium® II
- Supports Synchronous and Asynchronous PCI.
- 3 CPU clocks
- 3 AGP clocks
- Up to 12 SDRAM clocks for 3 DIMs
- 6 PCI synchronous clocks
- Optional common or mixed supply mode:
  (VDD = VDDP = VDDC = 3.3V) or
  (VDD = VDDP = 3.3V, VDDC = 2.5V)
- < 250ps skew among CPU or SDRAM clocks
- < 250ps skew among PCI clocks
- I^2C 2-Wire serial interface
- Programmable registers featuring:
  - Jumperless frequency selection
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- Power Management Capability
- 48 MHz for USB support
- Internal Crystal Load Capacitors
- 48-pin SSOP package
- **Spread Spectrum Technology for EMI reduction**

FREQUENCY TABLE (MHz)

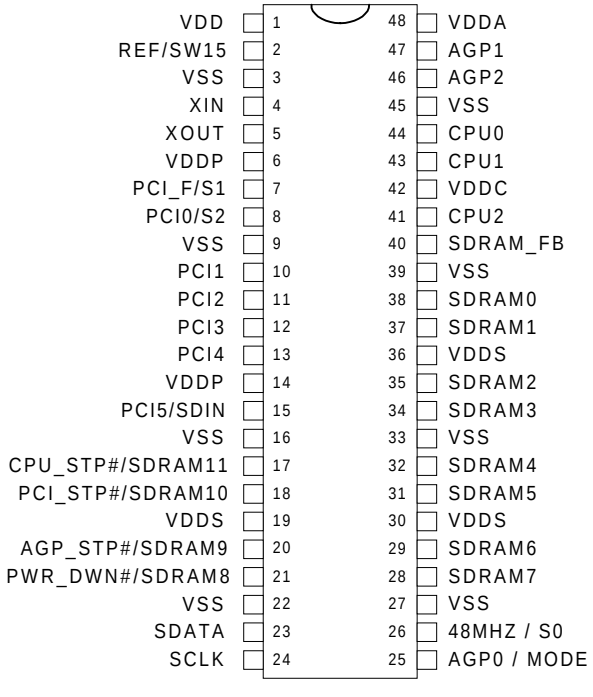
S2	S1	S0	CPU	AGP	PCI
0	0	0	60	60	30
0	0	1	66.8	66.8	33.4
0	1	0	50	50	25
0	1	1	75	75	37.5
1	0	0	75	50	25
1	0	1	83.3	55.53	27.77
1	1	0	90.0	60.0	30.0
1	1	1	100	66.6	33.3

BLOCK DIAGRAM



CONNECTION DIAGRAM

IMISG750



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PIN DESCRIPTION

Pin Number	Pin Name	PWR	I/O	TYPE	Description
4	**XIN**	VDD	I	OSI	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.
5	**XOUT**	VDD	O	OSO	If an external input refernce is used, Pin 5 is left unconnected.
7	**S1**	VDDP	I, PU	-	This is a bidirectional pin. During power up, this pin is an input for frequency selection S1 control bit (see page1,and app note on p. 12).
	PCI_F	VDDP	O	1	When the power reaches the rail (see fig.1, page 4), the input selection is latched internally and this pin becomes a low skew PCI clock output that **does not** stop when PCI_STP# (pin 18) is ascerted low.
8	**S2**	VDDP	I, PU	-	This is a bidirectional pin. During power up, this pin is an input for frequency selection S2 control bit (see page1,and app note on p. 12).
	PCI0	VDDP	O	1	When the power reaches the rail (see fig.1, page 4), the input selection is latched internally and this pin becomes a low skew PCI clock output.
15	**PCI5**	VDDP	O	1	This is a bidirectional pin. Its function is set by pin2 (SW15) at powerup. If SW15 is high (default with internal pull-up), then this pin is a PCI5 output.
	SDin	VDDP	I,PU	1	If SW15 is low (see app note on page 11), then pin 15 is an input for externally generated SDRAM clock source.
10,11,12,13	**PCI(1:4)**	VDDP	O	1	Low skew (<250pS) clock outputs for PCI frequencies. Powered by VDDP.
25	**MODE**	VDDS	I, PU	-	This is a bidirectional pin. During power up, this pin is an input 'MODE' for selecting the direction of pins 17 & 18. when MODE is set high (default, internal pull-up) these bits are SDRAM(10:11) outputs. When MODE is low (see app note on p.11), pins 17 & 18 become inputs for power management purposes.
	AGP0	VDDS	O	1	when the power reaches the rail (see fig.1, p.4), the input selection is latched internally, and this pin becomes an AGP0 clock output. (see table1, page1)
46, 47	**AGP(1:2)**	VDDA	O	1	These pins are AGP clock outputs. (see table1, page1)
44, 43, 41	**CPU(0:2)**	VDDC	O	1	Low skew host clock outputs. (see frequency table 1, page1.)
38,37,35,34,32, 31,29, 28, 40	**SDRAM(0:7) SDRAM_FB**	VDDS	O	1	Low skew SDRAM clock outputs. They are powered by VDDS.
18,17,20, 21	**SDRAM (8:11)**	VDDS	O	1	These are bidirectional pins. When 'MODE' (pin25) is set high, they are SDRAM(8:11) clock outputs.
	CPU_STP# PCI_STP# AGP_STP# PWR_DWN#	VDDS	I,PU	-	When 'MODE' is low, these pins become inputs for power management function. If CPU_STP# is asserted Low, then CPU(0:2) are stopped in low state If PCI_STP# is asserted Low, then PCI(0:4) are stopped in low state. If AGP_STP# is asserted Low, then AGP(0:2) are stopped in low state If PWR_DWN# is asserted Low, then VCO's crystal and buffers are stopped in low state putting the IC in shutdown mode.
2	**SW15**	VDD	I, PU	-	This is a bidirectional pin. During power up, this pin is an input for selecting the direction of pin 15. (see page1,and app note on p.11).
	REF	VDD	O	1	When the power reaches the rail(see fig.1, page 4), the input selection is latched internally and this pin becomes a buffered output of the crystal.
26	**S0**	VDDS	I, PU	-	This is a bidirectional pin. During power up, this pin is an input for frequency selection S0 control bit (see page1 & app note on page 11).
	48MHz	VDDS	O	2	When the power reaches the rail(see fig.1, page 4), the input selection is latched internally and this becomes a 48 Mhz USB clock output.
23	**SDATA**	VDDS	I/O, PU	-	Serial Data for I^2C control interface. This bidirectional pin receives data streams from the I2C bus and outputs an acknowledge for valid data following Philips I^2C slave device standard.
24	**SCLK**	VDDS	I, PU	-	Serial Clock for I^2C control interface.

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PIN DESCRIPTION (Cont.)

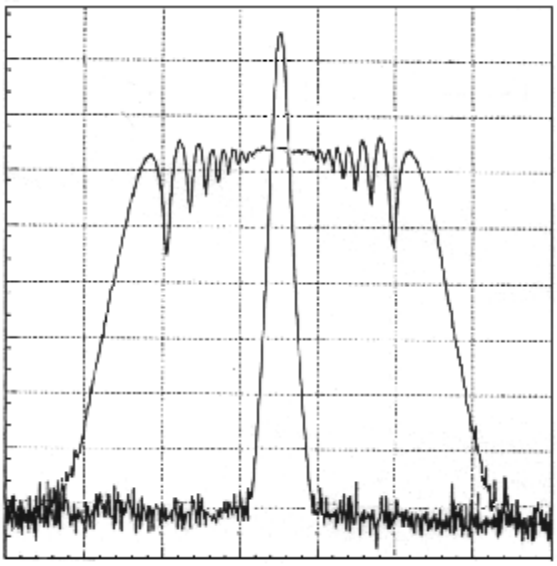
Pin Number	Pin Name	PWR	I/O	TYPE	Description
3, 9, 16, 22, 27, 33, 39, 45	**VSS**	-	PWR		Common ground pins.
1	**VDD**	-	PWR		Power supply for pins 2 and 4
6,14	**VDDP**	-	PWR		Power supply for pins 7,8,10,11,12,13 and 15
19,30,36	**VDDS**	-	PWR		Power supply for pins 17, 18, 20, 21, 23,24, 25, 26, 28, 29, 31, 32, 34, 35, 37, 40, and 38
42	**VDDC**	-	PWR		Power supply for CPU pins 41,43, and 44. May be connected to 3.3v or 2.5v.
48	**VDDA**	-	PWR	-	Power supply for pins 46 and 47

NOTE: 'PU' indicates an internal pull-up (> 100kΩ) is attached to that pin.

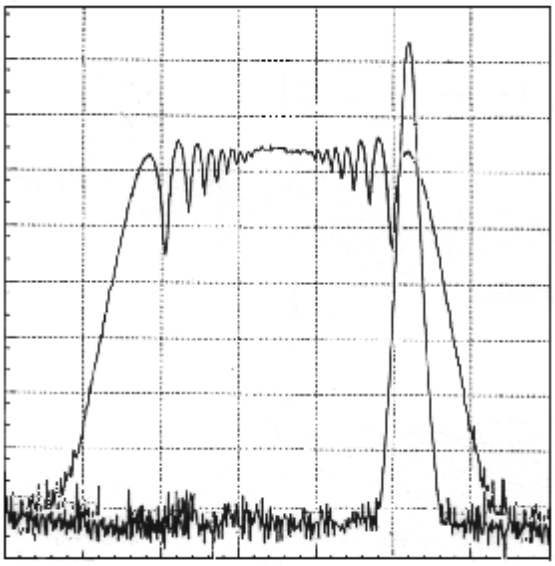
A bypass capacitor (0.1µF) should be placed as close as possible to each VDD, VDDP, VDDS, VDDC, and VDDA pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

SPECTRUM SPREAD CLOCKING

Center Spread



Down Spread



Spectrum Analysis

Low EMI Clock Generator for ALI-M1541 for Socket 7 with AGP Boards and Mobile Pentium® II Designs.

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SPECTRUM SPREADING SELECTION TABLE

Rested Frequency in MHz desired (actual)	Down Spreading (frequencies in MHz)							
	SSW=0				SSW=1			
	F Min	F Center	F Max	Spread	F Min	F Center	F Max	Spread
50 (50.11)	49.24	49.59	49.94	-1.40%	48.91	49.59	50.27	-2.80%
60 (60.00)	59.37	59.72	60.07	-1.16%	59.03	59.72	60.41	-2.33%
66.8 (66.82)	66.01	66.36	66.71	-1.05%	65.67	66.36	67.05	-2.11%
75 (75.00)	74.39	74.74	75.09	-0.94%	74.04	74.74	75.44	-1.87%
83.3 (83.18)	81.78	82.12	82.46	-0.84%	81.44	82.12	82.80	-1.68%
90 (90.00)	89.39	89.75	90.11	-0.80%	89.06	89.75	90.44	-1.54%
100 (99.88)	98.20	98.54	98.88	-0.70%	97.85	98.54	99.23	-1.41%
Rested Frequency in MHz desired (actual)	Center Spreading (frequency in MHz)							
	SSW=0				SSW=1			
	F Min	F Center	F Max	Spread	F Min	F Center	F Max	Spread
50 (50.11)	49.62	49.97	50.32	+/- 0.70%	49.28	49.97	50.66	+/- 1.38%
60 (60.00)	59.75	60.10	60.45	+/- 0.58%	59.41	60.10	60.79	+/- 1.15%
66.8 (66.82)	66.39	66.74	67.09	+/- 0.52%	66.05	66.74	67.43	+/- 1.04%
75 (75.00)	74.78	75.13	75.48	+/- 0.47%	74.43	75.13	75.83	+/- 0.93%
83.3 (83.18)	83.16	83.51	83.86	+/- 0.42%	82.82	83.51	84.20	+/- 0.83%
90 (90.00)	89.75	90.11	90.47	+/- 0.40%	89.41	90.11	90.80	+/- 0.77%
100 (99.88)	99.59	99.94	100.29	+/- 0.35%	99.24	99.94	100.64	+/- 0.70%

POWER UP BIDIRECTIONAL PIN TIMING

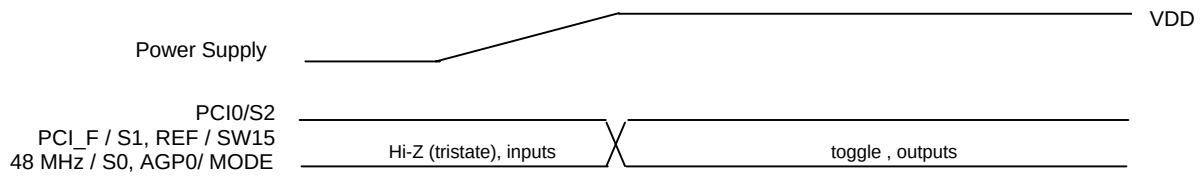

Fig.1

POWER MANAGEMENT FUNCTIONS

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When MODE=0, the device supports power management and pins 17, 18, 20 and 21 are inputs CPU_STP#, PCI_STP#, AGP_STP# AND PWR_DWN# respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the I^2C serial interface and these pins indicate that it should be enabled. The clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. The CPU, PCI, and AGP clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled. See fig.2 below.

CPU_STP#	AGP_STP#	PCI_STP#	PWR_DWN#	CPU	AGP	PCI	OTHER CLK	XTAL & VCO
X	X	X	0	LOW	LOW	LOW	LOW	OFF
0	0	0	1	LOW	LOW	LOW	RUNNING	RUNNING
0	0	1	1	LOW	LOW	RUNNING	RUNNING	RUNNING
0	1	0	1	LOW	RUNNING	LOW	RUNNING	RUNNING
0	1	1	1	LOW	RUNNING	RUNNING	RUNNING	RUNNING
1	0	0	1	RUNNING	LOW	LOW	RUNNING	RUNNING
1	0	1	1	RUNNING	LOW	RUNNING	RUNNING	RUNNING
1	1	0	1	RUNNING	RUNNING	LOW	RUNNING	RUNNING
1	1	1	1	RUNNING	RUNNING	RUNNING	RUNNING	RUNNING

POWER MANAGEMENT TIMING

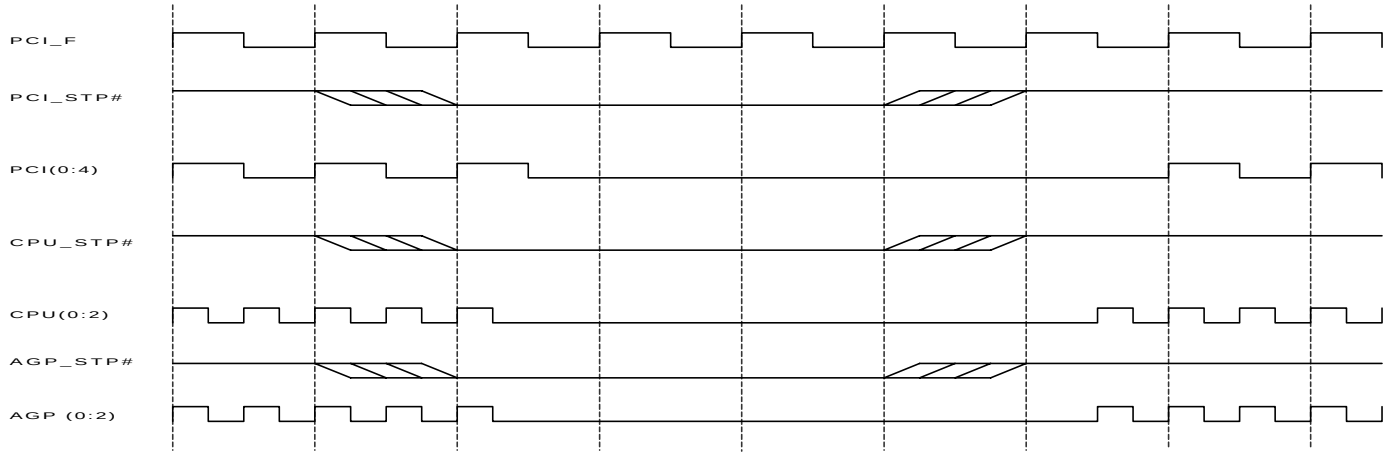

Fig. 2

Please note that all clocks can also be individually (asynchronously) enabled or stopped via the 2-wire I^2C control interface. In this case all clocks are stopped in the low stat.

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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged. After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte 2, ...) will be valid and acknowledged.

Byte 0: Frequency, Function Select Register

Bit	@Pup	Pin#	Description
7	0	*	SSW bit. Selects Spread Spectrum Modulation Width, 0 = Narrow Modulation, 1=Wide Modulation. See tables on page 4.
6	0	*	S2 (for frequency table selection by software via I²C)
5	0	*	S1 (for frequency table selection by software via I²C)
4	0	*	S0 (for frequency table selection by software via I²C)
3	0	*	0 = frequency is selected by hardware (device pins) 1 = enables frequency selection via software (I²C byte 0)
2	0	*	0 = Center spreading (when Spread Spectrum mode is enabled) 1 = Down spreading (when Spread Spectrum mode is enabled)
1	0	*	0 = Spread Spectrum disabled 1 = Spread Spectrum enabled
0	0		0 = Running 1 = All clock outputs tristate

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SERIAL CONTROL REGISTERS (Cont.)

Byte 1: CPU, SIO, USB Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	48 Mhz enable/Stopped
6	1	-	Reserved
5	1	-	0 = TEST Mode. 1 = Normal Operation.
4	1	-	Reserved
3	1	-	Reserved
2	1	41	CPUCLK2 enable/Stopped
1	1	43	CPUCLK1 enable/Stopped
0	1	44	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	7	PCI_F enable/Stopped
5	1	15	PCI5 enable/Stopped
4	1	13	PCI4 enable/Stopped
3	1	12	PCI3 enable/Stopped
2	1	11	PCI2 enable/Stopped
1	1	10	PCI1 enable/Stopped
0	1	8	PCI0 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	28	SDRAM7 enable/Stopped
6	1	29	SDRAM6 enable/Stopped
5	1	31	SDRAM5 enable/Stopped
4	1	32	SDRAM4 enable/Stopped
3	1	34	SDRAM3 enable/Stopped
2	1	35	SDRAM2 enable/Stopped
1	1	37	SDRAM1 enable/Stopped
0	1	38	SDRAM0 enable/Stopped

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SERIAL CONTROL REGISTERS (Cont.)

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	25	AGP0 enable/Stopped
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	17	SDRAM11 enable/Stopped
2	1	18	SDRAM10 enable/Stopped
1	1	20	SDRAM9 enable/Stopped
0	1	21	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	**Reserved for IMI test.** Must be set to 1 for normal device operation (VR)
6	x	-	Reserved
5	x	-	Reserved
4	1	47	AGP1 enable/Stopped
3	1	-	**Reserved for IMI** test Must be set to 1 for normal device operation. (DT1)
2	1	-	**Reserved for IMI test** Must be set to 1 for normal device operation. (DT0)
1	1	46	AGP2 enable/stopped
0	1	2	REF enable/Stopped

TEST MODE FUNCTION TABLE (ENABLED VIA I^2C BYTE 1 BIT 5)

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Test Mode	XIN/2	XIN/4	XIN/2	XIN	XIN
Normal	see table	see table	CPU	14.318	14.318

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	350	mA	@100 MHz, 3.3 V
Static Supply Current	Isdd	-	-	3	mA	@ powerdown, Active
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDP = VDDS =3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	tOFF	1	-	4	ns	Load: CPU = 20pF measured @1.25V SDRAM = 30pF measured @1.5V PCI = 20pF measured @1.5V
Skew (CPU-CPU), (PCI-PCI), (AGP-AGP), (SDRAM-SDRAM), (AGP-PCI)	tSKEW1	-	-	250	ps	Load: CPU = 20pF measured @1.25V PCI = 30pF measured @1.5V AGP = 20pF measured @1.5V SDRAM = 30pF measured @1.5V
Skew (CPU-SDRAM)	tSKEW2	-	-	500	ps	Load: CPU = 20pF measured @1.25V SDRAM = 30pF measured @1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Propagation Delay SDin to SDRAM(0:11)	tPD	2	4	6	nS	SDRAM ouputs loaded @ 30pF, measured @1.5V
VDD = VDDP = VDDS = 3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB4L1 TYPE BUFFER CHARACTERISTICS FOR AGP(0:2), SDRAM (0:11, FB), AND REF0						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	18	-	23	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5 V
Pull-Down Current Min	IOL_{min}	13	-	25	mA	Vout = 0.4 V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5 V
Rise/Fall Time @ (0.4 V - 2.0 V)	TRF	0.4	-	1.6	nS	Load : Min = 10 pF, Max = 20pF
VDD = VDDP = VDDS =3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

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BT5LP1 TYPE BUFFER CHARACTERISTICS FOR 48MHz						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	17	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	30	-	44	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	13	-	19	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	32	-	44	mA	Vout = 1.5 V
Rise/Fall Time @ (0.4 V - 2.4 V)	TRF	0.5	-	2.0	nS	Load : Min = 15 pF, Max = 30pF
VDD = VDDP = VDDS =3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB4L1_V TYPE BUFFER CHARACTERISTICS FOR CPU (0:2						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	20	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	22	-	37	mA	Vout = 1.25 V
Pull-Down Current Min	IOL_{min}	18	-	23	mA	Vout = 0.4 V
Pull-Down Current Max	IOL_{max}	50	-	61	mA	Vout = 1.5 V
Rise/Fall Time @ (0.4 V - 2.0 V)	TRF	0.4	-	1.6	nS	Load : Min = 10 pF, Max = 20pF
VDD = VDDP = VDDS =3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB4LP1 TYPE BUFFER CHARACTERISTICS FOR PCI (0:5,F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	18	-	23	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5 V
Pull-Down Current Min	IOL_{min}	18	-	25	mA	Vout = 0.4 V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5 V
Rise/Fall Time @ (0.4 V - 2.0 V)	TRF	0.4	-	1.6	nS	Load : Min = 10 pF, Max = 20pF
VDD = VDDP = VDDS =3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resistance (ESR)	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)

For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore	=	2.0 pF
Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore	=	18.0 pF
the total parasitic capacitance would therefore be	=	20.0 pF

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

Low EMI Clock Generator for ALI-M1541 for Socket 7 with AGP Boards and Mobile Pentium® II Designs.

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APPLICATION NOTE FOR SELECTION ON BIDIRECTIONAL PINS

Pins 2, 7, 8, 25 and 26 are Power up bidirectional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode (see Fig1, page4), therefore, they are considered input select pins internal to the IC, these pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 5ms settling time), then it is recommended to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see FIG. 3A and Fig. 3B.

Fig. 3A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.3A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 3B represents a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

If the system power supply is fast (less than 5ms settling time), then FIG3A only applies and Pull up Rup resistor is not necessary.

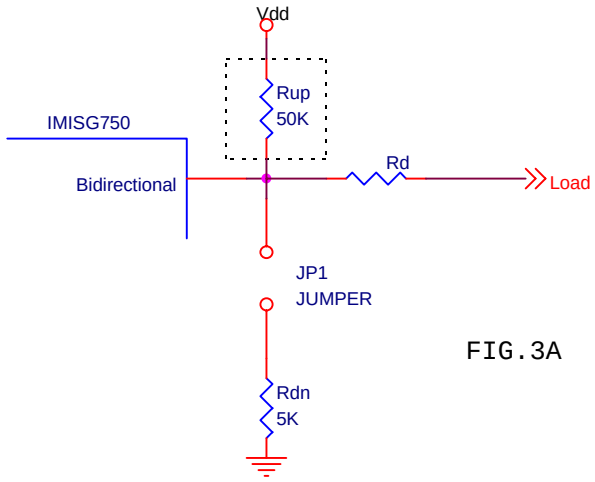

FIG.3A

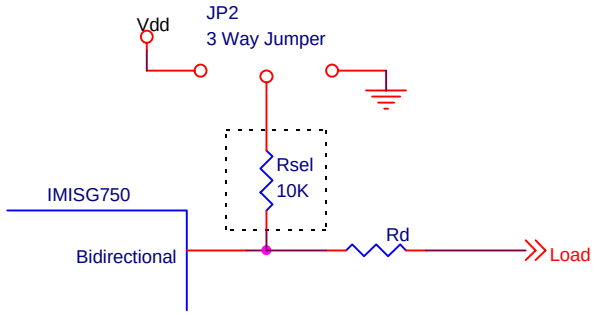

FIG.3B

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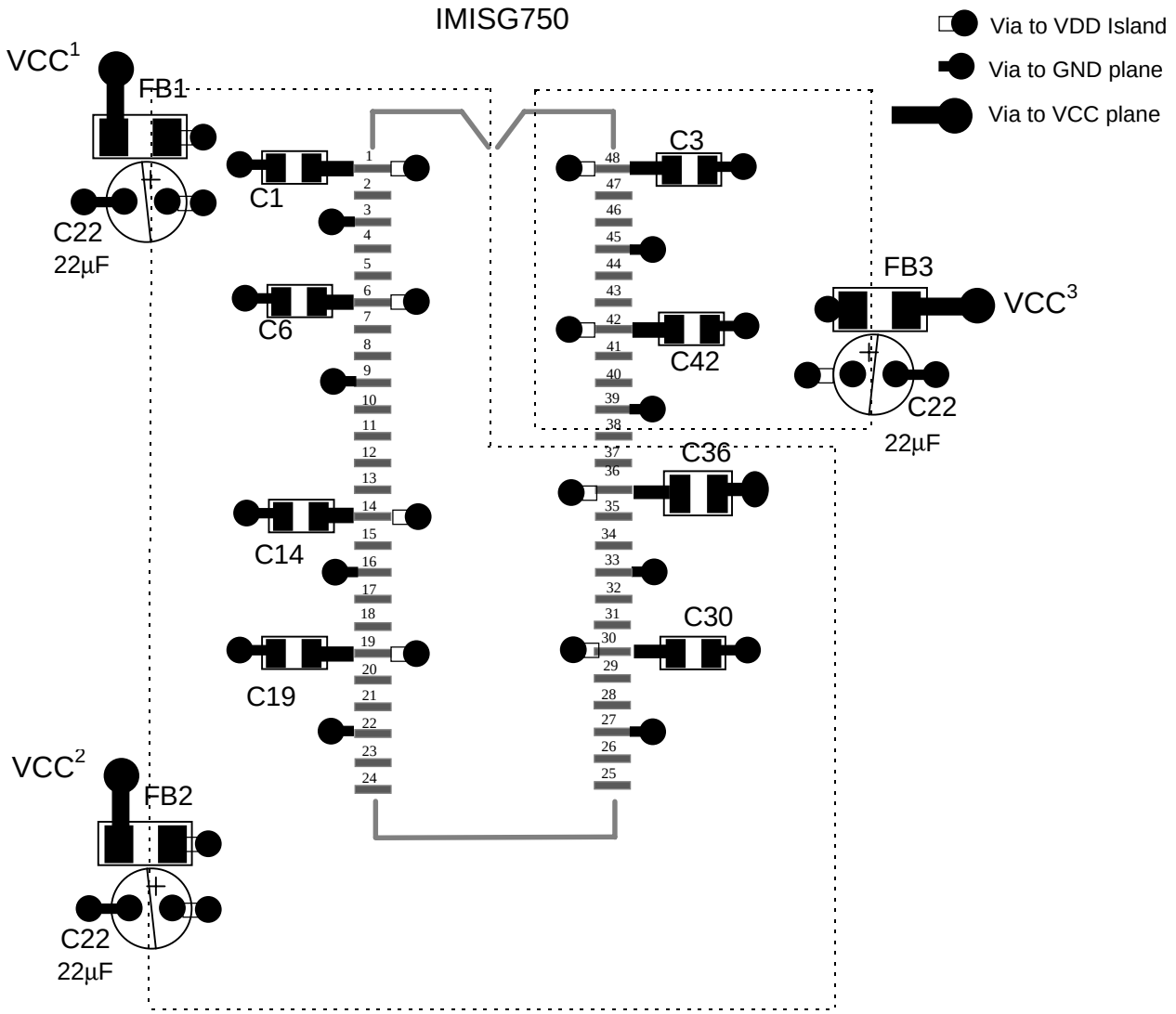
PCB LAYOUT SUGGESTION



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C1, C6, C14, C19, C3, C42, C36 and C30 (all are 0.1µF) should always be used and placed as close as possible to their VDD pins.

Low EMI Clock Generator for ALI-M1541 for Socket 7 with AGP Boards and Mobile Pentium® II Designs.

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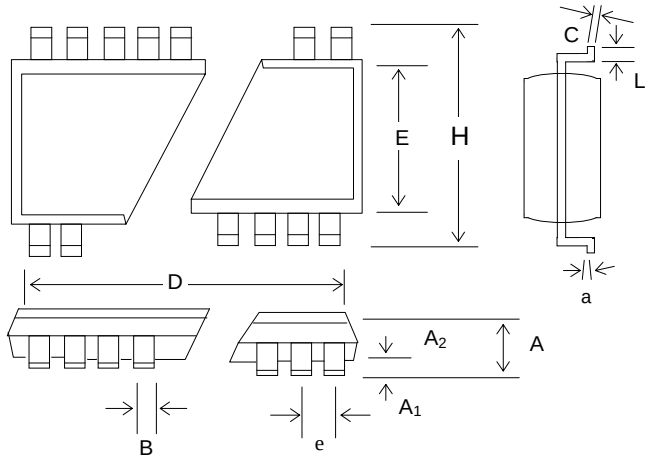
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG750CYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG750CYB
Date Code, Lot #

IMISG750CYB

- Flow
  B = Commercial, 0ºC to + 70ºC
- Package
  Y = SSOP
- Revision
- IMI Device Number

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